LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

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UK UIM Coil Driver Pre-Production Prototype Bench Test and Evaluation		
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1 Introduction and Executive Summary

1.1 Introduction

This report documents the bench test results and evaluation of the AdL Suspension UIM Driver Pre-production Prototype chassis supplied by the University of Birmingham. Bench tests were conducted in accordance with LIGO document number T080021-v2, "UK UIM Driver Pre-Production Test Plan". A link to the completed test plan with results is included in Appendix A of this document. The design requirements for the UIM Driver can be found in LIGO document number T060067-00-C, "AdL Quad Suspension UK Coil Driver Design Requirements".

The format of this report roughly follows the format of LIGO document T070288-00-C, "Adl Noise Prototype Electronics Test Plan". The tests outlined in T0700288-00-C are a series of tests and evaluations that will be used to evaluate the full set of electronics provided by the University of Birmingham for the AdL Quad Suspension system. The major categories of the plan are:
Manufacturing
Operational
Performance
This test report covers relevant portions corresponding to each of these categories.

1.2 Executive Summary

The UIM Pre-Production Prototype chassis supplied to AdL for test represents a large step forward from the original prototype chassis supplied earlier in 2008. The chassis appears to meet all requirements set forth in LIGO document number T060067-00-C, "AdL Quad Suspension UK Coil Driver Design Requirements". The only deficiencies noted are:

- The channel order for the voltage, current and rms current monitor is reversed from the channel order for all other connections. On most connections to the chassis, channel 1 connections start at pin 1 of the connector and proceed sequentially up through channel 4. On the J1 connector of the monitor board this order is reversed with channel 4 starting on pin 1, followed by channel 3, channel 2 and channel 1. While the order of channels is somewhat arbitrary this deviation from what may be considered the nominal order should be noted and may cause some confusion during operation in the future.
- The jumper wires on the monitor board used to correct a layout problem (see figure 6 below) represent a possible failure mechanism. If the layout of the monitor board is not corrected prior to production, a more robust means of attaching and securing the jumper wires needs to devised.
- The schematics provided with the chassis appear to document the UIM board and the monitor board. A test plan for the UIM board itself was supplied, but no test results for the boards or the chassis were supplied. No test plan for the monitor board or the fully assembled chassis was supplied.
- Neither a quick start guide nor a description of the operation of the chassis was supplied. Prior to production a full set of documentation including these items, a complete bill of materials and all design files need to be provided.

2 Manufacturing

2.1 Quality of Manufacture

The UIM Driver chassis provided to LIGO for testing and evaluation is a pre-production prototype. Once it has been determined that the pre-production prototype has met the requirements and that all deficiencies noted in this report are corrected the design can be declared frozen and the UK can begin production of all UIM units required for AdL. The photos below are front and rear views of the UIM Driver with the cover removed.

Figure 1: UIM Preproduction Prototype (PP) Chassis Front View

Figure 2: UIM PP Chassis Rear View

2.1.1 Chassis Labeling and Identification

As can be seen from the photos, front and rear panel panels are professionally manufactured and all connection clearly labeled. The serial number for the chassis appears on the back panel and is applied using a label maker. This should be acceptable for production units.

Figure 3: UIM PP Chassis Serial Number

Power indicators are included on the front and rear panels and are clearly labeled.

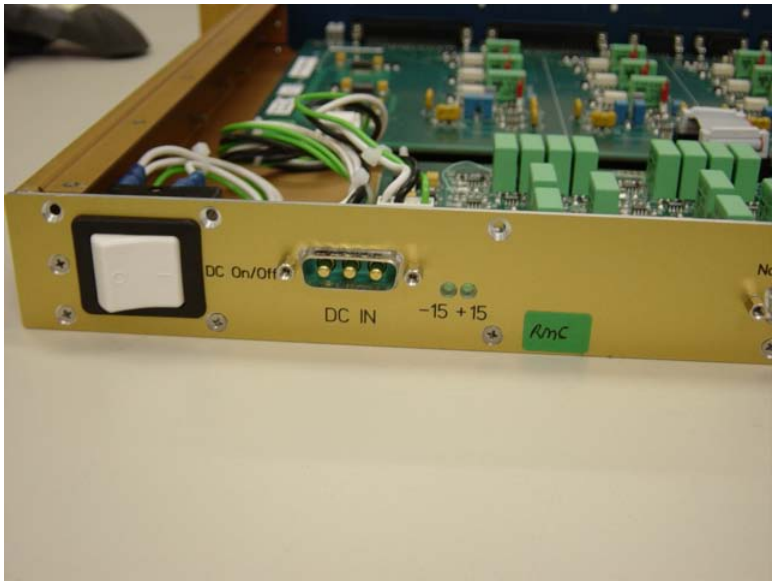

Figure 4: UIM PP Chassis Power Indicators

2.1.2 Circuit Boards

The photo below is a closer view of the UIM Driver board. As can be seen from the picture, the circuit board is multi-layer, professionally manufactured circuit board. Each channel of the circuit board flows from the front to the rear of the chassis and appears to have been produced using the multi-channel design features available in Altium. This is a very efficient and convenient way to produce designs that utilize the same circuit topology for multiple channels. When this feature is used, the logical designators for each component in the design are the same since the channel number portion of the physical designator is suppressed on the silkscreen. Each channel of the design is clearly labeled and designated on the silkscreen of the board.

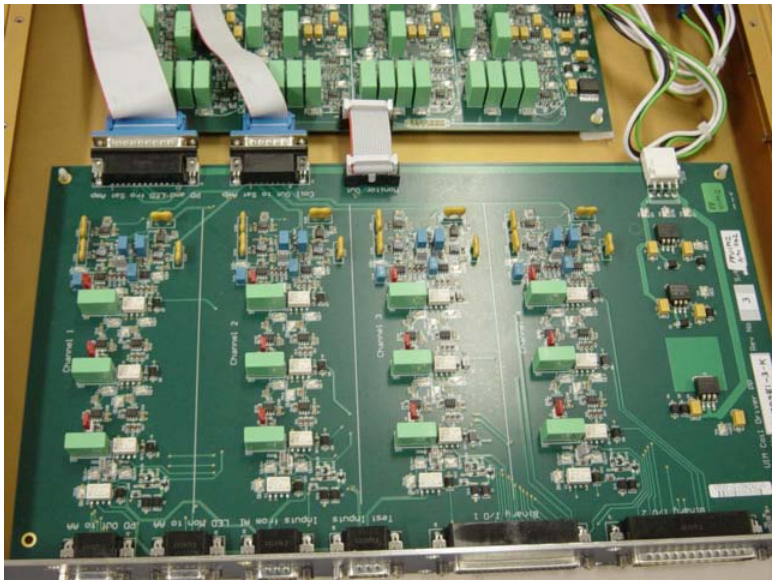

Figure 5: UIM PP Driver Board

The Monitor board was manufactured in a similar fashion and the only circuit board issues observed are the wires added from TP8 to R24 of each channel. These wires were added after circuit board

manufacture to correct an omission. It should be noted that one of these wires was broken free on the R24 end of the connection during shipment from the UK to the US. Prior to testing this connection was repaired. Production models of the Monitor board should be corrected so that these wires are not necessary. Both boards (driver and monitor) are identified in the space provided with the drawing number, revision number and serial number for the board. The circuit board (pcb artwork) revision number is included on the silkscreen for each board.

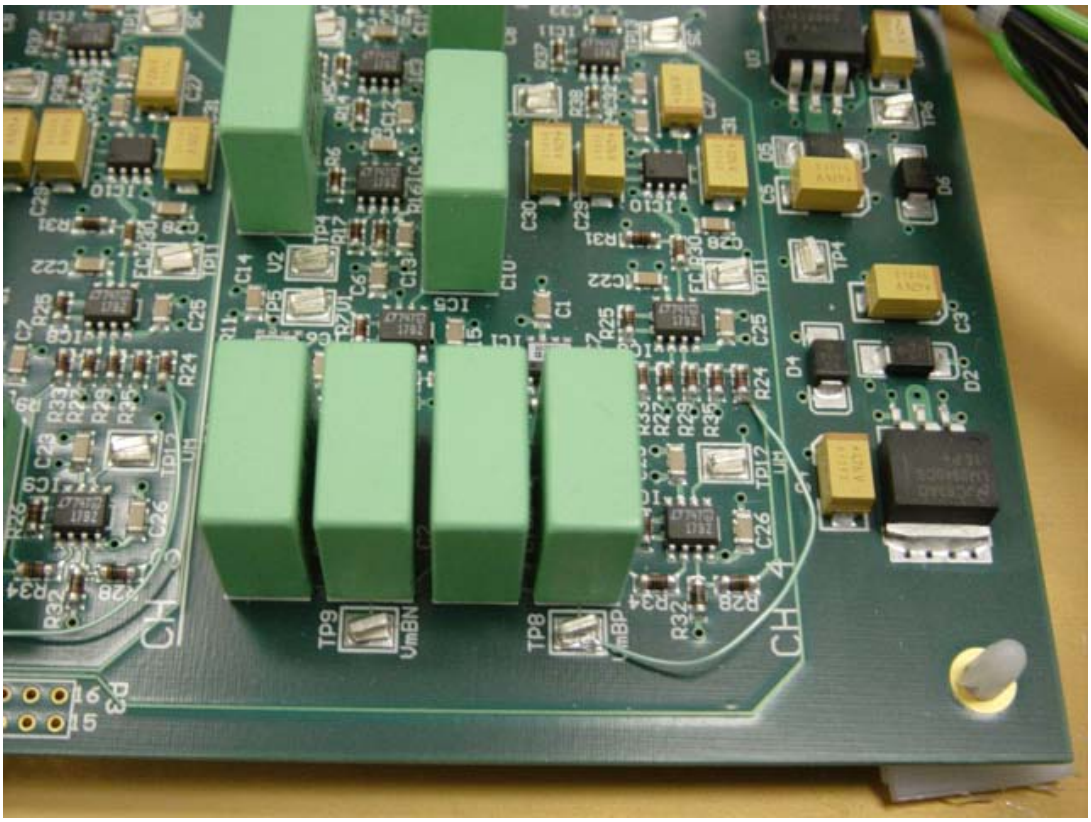

Figure 6: UIM PP Monitor Board Jumper Wires

Each of the circuit boards (Driver and Monitor) has many test points that are clearly labeled. These test points are the same SMT style that has been used in many LIGO and AdL designs. Several of the test points are visible in the picture above.

2.1.3 Cabling, Connectors and Harnesses

The photo below is a closer view of the input power connections and chassis power wiring. As can be seen from the picture, the internal power harness wiring does follow the LIGO power wiring color code. In this case, the positive voltage, return and negative voltage wire colors are white, black and green, respectively. Heat shrink has been included over the power connector pins to prevent inadvertent shorting of the pins. Individual wires in the power harness have been tied together and routed neatly inside the chassis. The Molex connections used are the same crimp pin style used in other AdL designs and the pins and wires are adequate for the currents involved.

Figure 7: UIM PP Chassis Power Harness

The connectors used for incoming and outgoing field cables are sub D connectors. These connectors all have jack screws used for retaining the field cables and are acceptable for the production units. Internal cabling, with the exception of the power wiring noted above, is either IDC sub D or keyed header/receptacle and is acceptable for the production units.

2.2 Serviceability

The chassis used for the UIM PP is a LIGO style 1U chassis manufactured by Hamilton Metalcraft Inc. and is acceptable for the production units.

Although a complete bill of materials was not provided, a check of the availability of the capacitors used in the critical portions of the circuit showed that they may not be readily available in the US. If this is the case, then an adequate number of spares need to be provided with the production units. The same can be said of any other components used in the designs. This possibility will need to be evaluated when a complete set of documentation is supplied.

The layout of the boards in the chassis, and positioning of the connectors does allow for easy removal or access to most of the components on the boards. The only exception is for a few of the components on the monitor board that are mounted under the output connectors attached to the rear panel of the chassis. While this not optimal, it should be acceptable for the production units.

As can be seen in several of the pictures, the circuit boards are attached to the chassis using standoffs that stick to the bottom panel of the chassis. These temporary standoffs were used in place of the permanently mounted standoffs planned for the production chassis. Permanently mounted standoffs are a requirement for production units as previous experience has shown that the adhesive used for the temporary standoffs will give way during shipping and/or over the life of the chassis.

2.3 Adequacy of Documentation

A complete set of paper schematics was provided for the driver and monitor boards. No bill of materials, chassis test plans, test results, quick start guide or other documentation was provided. Prior to production, all materials listed in Electronics Requirements document (T060067) and LIGO document T000053-04-D, “Universal Suspension Subsystem Design Requirements Document” will need to be evaluated. Additionally it is preferred that all Altium schematics, gerber files, and other documentation be provided electronically.

3 Operational

3.1 Interfaces

The interfaces (connector types, pinouts, signal levels) between the University of Birmingham electronics and the AdL Electronics appear to be in compliance with Universal Design Requirements document (T000053).

3.2 Test Inputs and Monitoring

The design of the UIM PP Driver includes test inputs for each channel. These test inputs are connected to the input and can be enabled or disabled via an external control signal or a local board connection. When the test input is connected, the input from the control system is disconnected and visa versa. The use of the normally closed contact for the test input allows this relay to be used as a fail-safe enable/disable for the control input. For every relay used in the design there is a separate read back of the actual relay position in accordance with the requirements. One observation worthy of mentioning is that when links W2 and W6 are left open and the test input switch in the normally closed position, there is no bias return path for op amps IC4 and IC8. This leads to amplifier offsets and drifts that may not be acceptable in AdL. It is recommended that W2 and/or W6 be installed during production.

Other monitors included in the design and in accordance with the requirements are:

- Low noise monitor of the driver output
- Output Voltage Monitor
- Fast output current monitor
- RMS current monitor

These appear to be adequate for use in AdL.

3.3 Long Term Reliability and Stability

The tests conducted on the UIM PP Driver Chassis took place over a two week time frame where the unit was intermittently powered and turned off for testing. While no failures or stability issues were observed, this time period is inadequate to determine if there are any long term reliability or stability issues. Additionally, no overheating or heat management issues were observed.

4 Performance

Performance of the chassis was measured using the set of tests outlined in LIGO document T080021-v2. The completed report is can be viewed via the link provided in Appendix A. The sections below summarize the tests results.

4.1 Noise and Dynamic Range

4.1.1 Driver Noise

The noise requirements for the low noise mode of operation are outlined in T060067. For convenience the summary table from T060067 is repeated below.

Table 1: UIM Driver Current Noise Requirements (Low Noise Mode)

Frequency	Current Noise Requirement
1 Hz	0.500 nA/√Hz
10 Hz	3 pA/√Hz
100 Hz	200 nA/√Hz
1000 Hz	1000 nA/√Hz

Note that the requirements are given in units of current spectral density. Measuring current noise directly is very difficult so the tests performed measured the output voltage noise of the driver at the most stringent frequency, which is 10Hz. At this frequency, in order to meet the requirement, the output noise voltage of the driver must be less than 23 nV/√Hz. The measurement of output noise voltage for the driver is described in section 3.2 of the test plan. This can be a very difficult measurement to make as the measurement is subject to many external noise sources. The table below summarizes the driver output noise measurements for each channel.

Table 2: UIM Driver Voltage Noise Measurements at 10Hz (Low Noise Mode)

Channel	Output Noise Measured
Channel 1	26.7 nV/√Hz
Channel 2	24 nV/√Hz
Channel 3	24 nV/√Hz
Channel 4	23 nV/√Hz

As can be seen in the table above, the measured output voltage noise is very close to the requirement and any differences may actually be attributed to measurement error. A better measurement of the actual output noise voltage can be obtained using the Noise Monitor circuitry provided as part of the design. Test results for the monitor are documented in the section below. As can be seen from the results in the section below, the output noise is measured using the noise monitor is at or below the requirement.

4.1.2 Monitor Noise

One of the requirements for monitors on the UIM driver is a noise monitor capable of "seeing" output referred noise voltage of the driver at 10Hz (hardest requirement) in the low noise mode of operation. In an effort to do this, the University of Birmingham has designed a noise monitor that is a high gain AC coupled differential amplifier tied to the voltage output legs of the driver. The design submitted by the University of Birmingham was tested and the actual noise measured compared to the simulation results. These tests and the results are documented section 3.4.2 of the test plan.

Given the design of the monitor circuit and the driver output voltage noise requirement of 23 nV/√Hz at 10 Hz described in section 4.1.1 above the measured output voltage noise of the monitor circuit at 10 Hz should be less than 2.9 uV/√Hz. As can be seen in the summary table below the measured output noise for all channels was at or below this requirement.

Table 3: UIM Driver Monitor Noise Measurements at 10Hz (Low Noise Mode)

Channel	Output Noise Measured
Channel 1	2.7 uV/√Hz
Channel 2	2.7 uV/√Hz
Channel 3	2.6 uV/√Hz
Channel 4	2.9 uV/√Hz

4.1.3 Dynamic Range

The dynamic range requirement for the UIM Driver is 2 mA_{rms} for frequencies less than 1Hz. The dynamic range of the driver was tested in section 3.1.3 of the test plan. The driver appears to meet the dynamic range requirement.

4.1.4 Transfer Function Measurements

4.1.4.1 Driver Transfer Function

The transfer function of the UIM driver from input to current output was measured and compared to the Altium simulation for both the low noise and high dynamic range modes of operation. The testing

confirmed that measured response and simulated response were very similar for both modes. The only difference noted was at 0.1Hz, but further investigation revealed that it was most probably due to measurement error.

4.1.4.2 Noise Monitor Transfer Function

The transfer function from the input of the driver to the output of the noise monitor circuit was measured in section 3.5.1 of the test plan. A plot of the expected transfer function for the design submitted is shown in the figure below.

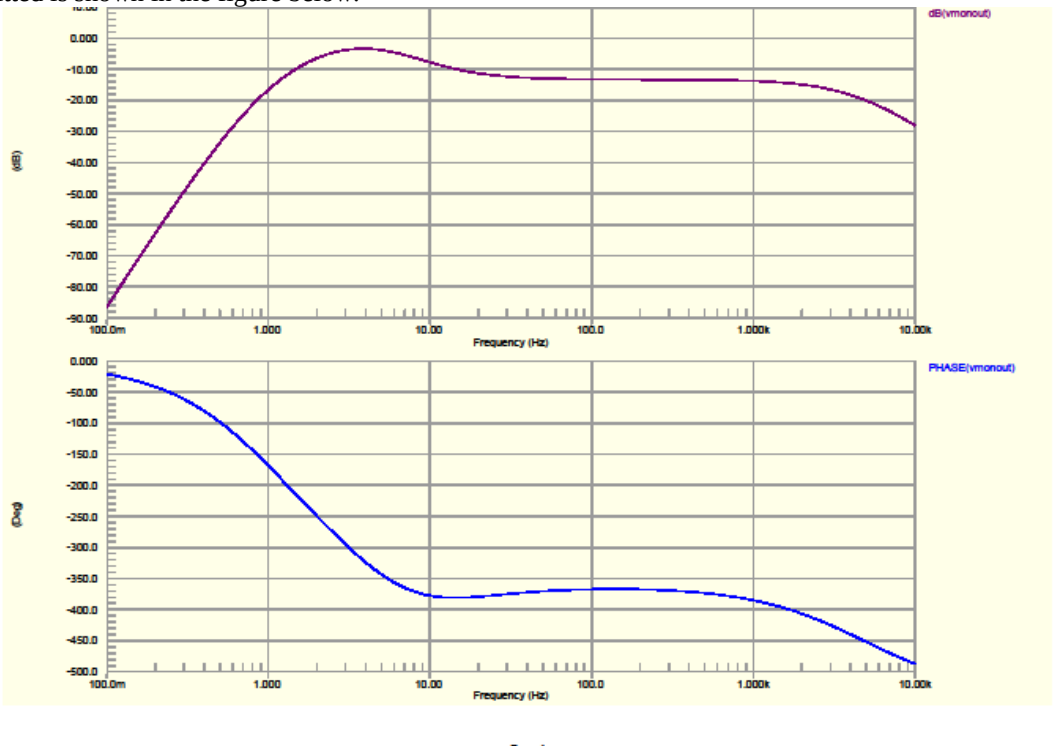

Figure 8: Noise Monitor Transfer Function, Measured from Driver Input to Monitor Output

The measured transfer functions for all four channels were found to be in close agreement with the Altium simulation, but as was previously stated in section 4.1.2 of this report, the noise monitor circuit needs to be redesigned to measure the full output noise of the driver at 10Hz. Once the circuit has been redesigned, the transfer function tests will need to be repeated.

4.2 Cross-Coupling

Cross coupling from channel to channel was measured on the original prototype chassis and found to be acceptable. Since the layout of the UIM pre-production prototype chassis has not changed significantly these tests were not repeated.

4.3 Local Damping

This section of the test plan is not applicable and can only be conducted on a full quad suspension system.

4.4 Environmental

No environmental tests were conducted during the bench testing of the pre-production prototype. Testing at LASTI should include measurements of the sensitivity of the design to external acoustic and magnetic noise. An assessment of the grounding and shielding of the system should also be made.

Appendix A

Test Plan and Results

A copy of the completed test plan for the Pre-production UIM Driver can be found at in the LIGO DCC as a related document to this report.