



LIGO Laboratory / LIGO Scientific Collaboration

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AdvLigo
Physical Environment Monitoring
Data Acquisition System Design

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1 Introduction

The purpose of this document is to describe the design of the Physical Environment Monitoring (PEM) system to be installed as part of Advanced LIGO (aLIGO) Data Acquisition (DAQ) System.

2 Scope

The scope of this document is to outline the design of the computer and supporting electronics to be provided as part of the aLIGO PEM DAQ system which meet the requirements specified in [aLIGO CDS Physical Environment Monitoring Data Acquisition Requirements](#).

This includes:

- 1) System layouts and interconnects
- 2) System Interfaces
- 3) Parts List

Specifically not in the scope of this document:

- 1) Detailed PEM sensor wiring diagrams (to be developed as separate documentation).
- 2) Software designs (separate, TBD documentation)

3 Overview

For aLIGO, the computer and I/O system for the acquisition of PEM sensor data is to be replaced with an upgraded system, consistent with the standard aLIGO Control and Data System (CDS) design. This is limited in scope to those sensors which are acquired in LIGO as fast channels (256 to 16384 samples/sec) by the present Analog Data Collection Units (ADCU).

This primarily involves the replacement of initial LIGO Versa Modular Eurocard (VME) equipment with:

- 1) New server class computers to replace VME processors.
- 2) New PCI Express (PCIe) Analog to Digital Convertors (ADC) and Digital to Analog Convertor (DAC) modules.
- 3) Replacement of Anti-Aliasing (AA) and Anti-Imaging (AI) conditioning electronics.
- 4) Replacement of sensor cabling, as necessary, to interface to the new electronics.

It is presently not planned to add new PEM sensors as part of the aLIGO upgrade, but a number of spare channels are provided in the design for later additions.

The initial LIGO PEM DAQ system provided solely for the acquisition of PEM sensor signals. For aLIGO, it is also required to provide computing capabilities to perform adaptive filtering and feed forward control. Therefore, the aLIGO design provides an additional interface into the CDS real-time control networks.

4 Design

The following figure provides an overview of the equipment and interconnections to be provided for the PEM DAQ system for a single interferometer (IFO). In addition, for LHO, equipment will also be provided at the mid stations (not shown in figure 1, see section 4.5).

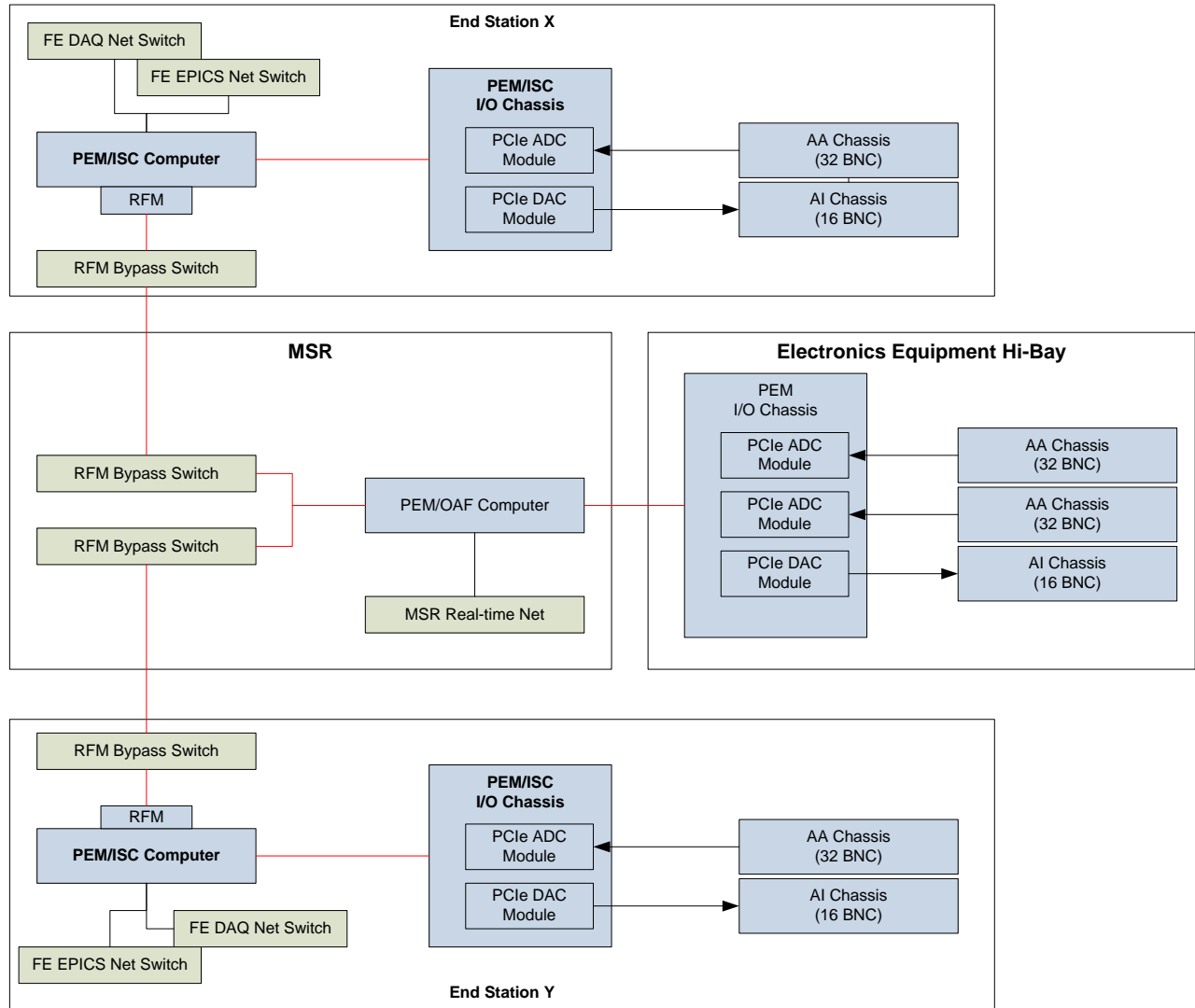


Figure 1: PEM DAQ Architecture

4.1 Common Components

The PEM DAQ system will employ a number of standard components from the aLIGO CDS design (see [aLIGO CDS Design Overview](#))

4.1.1 Computers

CDS standard computers are to be provided at each end station. These computers include:

- 1) Dual, quad core x86 processors with 3.0GHz clock
- 2) 8 GigaByte RAM
- 3) 73GByte hard disk
- 4) 3 PCIe expansion slots (2 full height/1 half height)
- 5) 2 Gigabit Ethernet ports

Central computers, for adaptive filtering and feed forward control, are TBD, awaiting compute requirements.

4.1.2 Remote PCIe I/O chassis

A CDS standard PCIe expansion chassis will be provided at each end station and at the corner station. Design details are included in [aLIGO I/O Chassis Design](#).

4.1.3 16bit ADC/DAC modules

CDS standard 16 bit [ADC/DAC](#) modules are provided for installation into the I/O chassis.

4.1.4 AA/AI chassis

CDS standard AA/AI chassis will be provided. These chassis provide isolated BNC connections for sensors/actuators and include [AA/AI filter boards](#).

4.2 Interfaces

4.2.1 Sensor connections

One, or more, AA chassis will be provided at each location for connection of PEM sensors. These chassis are equipped with 32 isolated BNC connectors.

4.2.2 Actuator Connections

A single AI chassis will be provided at each location for the connection of analog output drive signals, for test or other purposes (such as photon calibrators). These AI chassis provide 8 isolated BNC connections.

4.2.3 CDS Networks

The PEM DAQ computers are configured with the following Network Interface Cards (NIC):

- 1) Internal 1GigE network interface (connection to Front End (FE) EPICS network).
- 2) Internal 1GigE network interface (connection to FE DAQ network) to send data to DAQ system.
- 3) PCIe Reflected Memory (RFM), at end station location or PCIe to PCIe network interface, at the corner stations, to communicate real-time data (to support adaptive filtering and feed forward control).

4.3 End Stations

At the end stations, PEM is designed to share a computer and I/O chassis with the Instrument Sensing and Control (ISC) system. The equipment layout, with only PEM I/O shown, is presented in the following figure.

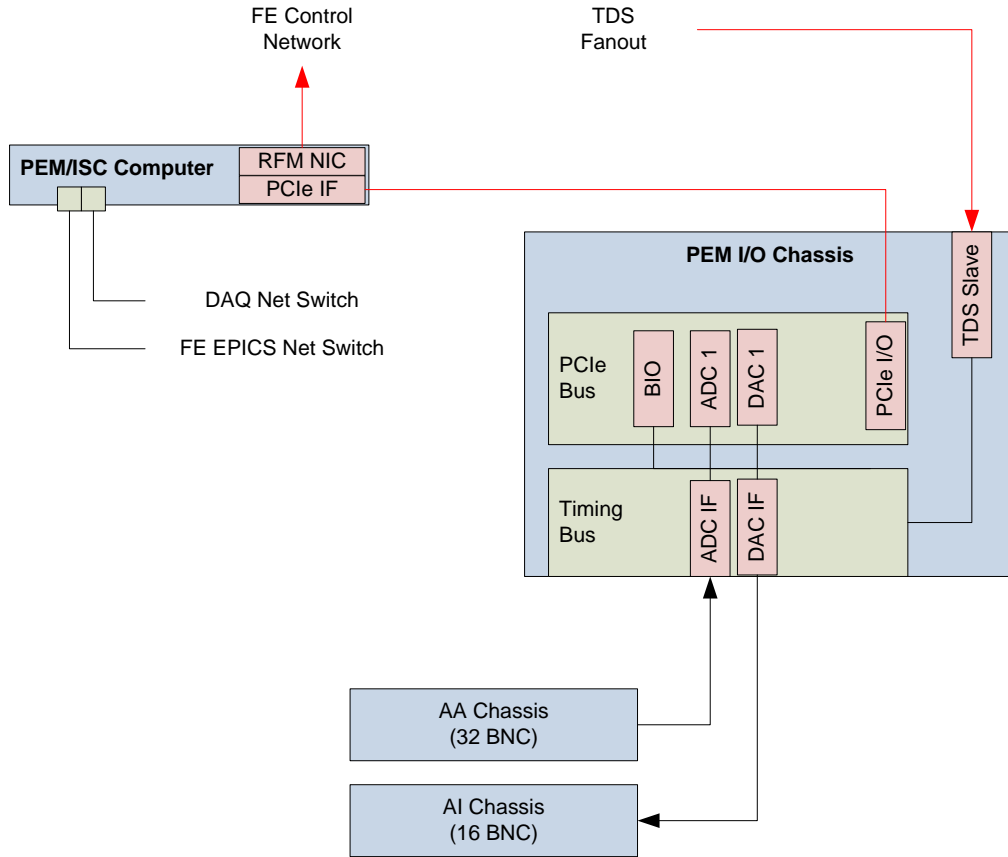


Figure 2: End Station PEM Detail

4.4 Corner Station

At the corner station, the PEM is equipped with its own computer and I/O chassis, as shown in the following diagram.

Beyond the task of providing for data acquisition for PEM sensors, this computer is intended for use in adaptive filtering and feed forward control. Given that the compute requirements are not yet well defined, it is intended to provide Sun 4600 computers (from the ELIGO installation) for the first article.

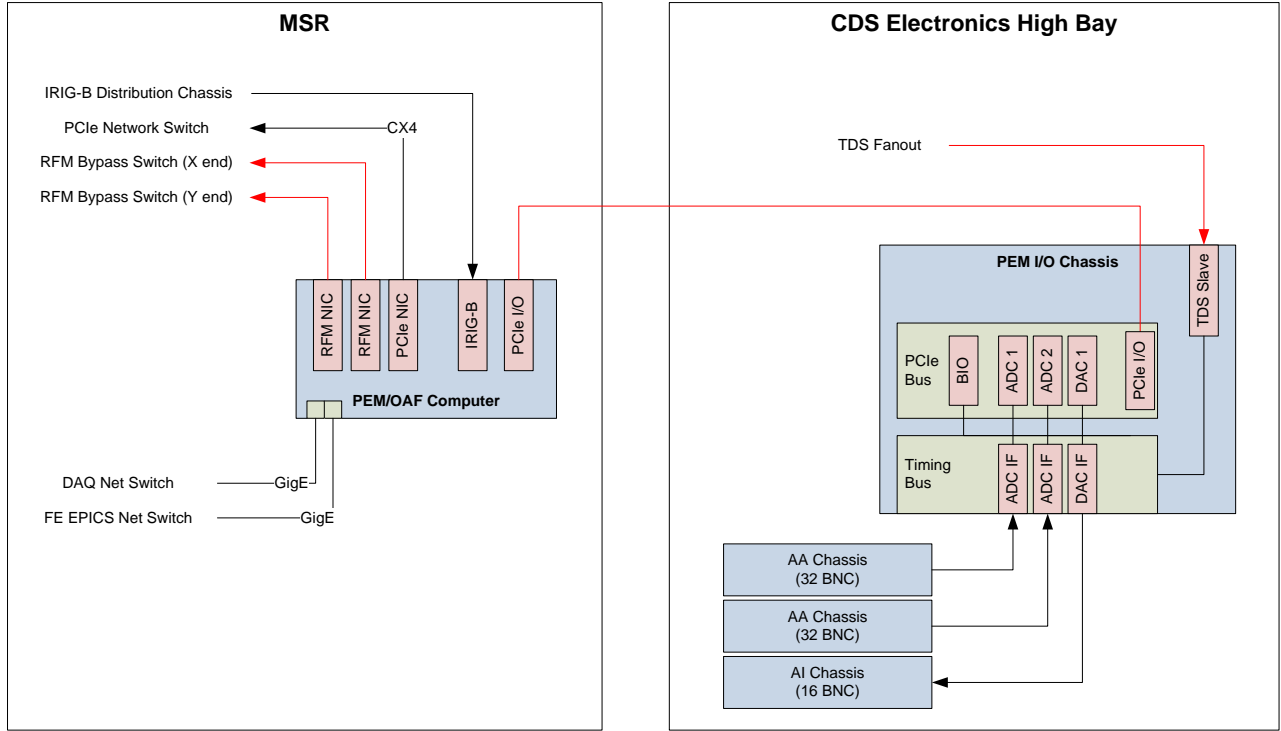


Figure 3: Corner Station PEM Detail

4.5 Mid Stations (LHO Only)

For the LHO site, it is still required to acquire a few seismometer, accelerometer and microphone signals. The PEM DAQ equipment layout is shown in the following figure.

The computer is connected, via Ethernet, to the DAQ and FE EPICS network switches. Since there is no requirement for use of these signals in adaptive filtering, no real-time control network connections are provided.

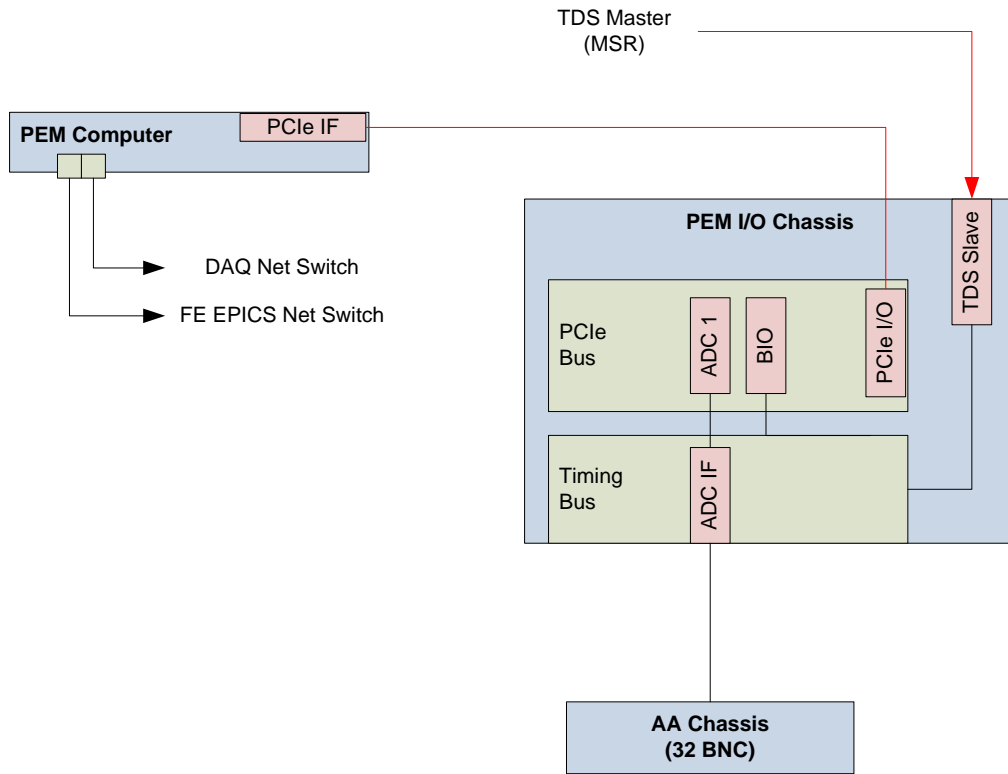


Figure 4: LHO Mid-Station PEM Detail

5 Equipment List

The following table provides a list of equipment provided for the aLIGO PEM DAQ system. Note that for the LHO mid stations, the plan is to reuse the I/O chassis from ELIGO and simply add an AA chassis and computer.

PEM Provided Equipment List				
Description	Installed		Spares	Total
	Per IFO	LHO Mid	Per Site	
Computer	3	2		11
PCIe RFM Card	4		1	14
PCIe NIC	1		1	5
PCIe expansion host adapter	3		1	11
CDS standard PCIe I/O chassis	3		1	11
PCIe ADC Module	4		1	14
PCIe DAC Module	3		1	11
PCIe Binary I/O Module	3		1	5
ADC Interface Module	4		1	14
DAC Interface Module	3		1	11
ADC to ADC Interface Card Ribbon Cable	4		1	14
Internal SCSI Cable (DAC to DAC IF Card)	3		1	11
AA Chassis	4	2	1	16
AI Chassis	3		1	11
External SCSI Cable (ADC/DAC to AA/AI)	7			21
Duplex, Multi-mode Fiber w/LC connectors	7			21
Multi-core Electrical to Fiber to Electrical Cable	3			9