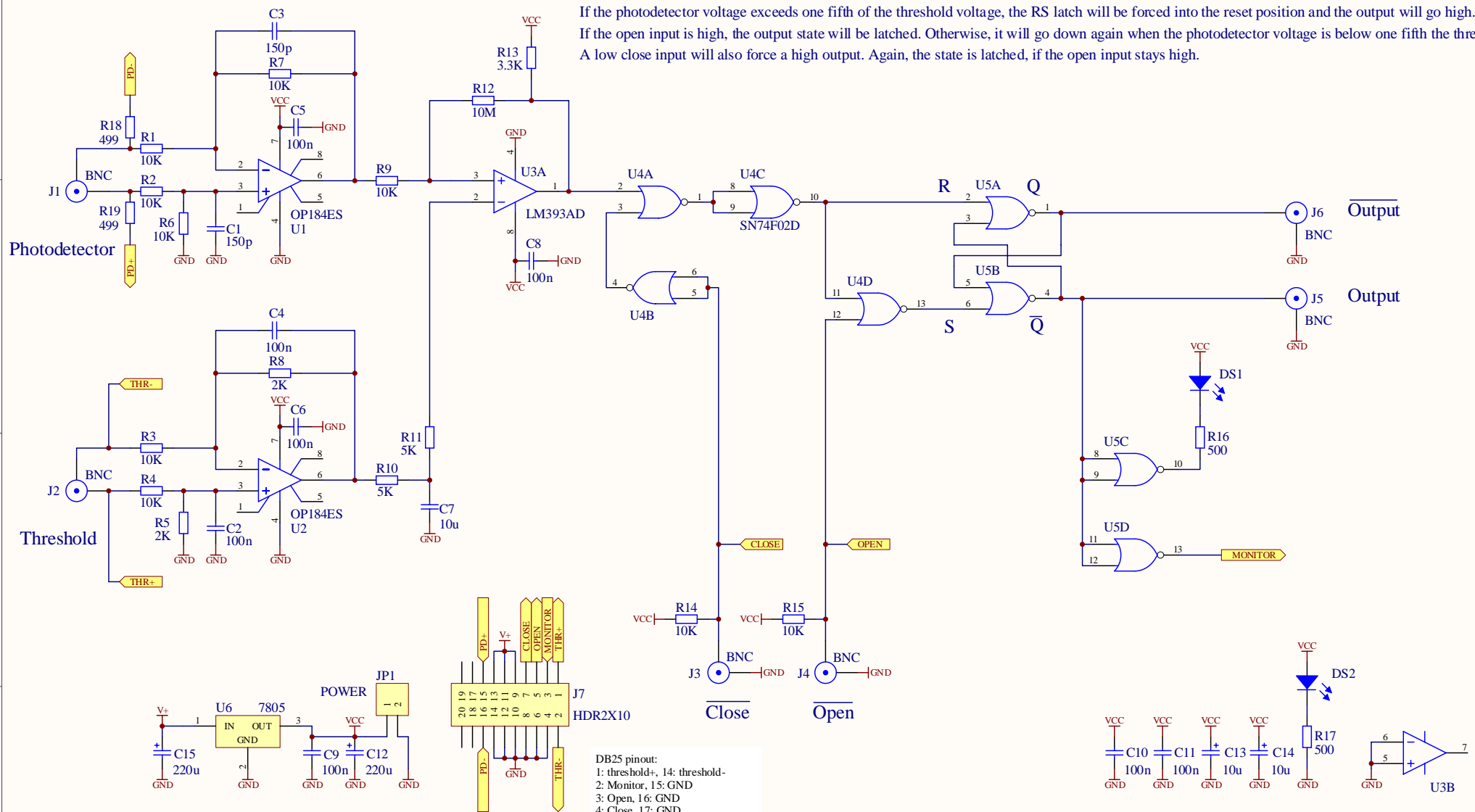


Theory of operations:

If the photodetector voltage exceeds one fifth of the threshold voltage, the RS latch will be forced into the reset position and the output will go high.
 If the open input is high, the output state will be latched. Otherwise, it will go down again when the photodetector voltage is below one fifth the threshold.
 A low close input will also force a high output. Again, the state is latched, if the open input stays high.



Comments:

Use TTL for 74F02 and not CMOS.
 Connect GND to AC ground; Drive 'close' and 'open' through opto-isolated open collector stages; Sense 'monitor' through an opto-isolator; isolate photodetector from table.

DB25 pinout:
 1: threshold+, 14: threshold-
 2: Monitor, 15: GND
 3: Open, 16: GND
 4: Close, 17: GND
 5, 6, 7: V+, 18, 19, 20: GND

Title		
Shutter Logic		
Size B	Number	Revision
	D040100-A	A
Date:	4/28/2004	Sheet 1 of 1
File:	C:\User\...\ShutterLogicSheet1.SchDoc	Drawn By: Daniel Sigg