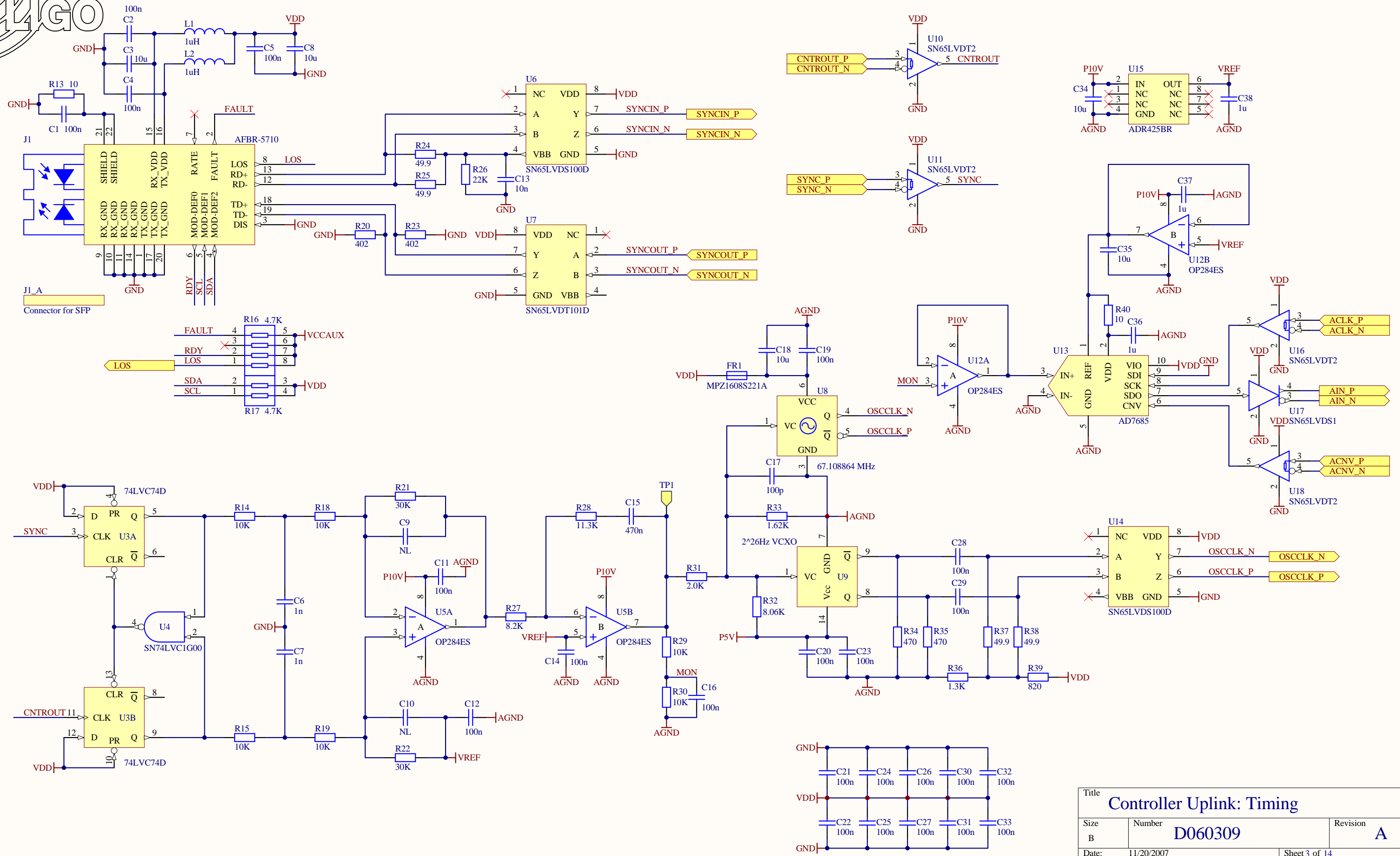
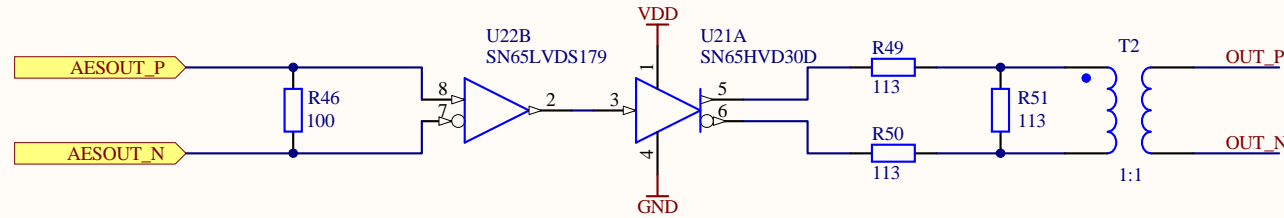
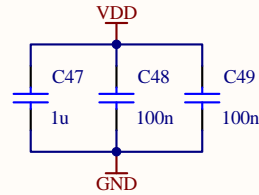
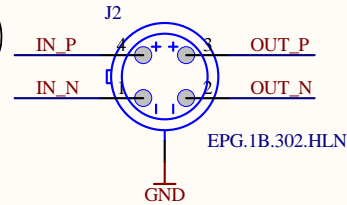


Title		Controller Uplink: Top	
Size	Number	D060309	
	Revision	A	
Date:	11/20/2007	Sheet 1 of 14	Drawn By: Daniel Stigg
File:	C:\User\SAU\Uplink1.SchDoc		

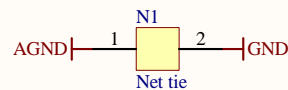
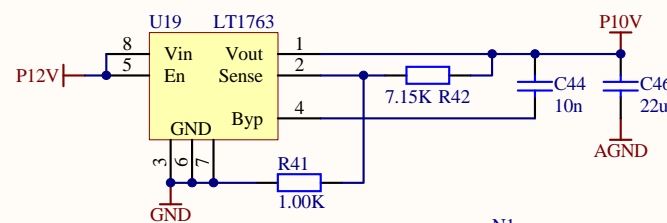
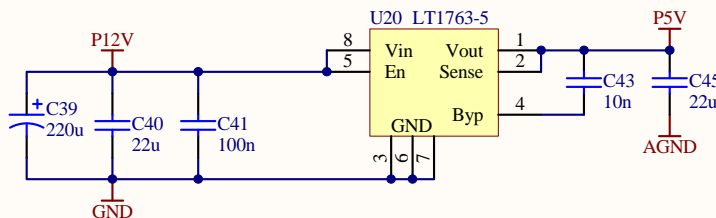
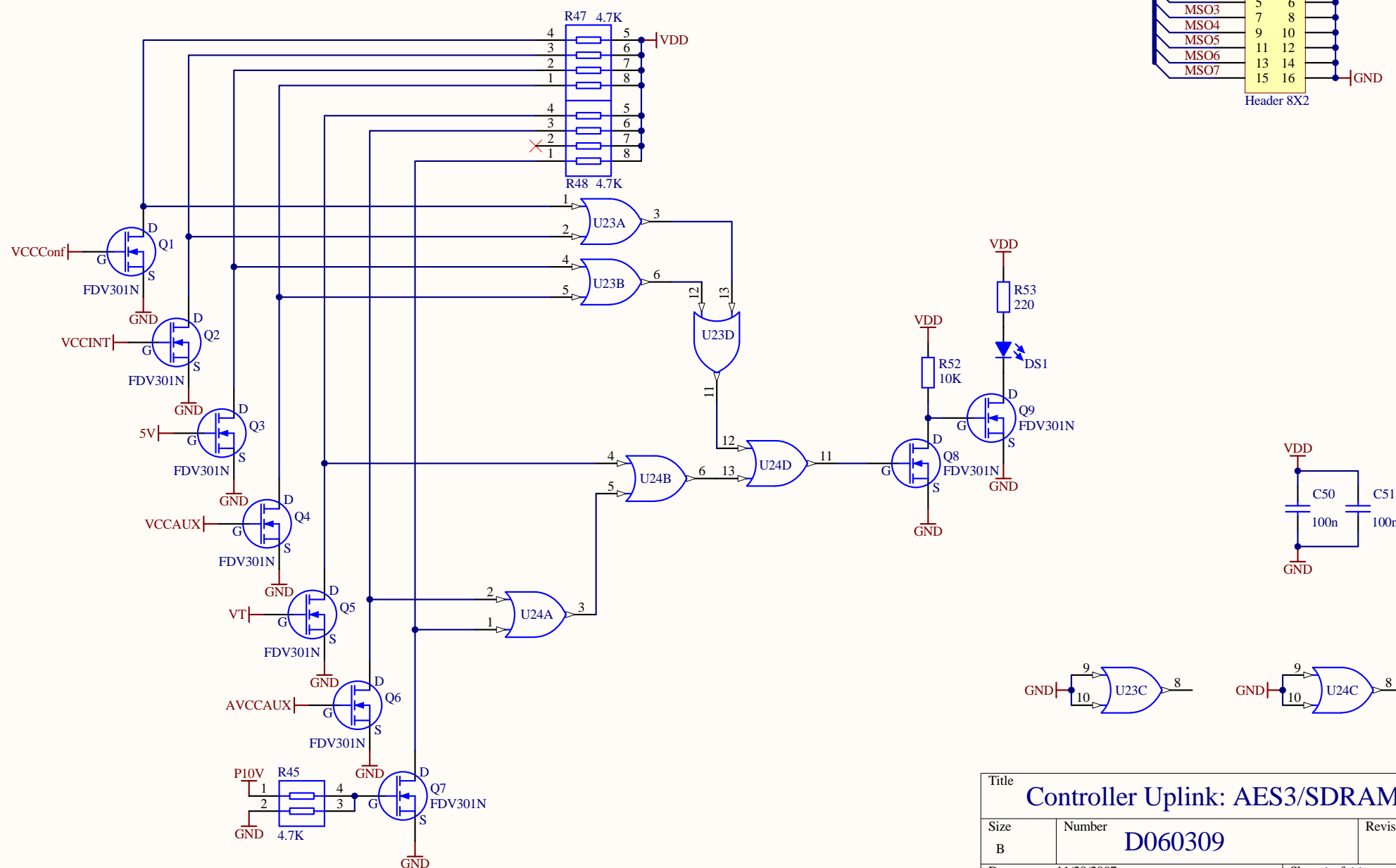
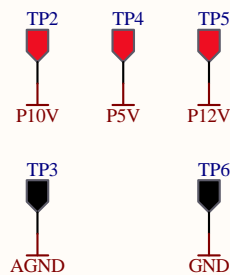
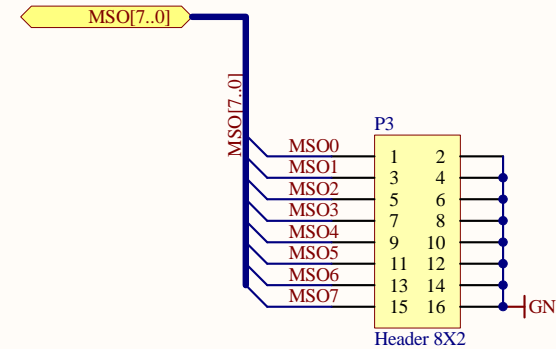
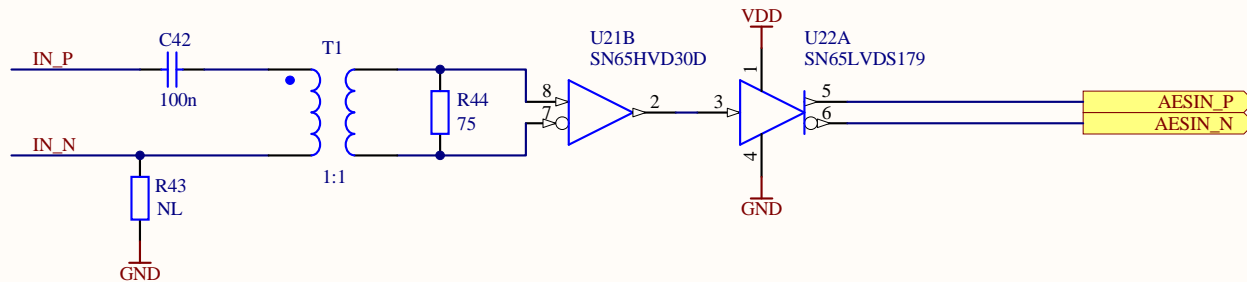


Title		
Controller Uplink: Timing		
Size	Number	Revision
B	D060309	A
Date:	11/20/2007	Sheet 3 of 14
File:	C:\User\...\SAUplink2.SchDoc	Drawn By: Daniel Sigg

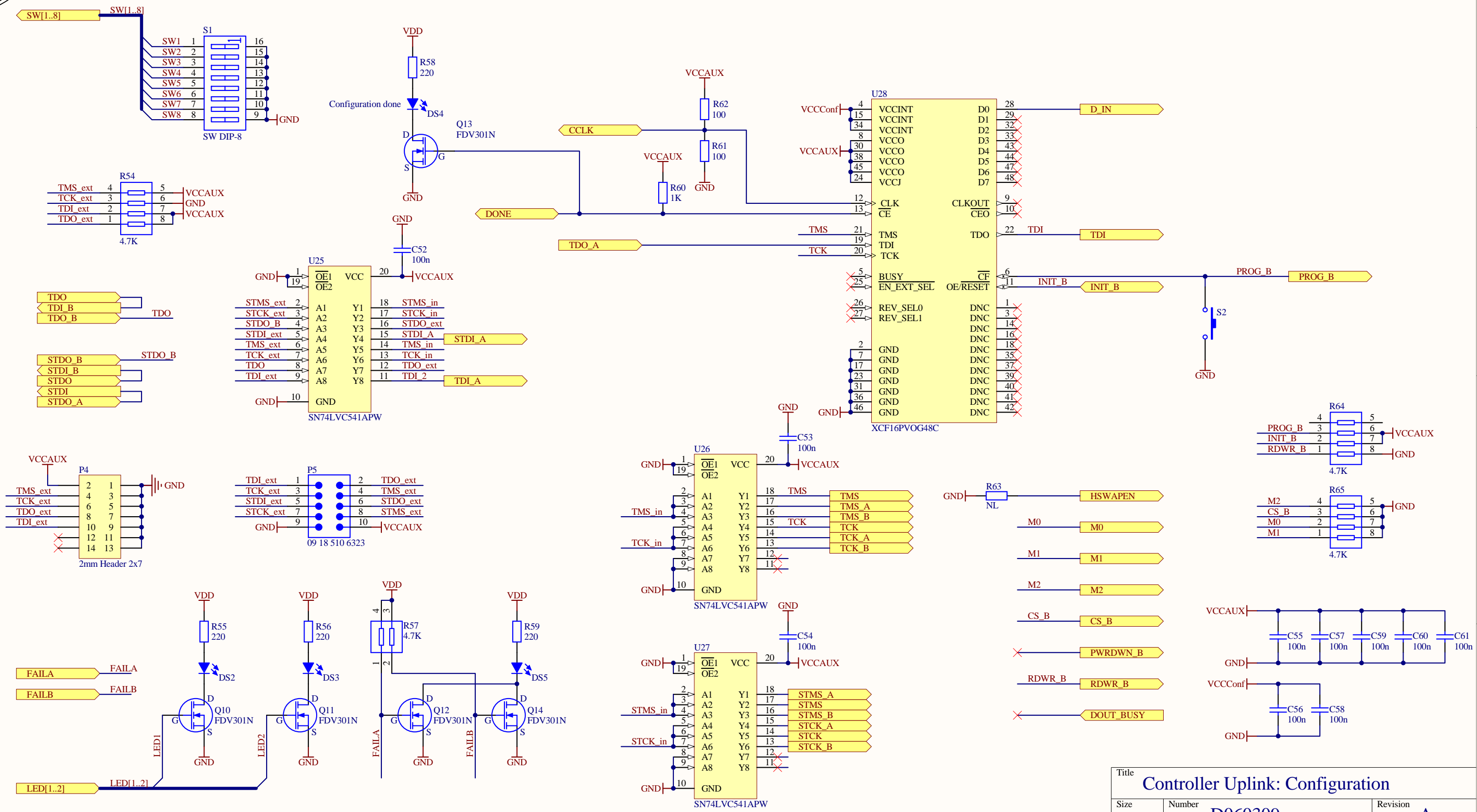
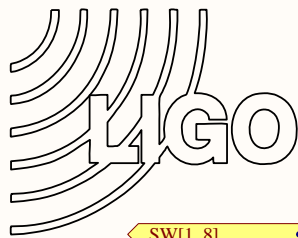


AES/BEU Output

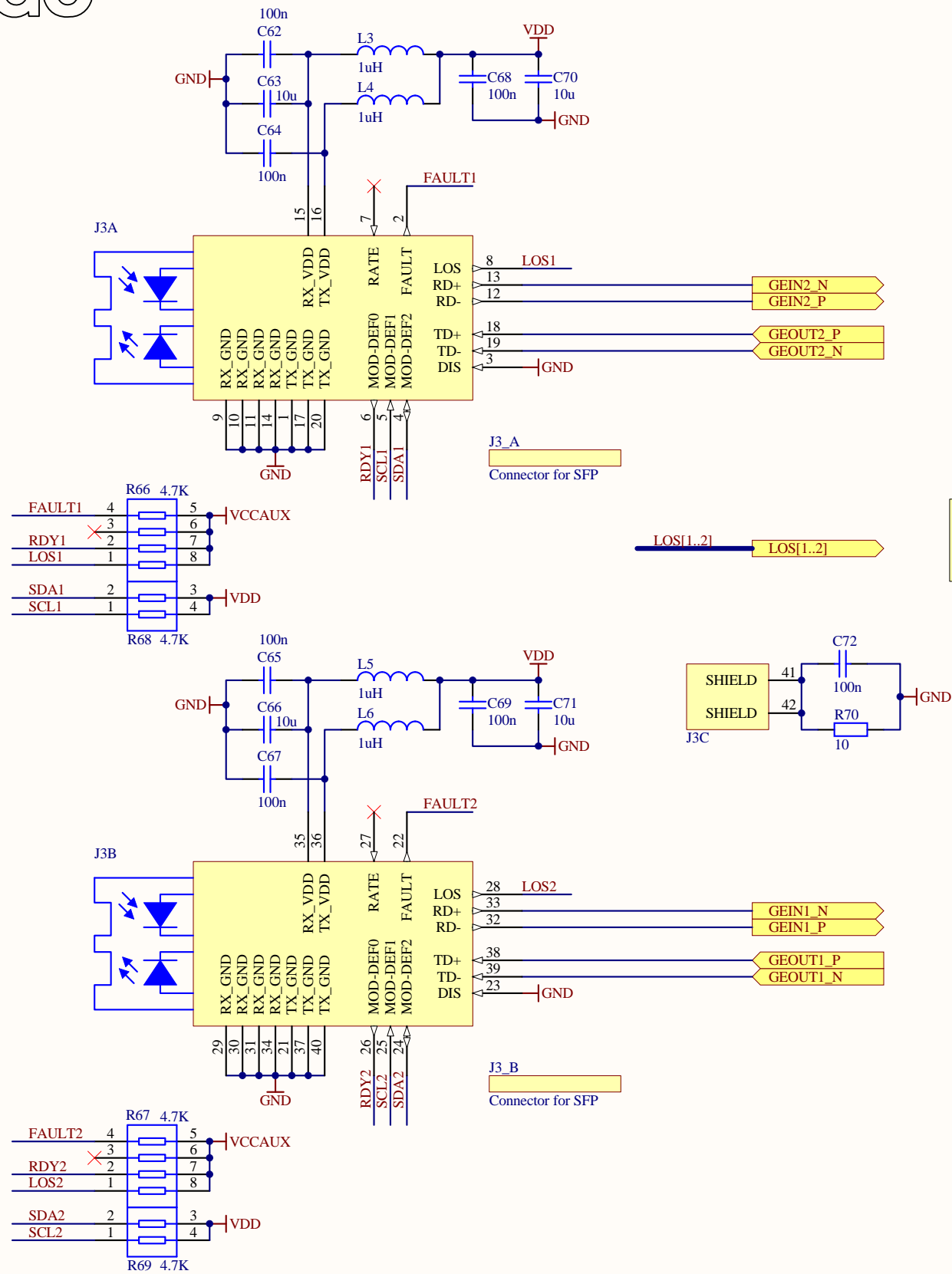
AES/BEU Input



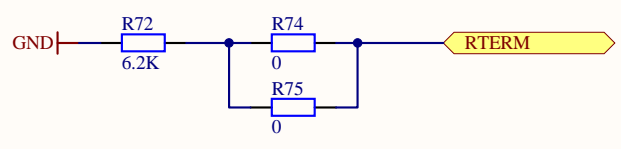
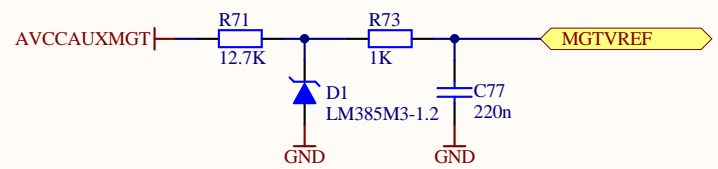
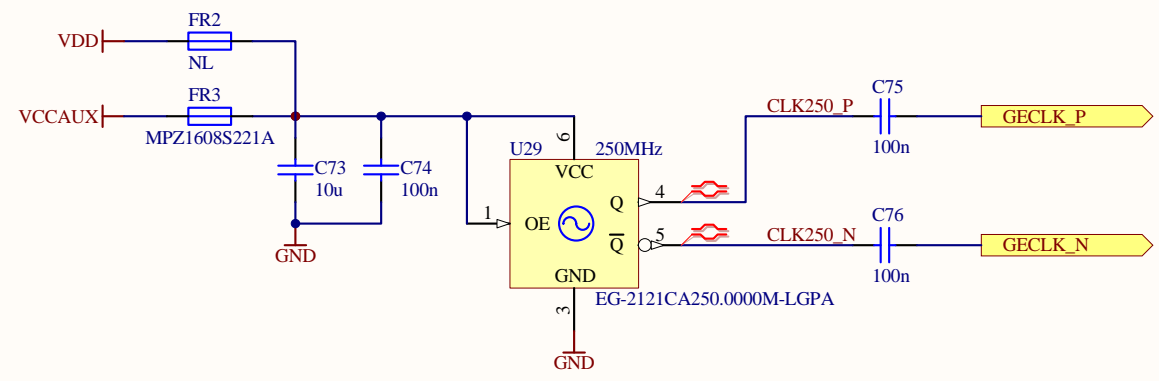
Title		
Controller Uplink: AES3/SDRAM		
Size	Number	Revision
B	D060309	A
Date:	11/20/2007	Sheet 4 of 14
File:	C:\User\...\SAUplink3.SchDoc	Drawn By: Daniel Sigg



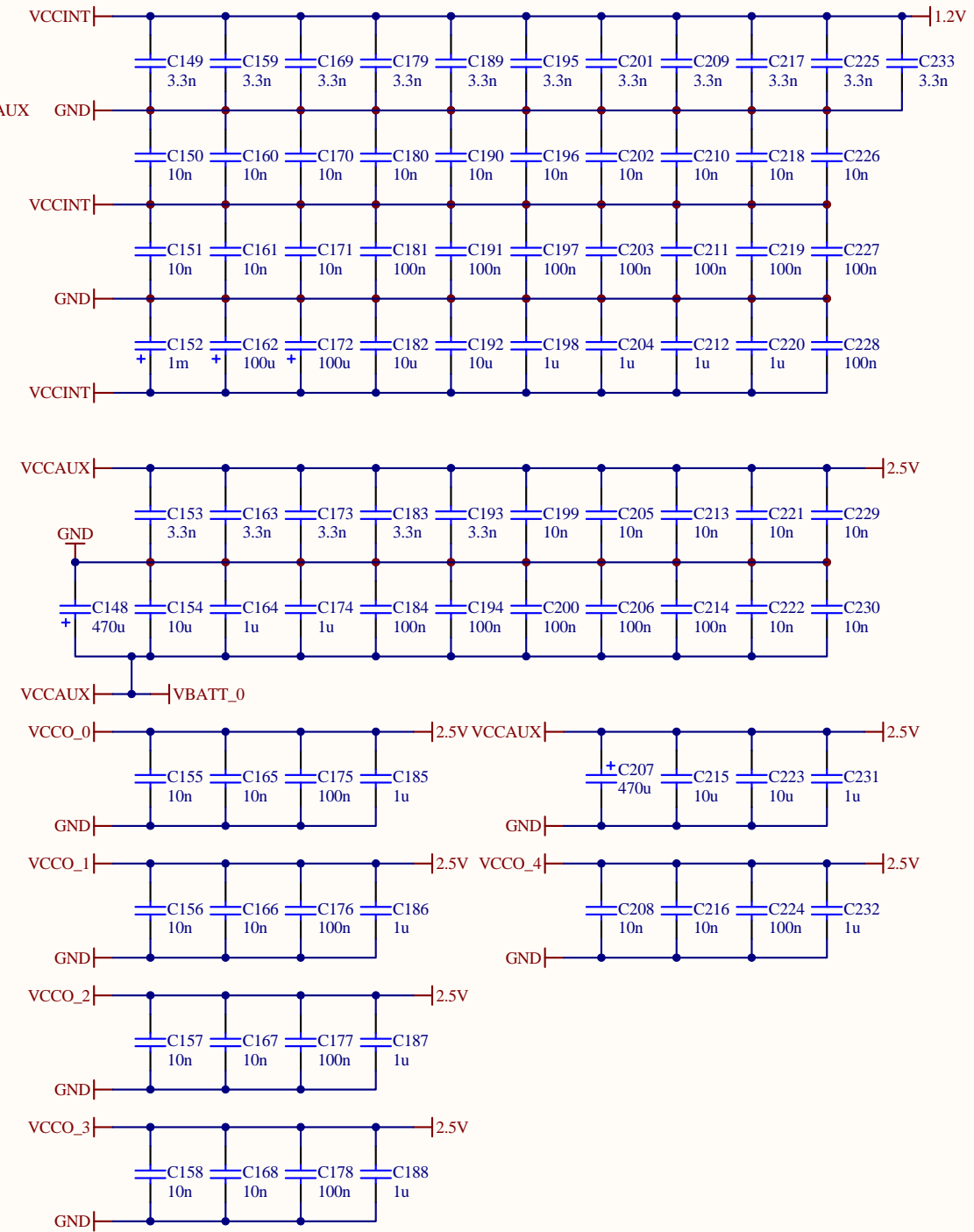
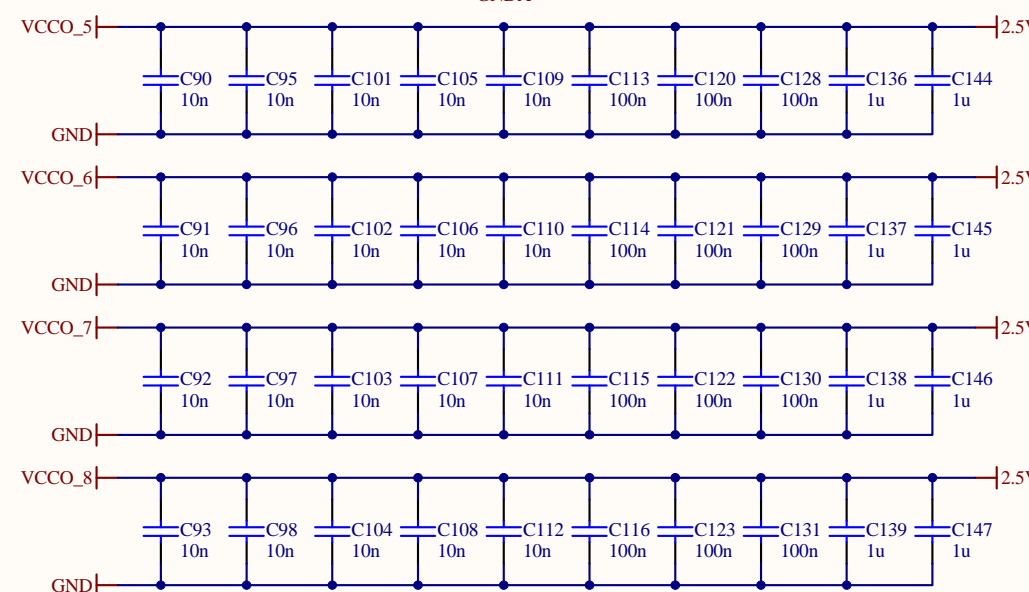
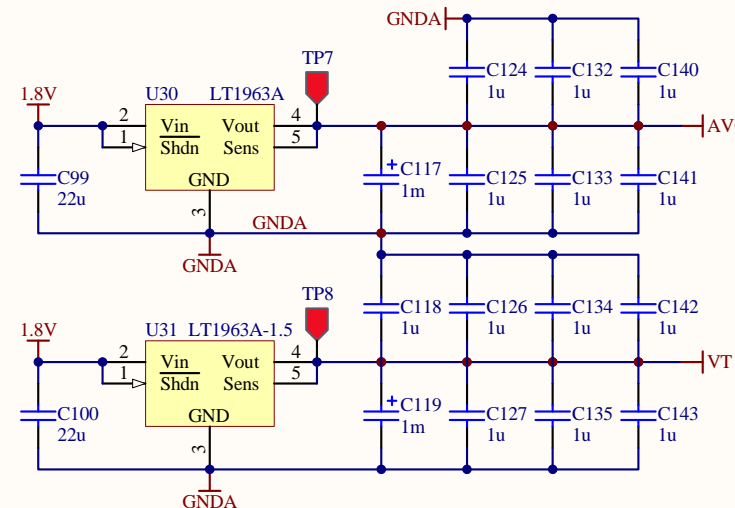
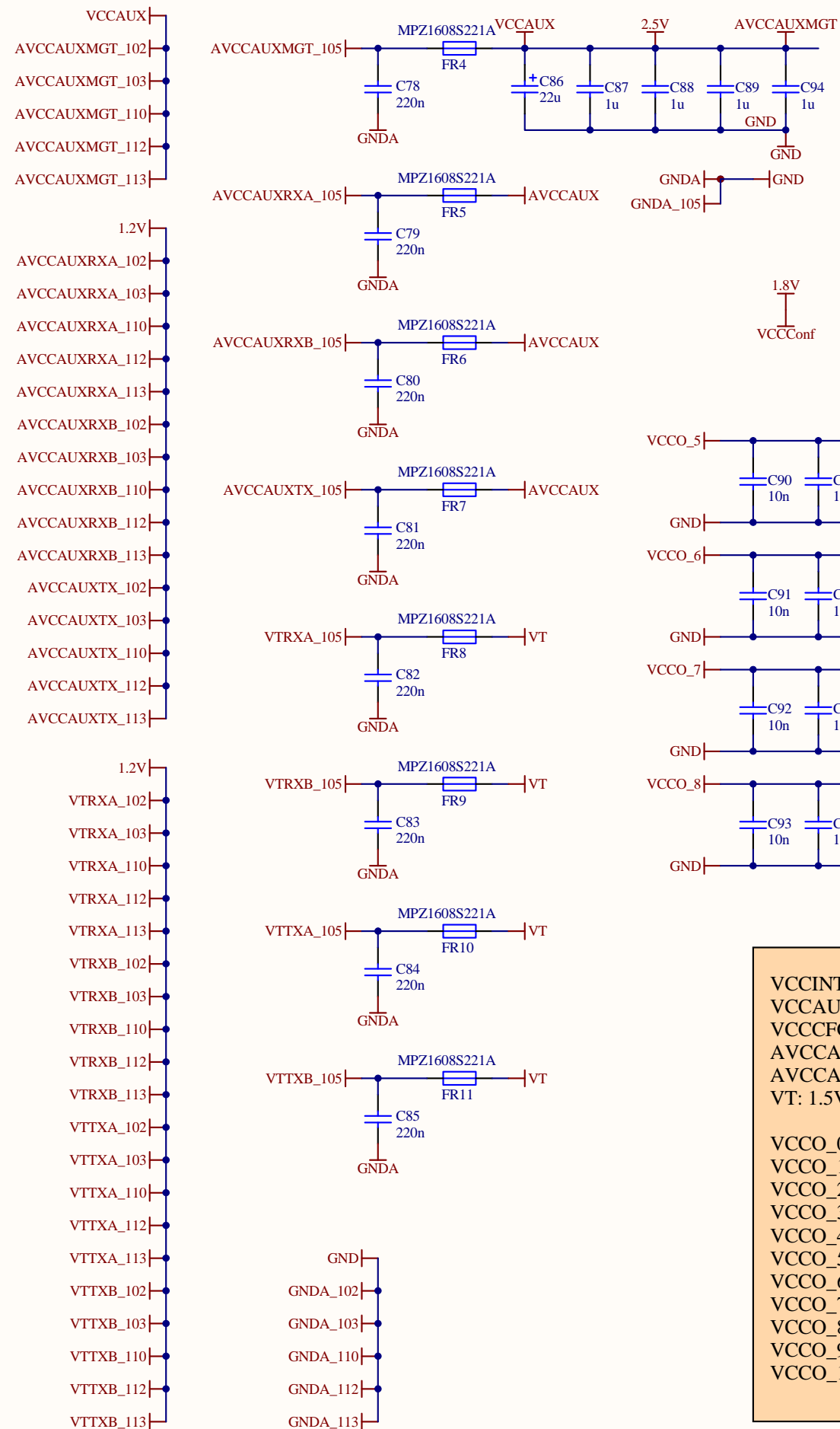
Title Controller Uplink: Configuration		
Size B	Number D060309	Revision A
Date: 11/20/2007	Sheet 5 of 14	
File: C:\User\...\SAUplink4.SchDoc	Drawn By: Daniel Sigg	



Receiver pins have reverse polarity



Title Controller Uplink: Gigabit Links		
Size B	Number D060309	Revision A
Date: 11/20/2007	Sheet 6 of 14	
File: C:\User\...\SAUplink5.SchDoc	Drawn By: Daniel Sigg	

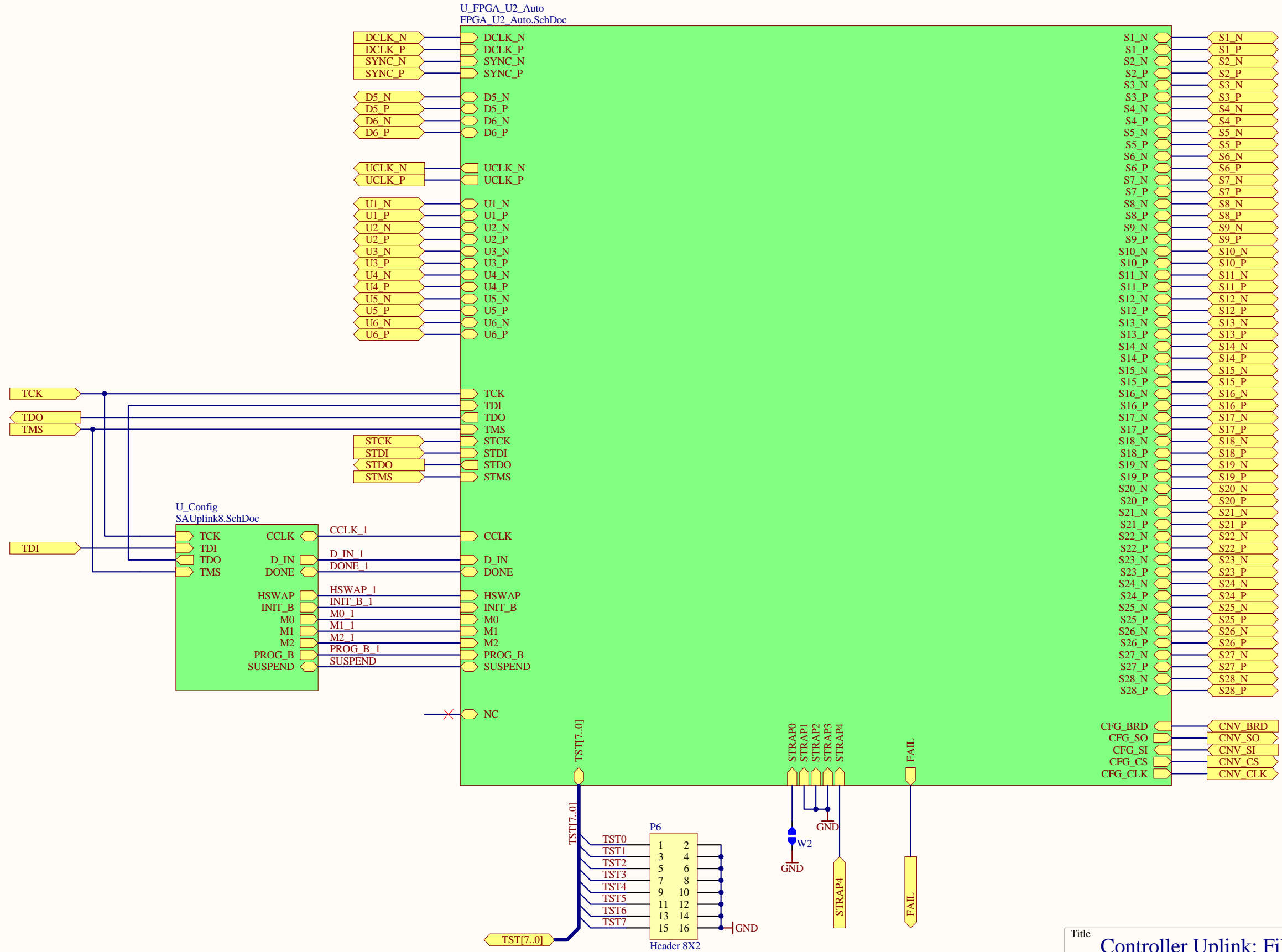
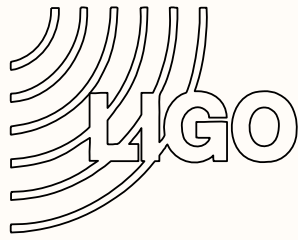


VCCINT: 1.2V main FPGA supply
VCCAUX: 2.5V auxiliary FPGS supply
VCCCFG: 1.8V platform FLASH PROM
AVCCAUX: 1.2V Rocket IO main supply
AVCCAUXMGT: 2.5V Rocket IO management supply
VT: 1.5V Rocket IO termination voltage

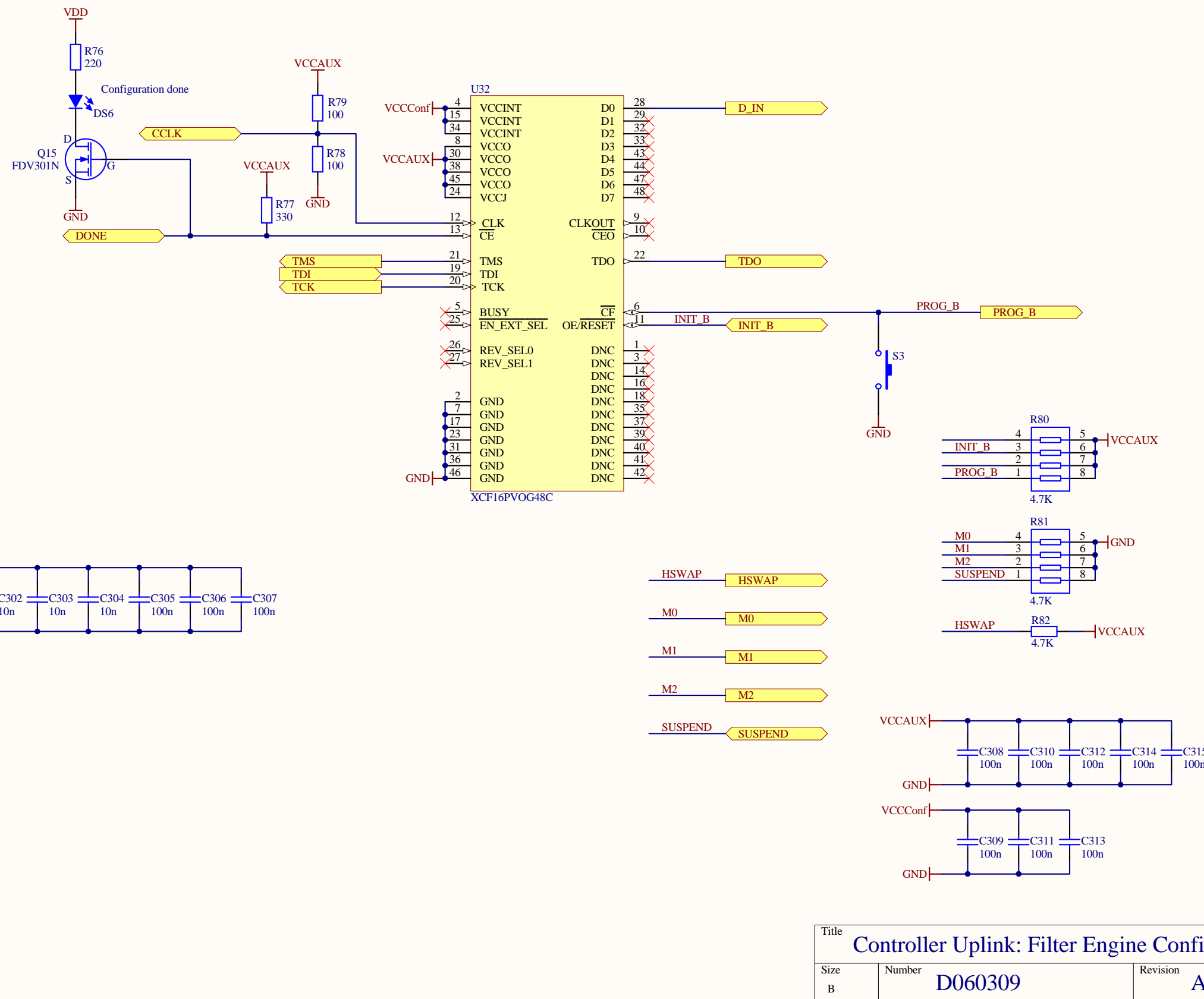
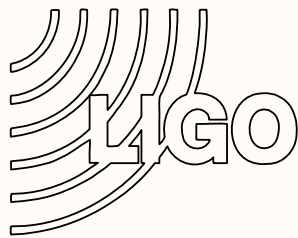
VCCO_0: 2.5V FPGA Bank 0 supply
VCCO_1: 2.5V FPGA Bank 1 supply
VCCO_2: 2.5V FPGA Bank 2 supply
VCCO_3: 2.5V FPGA Bank 3 supply
VCCO_4: 2.5V FPGA Bank 4 supply
VCCO_5: 2.5V FPGA Bank 5 supply
VCCO_6: 2.5V FPGA Bank 6 supply
VCCO_7: 2.5V FPGA Bank 7 supply
VCCO_8: 2.5V FPGA Bank 8 supply
VCCO_9: 2.5V FPGA Bank 9 supply
VCCO_10: 2.5V FPGA Bank 10 supply



Title Controller Uplink: FPGA Power		
Size B	Number D060309	Revision A
Date: 11/20/2007	Sheet 7 of 14	
File: C:\User\...\SAUplink6.SchDoc	Drawn By: Daniel Sigg	



Title		
Controller Uplink: Filter Engine		
Size	Number	Revision
B	D060309	A
Date:	11/20/2007	Sheet 8 of 14
File:	C:\User\...\SAUplink7.SchDoc	Drawn By: Daniel Sigg



Title		
Controller Uplink: Filter Engine Configuration		
Size	Number	Revision
B	D060309	A
Date:	11/20/2007	Sheet 9 of 14
File:	C:\User\...\SAUplink8.SchDoc	Drawn By: Daniel Sigg



CCLK	CCLK	S27_N	S27_N
CFG BRD	CFG_BRD	S27_P	S27_P
CFG_CLK	CFG_CLK	S28_N	S28_N
CFG_CS	CFG_CS	S28_P	S28_P
CFG_SI	CFG_SI	S3_N	S3_N
CFG_SO	CFG_SO	S3_P	S3_P
D_IN	D_IN	S4_N	S4_N
D5_N	D5_N	S4_P	S4_P
D5_P	D5_P	S5_N	S5_N
D6_N	D6_N	S5_P	S5_P
D6_P	D6_P	S6_N	S6_N
DCLK_N	DCLK_N	S6_P	S6_P
DCLK_P	DCLK_P	S7_N	S7_N
FAIL	FAIL	S7_P	S7_P
HSWAP	HSWAP	S8_N	S8_N
INIT_B	INIT_B	S8_P	S8_P
M0	M0	S9_N	S9_N
M1	M1	S9_P	S9_P
M2	M2	STCK	STCK
S1_N	S1_N	STDI	STDI
S1_P	S1_P	STDO	STDO
S10_N	S10_N	STMS	STMS
S10_P	S10_P	STRAP0	STRAP0
S11_N	S11_N	STRAP1	STRAP1
S11_P	S11_P	STRAP2	STRAP2
S12_N	S12_N	STRAP3	STRAP3
S12_P	S12_P	STRAP4	STRAP4
S13_N	S13_N	SYNC_N	SYNC_N
S13_P	S13_P	SYNC_P	SYNC_P
S14_N	S14_N	TS17_0	TS17_0
S14_P	S14_P	U1_N	U1_N
S15_N	S15_N	U1_P	U1_P
S15_P	S15_P	U2_N	U2_N
S16_N	S16_N	U2_P	U2_P
S16_P	S16_P	U3_N	U3_N
S17_N	S17_N	U3_P	U3_P
S17_P	S17_P	U4_N	U4_N
S18_N	S18_N	U4_P	U4_P
S18_P	S18_P	U5_N	U5_N
S19_N	S19_N	U5_P	U5_P
S19_P	S19_P	U6_N	U6_N
S2_N	S2_N	U6_P	U6_P
S2_P	S2_P	UCLK_N	UCLK_N
S20_N	S20_N	UCLK_P	UCLK_P
S20_P	S20_P	DONE	DONE
S21_N	S21_N	PROG_B	PROG_B
S21_P	S21_P	SUSPEND	SUSPEND
S22_N	S22_N	TCK	TCK
S22_P	S22_P	TDI	TDI
S23_N	S23_N	TDO	TDO
S23_P	S23_P	TMS	TMS
S24_N	S24_N	GND	GND
S24_P	S24_P	VCCAUX	VCCAUX
S25_N	S25_N	VCCINT	VCCINT
S25_P	S25_P	VCCO_0	VCCO_0
S26_N	S26_N	VCCO_1	VCCO_1
S26_P	S26_P	VCCO_2	VCCO_2
		VCCO_3	VCCO_3

U2A

BANK 0	IO_L01N_0	F20	
	IO_L01P_0	F20	
	IO_L02N_0	F19	
	IO_L02P_0	F19	
	IO_L03N_0	F22	
	IO_L03P_0	F22	
	IO_L06N_0	F23	
	IO_L06P_0	F23	
	IO_L07N_0	F22	
	IO_L07P_0	F22	
	IO_L08N_0	F17	
	IO_L08P_0	F17	
	IO_L09N_0	F21	
	IO_L09P_0	F21	
	IO_L10N_0	F21	
	IO_L10P_0	F21	
	IO_L11N_0	F20	
	IO_L11P_0	F20	
	IO_L12N_0	F16	
	IO_L12P_0	F16	
	IO_L13N_0	F17	
	IO_L13P_0	F17	
	IO_L14N_0	F20	
	IO_L14P_0	F20	
	IO_L15N_0	F19	
	IO_L15P_0	F19	
	IO_L16N_0	F15	
	IO_L16P_0	F15	
	IO_L17N_0	F18	
	IO_L17P_0	F18	
	IO_L18N_0	F18	
	IO_L18P_0	F18	
	IO_L19N_0	F17	
	IO_L19P_0	F17	
	IO_L20N_0	F15	
	IO_L20P_0	F15	
	IO_L21N_0	F17	
	IO_L21P_0	F17	
	IO_L22N_0	F16	
	IO_L22P_0	F16	
	IO_L23N_0	F15	
	IO_L23P_0	F15	
	IO_L24N_0	F14	
	IO_L24P_0	F14	
	IO_L25N_0	F14	
	IO_L25P_0	F14	
	IO_L26N_0	F14	
	IO_L26P_0	F14	
	IO_L27N_0	F13	
	IO_L27P_0	F13	
	IO_L28N_0	F13	
	IO_L28P_0	F13	
	IO_L29N_0	F13	
	IO_L29P_0	F13	
	IO_L30N_0	F12	
	IO_L30P_0	F12	
	IO_L31N_0	F12	
	IO_L31P_0	F12	
	IO_L32N_0	F11	
	IO_L32P_0	F11	
	IO_L33N_0	F10	
	IO_L33P_0	F10	
	IO_L34N_0	F9	
	IO_L34P_0	F9	
	IO_L35N_0	F9	
	IO_L35P_0	F9	
	IO_L36N_0	F8	
	IO_L36P_0	F8	
	IO_L37N_0	F8	
	IO_L37P_0	F8	
	IO_L38N_0	F7	
	IO_L38P_0	F7	
	IO_L39N_0	F7	
	IO_L39P_0	F7	
	IO_L40N_0	F6	
	IO_L40P_0	F6	
	IO_L41N_0	F6	
	IO_L41P_0	F6	
	IO_L42N_0	F5	
	IO_L42P_0	F5	
	IO_L43N_0	F5	
	IO_L43P_0	F5	
	IO_L44N_0	F4	
	IO_L44P_0	F4	
	IO_L45N_0	F4	
	IO_L45P_0	F4	
	IO_L46N_0	F3	
	IO_L46P_0	F3	
	IO_L47N_0	F3	
	IO_L47P_0	F3	
	IO_L48N_0	F2	
	IO_L48P_0	F2	
	IO_L49N_0	F2	
	IO_L49P_0	F2	
	IO_L50N_0	F1	
	IO_L50P_0	F1	
	IO_L51N_0	F1	
	IO_L51P_0	F1	
	IO_L52N_0	F0	
	IO_L52P_0	F0	

U2B

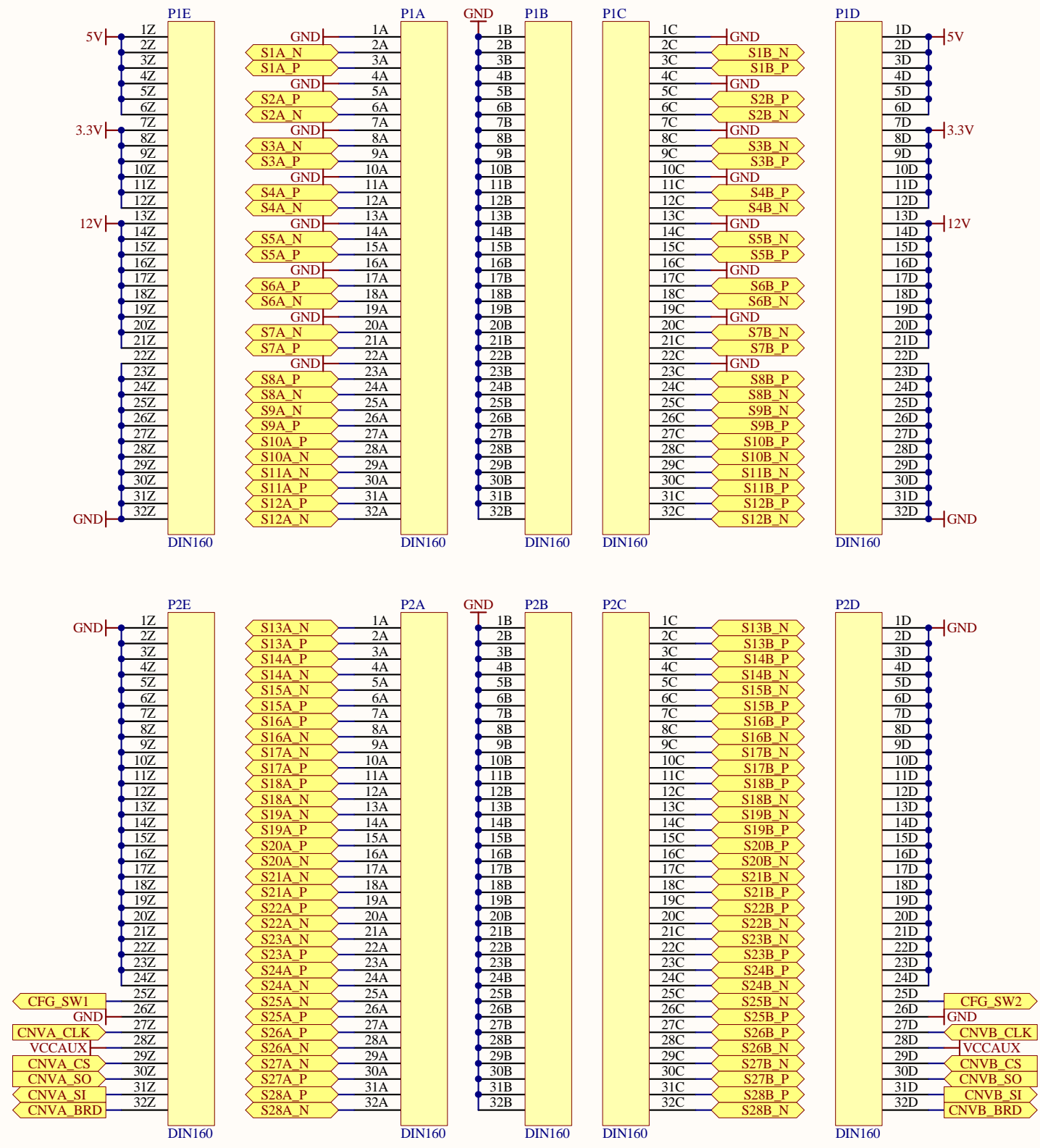
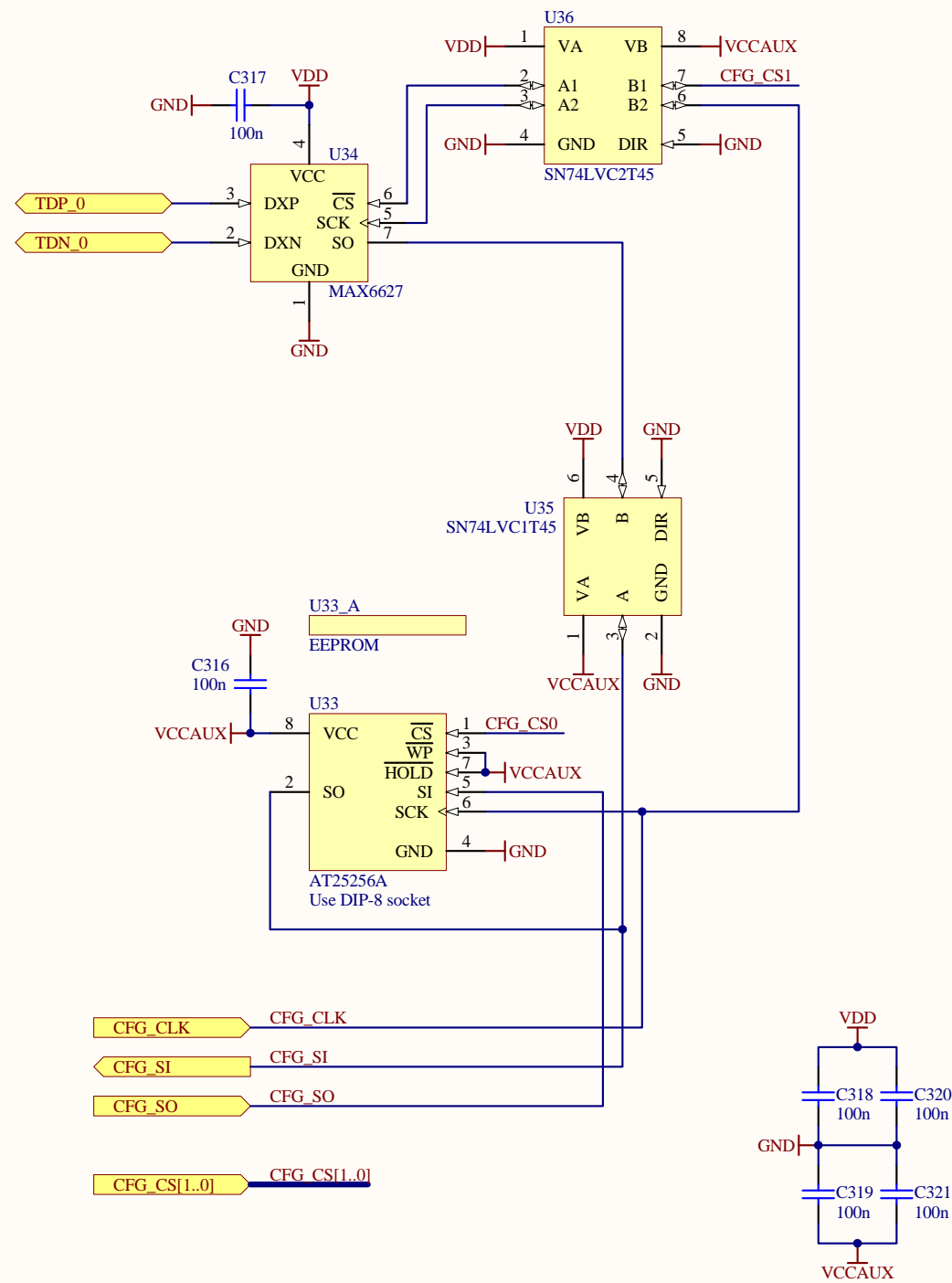
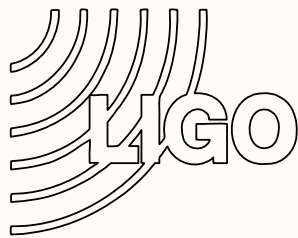
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	IO_L01P_1	F21	
	IO_L02N_1	F20	
	IO_L02P_1	F20	
	IO_L03N_1	F23	
	IO_L03P_1	F23	
	IO_L06N_1	F24	
	IO_L06P_1	F24	
	IO_L07N_1	F23	
	IO_L07P_1	F23	
	IO_L08N_1	F18	
	IO_L08P_1	F18	
	IO_L09N_1	F22	
	IO_L09P_1	F22	
	IO_L10N_1	F21	
	IO_L10P_1	F21	
	IO_L11N_1	F20	
	IO_L11P_1	F20	
	IO_L12N_1	F16	
	IO_L12P_1	F16	
	IO_L13N_1	F17	
	IO_L13P_1	F17	
	IO_L14N_1	F20	
	IO_L14P_1	F20	
	IO_L15N_1	F19	
	IO_L15P_1	F19	
	IO_L16N_1	F15	
	IO_L16P_1	F15	
	IO_L17N_1	F18	
	IO_L17P_1	F18	
	IO_L18N_1	F18	
	IO_L18P_1	F18	
	IO_L19N_1	F17	
	IO_L19P_1	F17	
	IO_L20N_1	F15	
	IO_L20P_1	F15	
	IO_L21N_1	F17	
	IO_L21P_1	F17	
	IO_L22N_1	F16	
	IO_L22P_1	F16	
	IO_L23N_1	F15	
	IO_L23P_1	F15	
	IO_L24N_1	F14	
	IO_L24P_1	F14	
	IO_L25N_1	F14	
	IO_L25P_1	F14	
	IO_L26N_1	F14	
	IO_L26P_1	F14	
	IO_L27N_1	F13	
	IO_L27P_1	F13	
	IO_L28N_1	F13	
	IO_L28P_1	F13	
	IO_L29N_1	F13	
	IO_L29P_1	F13	
	IO_L30N_1	F12	
	IO_L30P_1	F12	
	IO_L31N_1	F12	
	IO_L31P_1	F12	
	IO_L32N_1	F11	
	IO_L32P_1	F11	
	IO_L33N_1	F10	
	IO_L33P_1	F10	
	IO_L34N_1	F9	
	IO_L34P_1	F9	
	IO_L35N_1	F9	
	IO_L35P_1	F9	
	IO_L36N_1	F8	
	IO_L36P_1	F8	
	IO_L37N_1	F8	
	IO_L37P_1	F8	
	IO_L38N_1	F7	
	IO_L38P_1	F7	
	IO_L39N_1	F7	
	IO_L39P_1	F7	
	IO_L40N_1	F6	
	IO_L40P_1	F6	
	IO_L41N_1	F6	
	IO_L41P_1	F6	
	IO_L42N_1	F5	
	IO_L42P_1	F5	
	IO_L43N_1	F5	
	IO_L43P_1	F5	
	IO_L44N_1	F4	
	IO_L44P_1	F4	
	IO_L45N_1	F4	
	IO_L45P_1	F4	
	IO_L46N_1	F3	
	IO_L46P_1	F3	
	IO_L47N_1	F3	
	IO_L47P_1	F3	
	IO_L48N_1	F2	
	IO_L48P_1	F2	
	IO_L49N_1	F2	
	IO_L49P_1	F2	
	IO_L50N_1	F1	
	IO_L50P_1	F1	
	IO_L51N_1	F1	
	IO_L51P_1	F1	
	IO_L52N_1	F0	
	IO_L52P_1	F0	

U2C

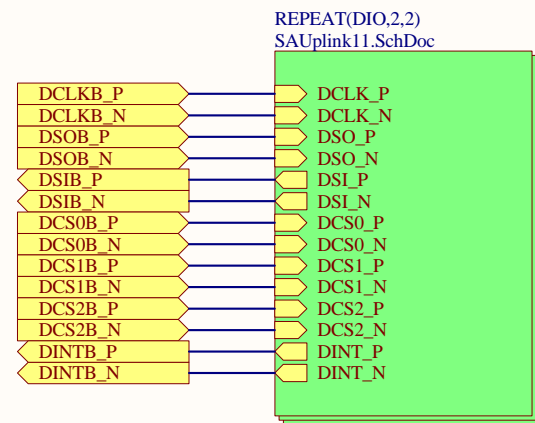
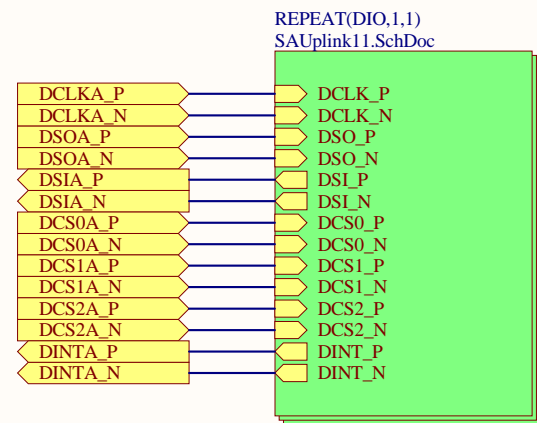
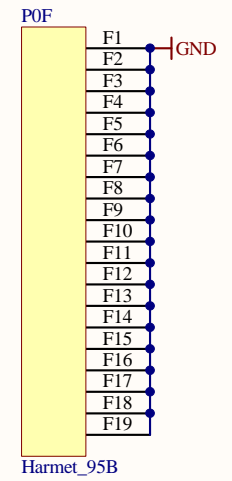
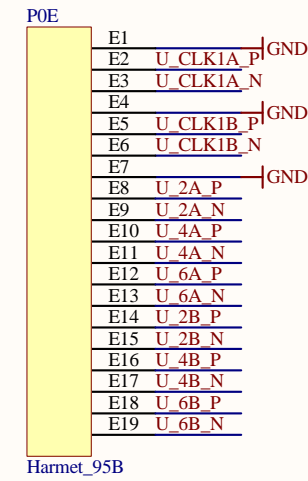
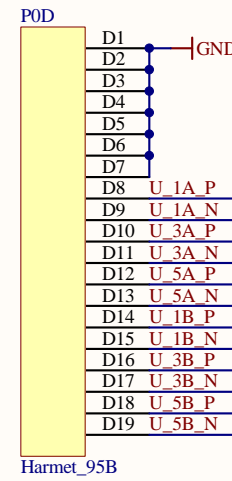
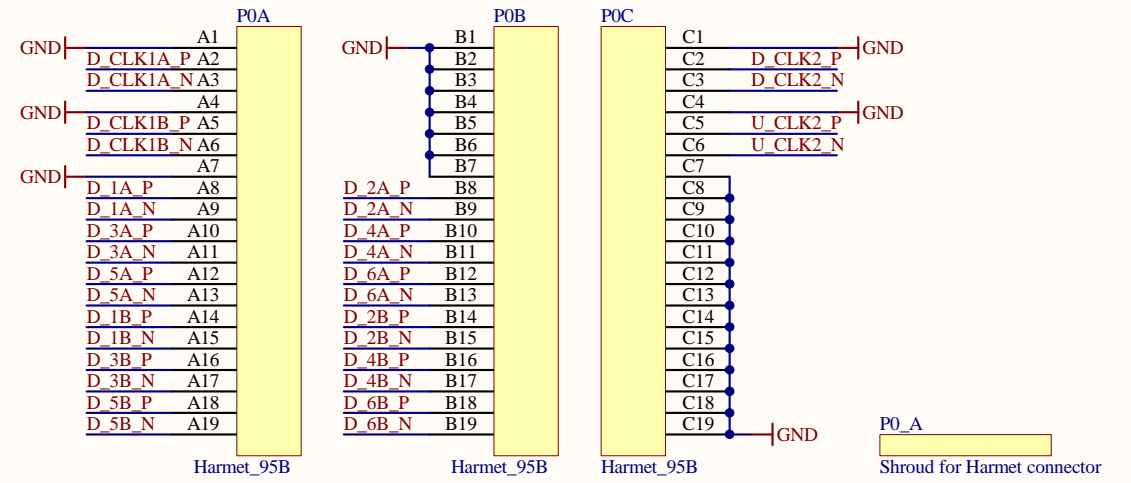
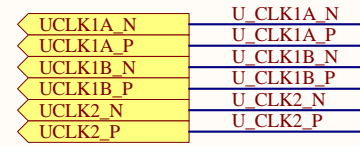
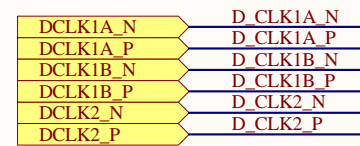
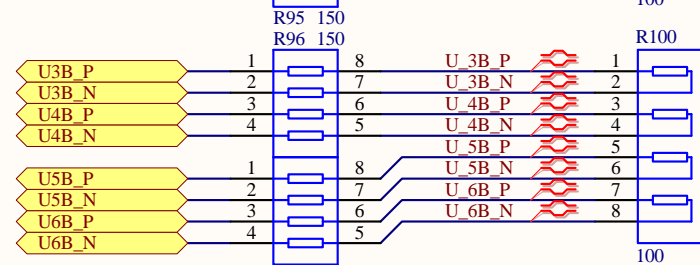
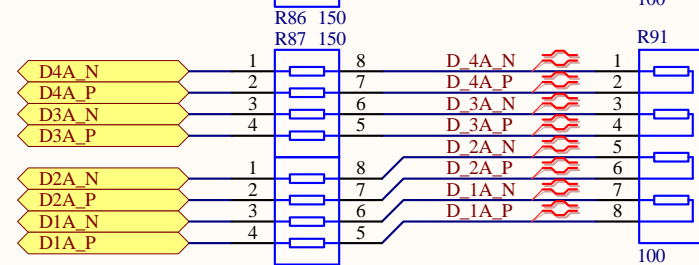
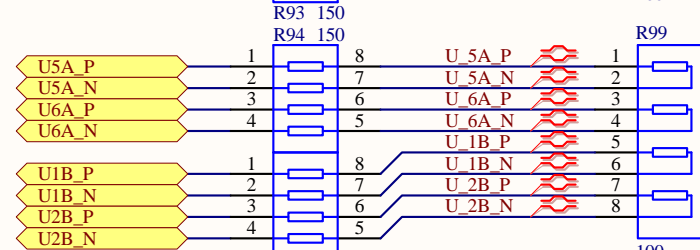
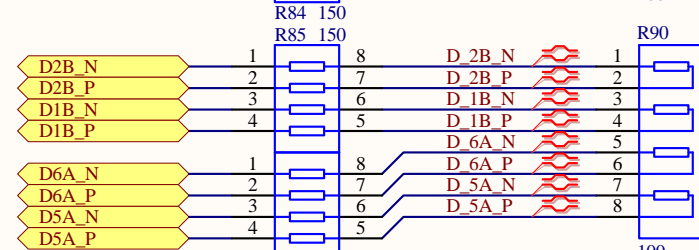
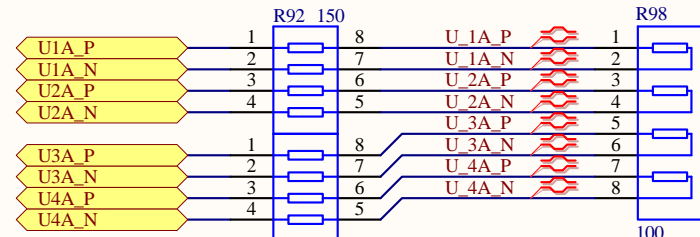
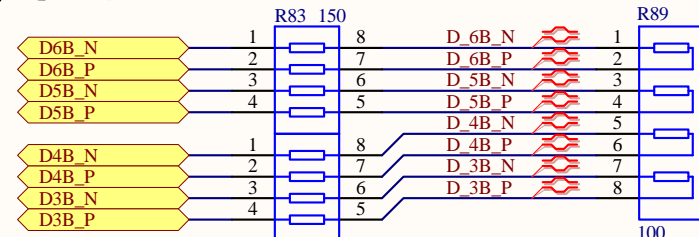
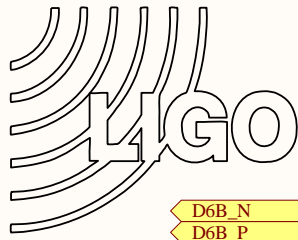
BANK 2	IO_L01N_2	F22	
	IO_L01P_2	F22	
	IO_L02N_2	F21	
	IO_L02P_2	F21	
	IO_L03N_2	F24	
	IO_L03P_2	F24	
	IO_L06N_2	F25	
	IO_L06P_2	F25	
	IO_L07N_2	F24	
	IO_L07P_2	F24	
	IO_L08N_2	F19	
	IO_L08P_2	F19	
	IO_L09N_2	F23	
	IO_L09P_2	F23	
	IO_L10N_2	F22	
	IO_L10P_2	F22	
	IO_L11N_2	F21	
	IO_L11P_2	F21	
	IO_L12N_2	F16	
	IO_L12P_2	F16	
	IO_L13N_2	F17	
	IO_L13P_2	F17	
	IO_L14N_2	F20	
	IO_L14P_2	F20	
	IO_L15N_2	F19	
	IO_L15P_2	F19	
	IO_L16N_2	F15	
	IO_L16P_2	F15	
	IO_L17N_2	F18	
	IO_L17P_2	F18	
	IO_L18N_2	F18	
	IO_L18P_2	F18	
	IO_L19N_2	F17	
	IO_L19P_2	F17	
	IO_L20N_2	F15	
	IO_L20P_2	F15	
	IO_L21N_2	F17	
	IO_L21P_2	F17	
	IO_L22N_2	F16	
	IO_L22P_2	F16	
	IO_L23N_2	F15	
	IO_L23P_2	F15	
	IO_L24N_2	F14	
	IO_L24P_2	F14	
	IO_L25N_2	F14	
	IO_L25P_2	F14	
	IO_L26N_2	F14	
	IO_L26P_2	F14	
	IO_L27N_2	F13	
	IO_L27P_2	F13	
	IO_L28N_2	F13	
	IO_L28P_2	F13	
	IO_L29N_2	F13	
	IO_L29P_2	F13	
	IO_L30N_2	F12	
	IO_L30P_2	F12	
	IO_L31N_2	F12	
	IO_L31P_2	F12	
	IO_L32N_2	F11	
	IO_L32P_2	F11	
	IO_L33N_2	F10	
	IO_L33P_2	F10	
	IO_L34N_2	F9	
	IO_L34P_2	F9	
	IO_L35N_2	F9	
	IO_L35P_2	F9	
	IO_L36N_2	F8	
	IO_L36P_2	F8	
	IO_L37N_2	F8	
	IO_L37P_2	F8	
	IO_L38N_2	F7	
	IO_L38P_2	F7	
	IO_L39N_2	F7	
	IO_L39P_2	F7	
	IO_L40N_2	F6	
	IO_L40P_2	F6	
	IO_L41N_2	F6	
	IO_L41P_2	F6	
	IO_L42N_2	F5	
	IO_L42P_2	F5	
	IO_L43N_2	F5	
	IO_L43P_2	F5	
	IO_L44N_2	F4	
	IO_L44P_2	F4	
	IO_L45N_2	F4	
	IO_L45P_2	F4	
	IO_L46N_2	F3	
	IO_L46P_2	F3	
	IO_L47N_2	F3	
	IO_L47P_2	F3	
	IO_L48N_2	F2	
	IO_L48P_2	F2	
	IO_L49N_2	F2	
	IO_L49P_2	F2	
	IO_L50N_2	F1	
	IO_L50P_2	F1	
	IO_L51N_2	F1	
	IO_L51P_2	F1	
	IO_L52N_2	F0	
	IO_L52P_2	F0	

U2D

BANK 3	IO_L01N_3	F23	
	IO_L01P_3	F23	
	IO_L02N_3	F22	
	IO_L02P_3	F22	
	IO_L03N_3	F25	
	IO_L03P_3	F25	
	IO_L06N_3	F26	
	IO_L06P_3	F26	
	IO_L07N_3	F25	
	IO_L07P_3	F25	
	IO_L08N_3	F20	
	IO_L08P_3	F20	
	IO_L09N_3	F24	
	IO_L09P_3	F24	
	IO_L10N_3	F23	

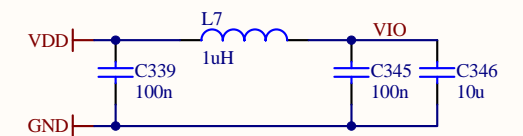
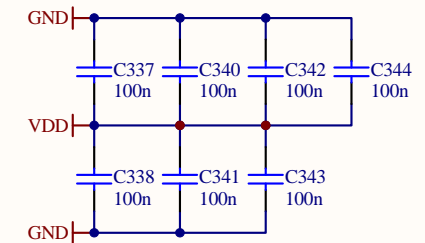
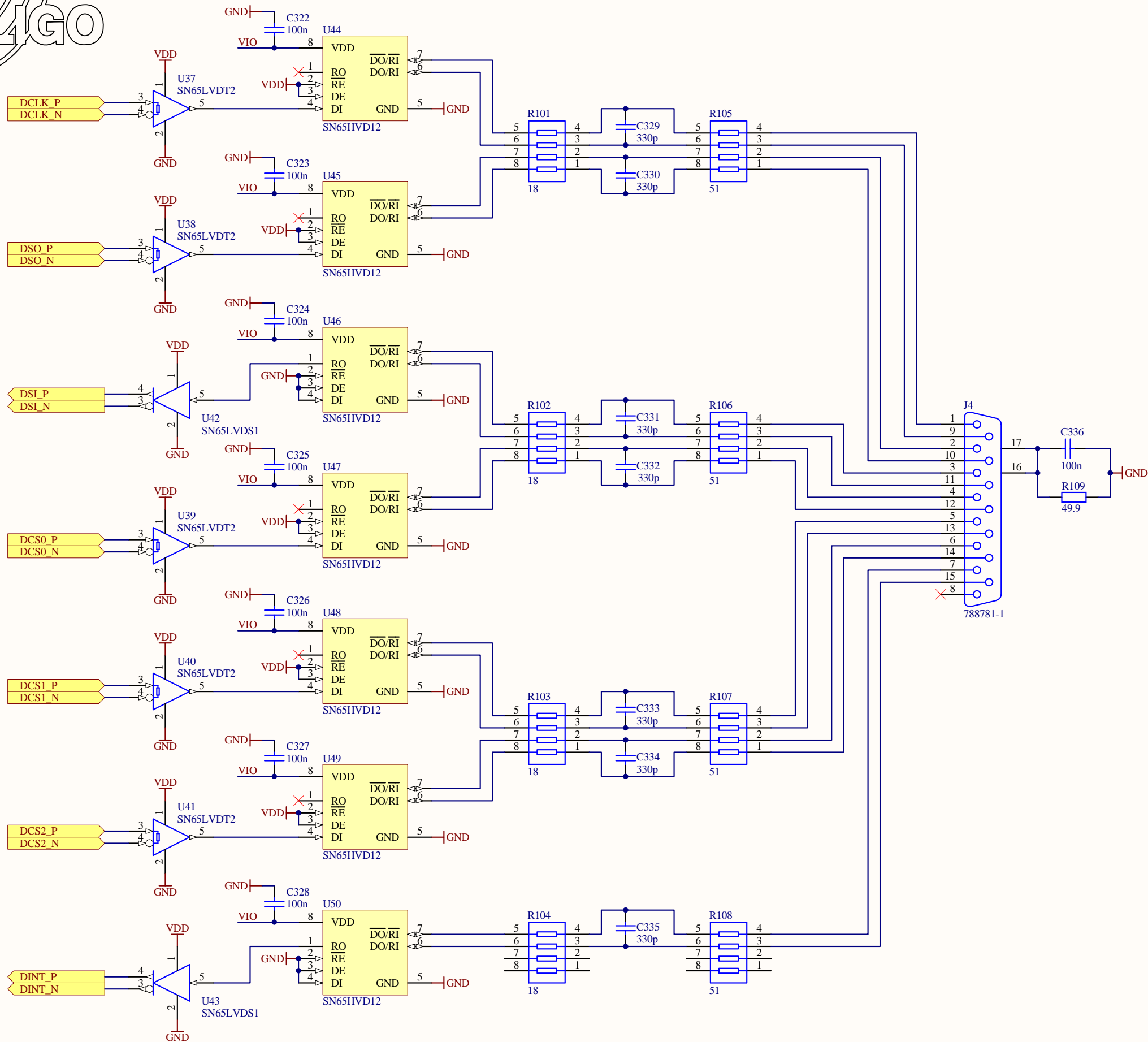
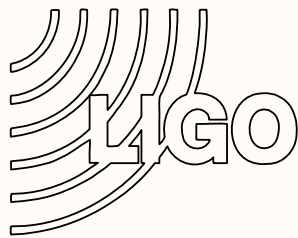


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Size B	Number D060309	Revision A
Date: 11/20/2007	Sheet 1 of 14	
File: C:\User\...\SAUplink9.SchDoc	Drawn By: Daniel Sigg	

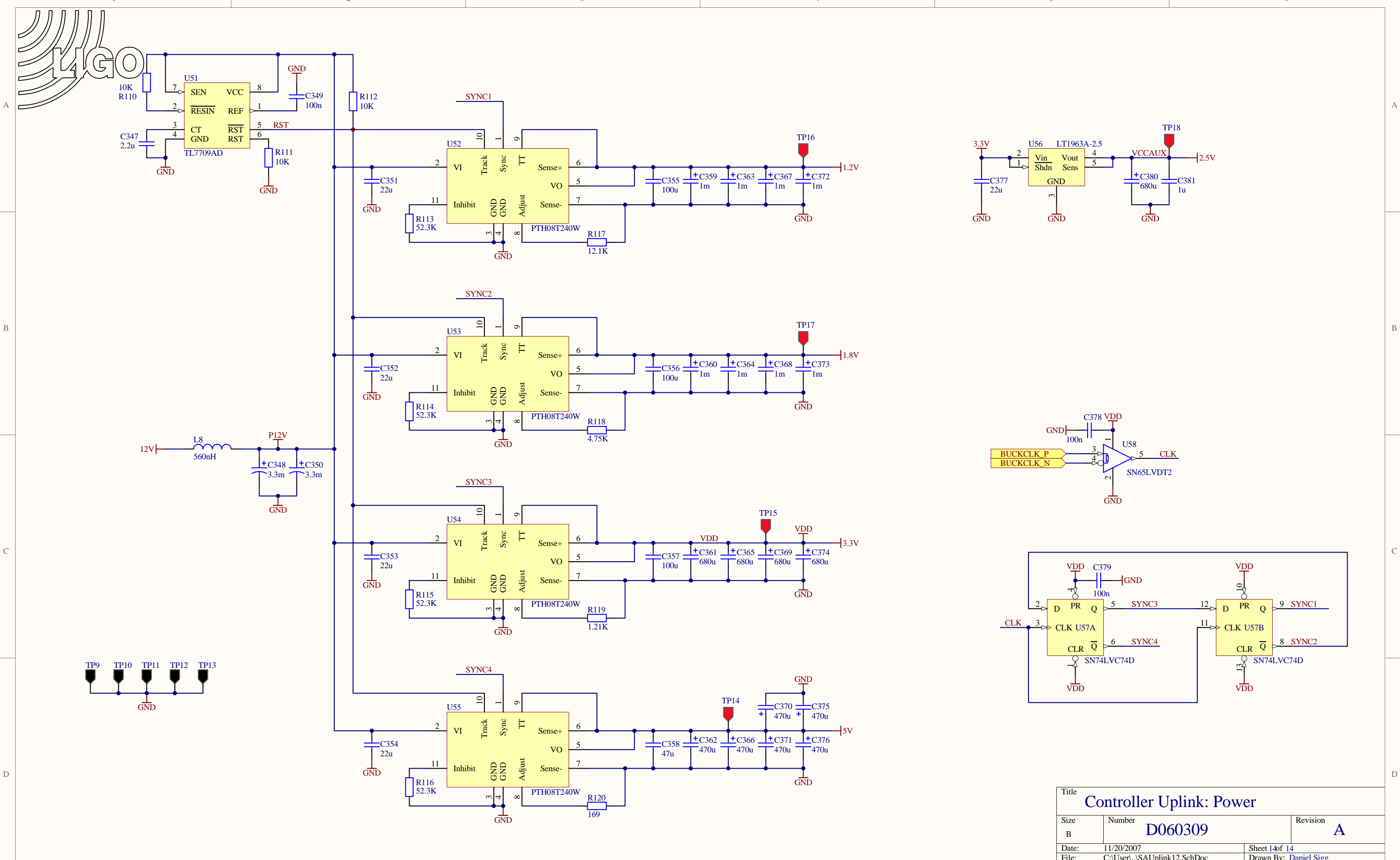


4 SPI Interfaces
 CLK: SPI clock line
 SO: serial data out
 SI: serial data in
 CS[2..0]: chip select
 INT: interrupt line
 Interface with Microship MCP23S17 to generate binary IO signals

Title		
Controller Uplink: Digital links		
Size	Number	Revision
B	D060309	A
Date:	11/20/2007	Sheet 12 of 14
File:	C:\User\...\SAUplink10.SchDoc	Drawn By: Daniel Sigg



Title Controller Uplink: Digital IO		
Size B	Number D060309	Revision A
Date: 11/20/2007	Sheet 13 of 14	
File: C:\User\...\SAUplink11.SchDoc	Drawn By: Daniel Sigg	



Title		
Controller Uplink: Power		
Size	Number	Revision
B	D060309	A
Date:	11/20/2007	Sheet 14 of 14
File:	C:\User\...\SAUplink12.SchDoc	Drawn By: Daniel Sigg