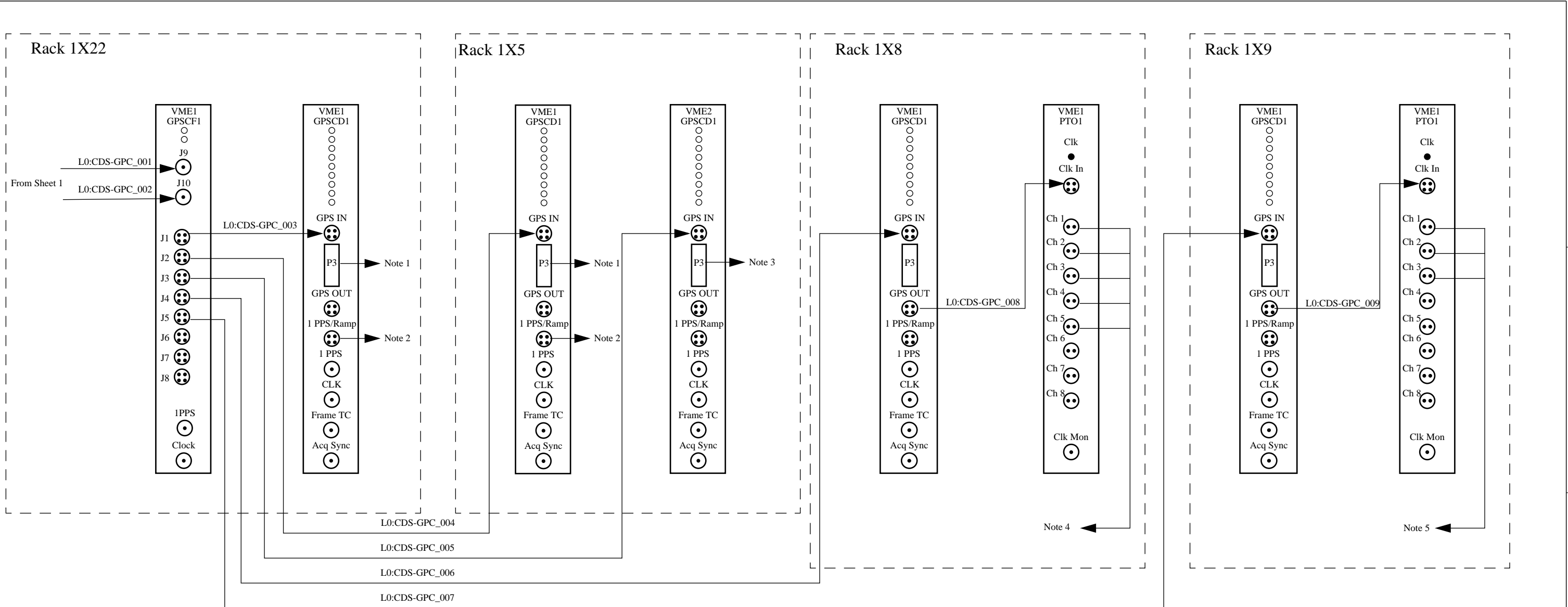


- Notes:
- GPS antennas located on roof of LVEA, as shown.
 - VME GPS modules are of three types:
 - Clock Masters: Receiver with on board 2^{22} Hz clock, phase locked to GPS, for ADC timing.
 - Time Masters: Receiver which distributes GPS time to GPS slave modules via IRIG-B.
 - IRIG Slave: Receives time information via IRIG-B from Time Masters.
 - Timing is provided to CDS ADC modules from LIGO designed timing modules:
 - GPS Clock Fanout (GPSCF): Inputs 1Hz and 2^{22} Hz clock from GPS and provides up to eight fanouts of these signals.
 - GPS Clock Driver (GPSCD): Inputs signals from GPSCF and provides timing to CDS ADC/DAC modules.
 - All time readouts in system are GPS time.

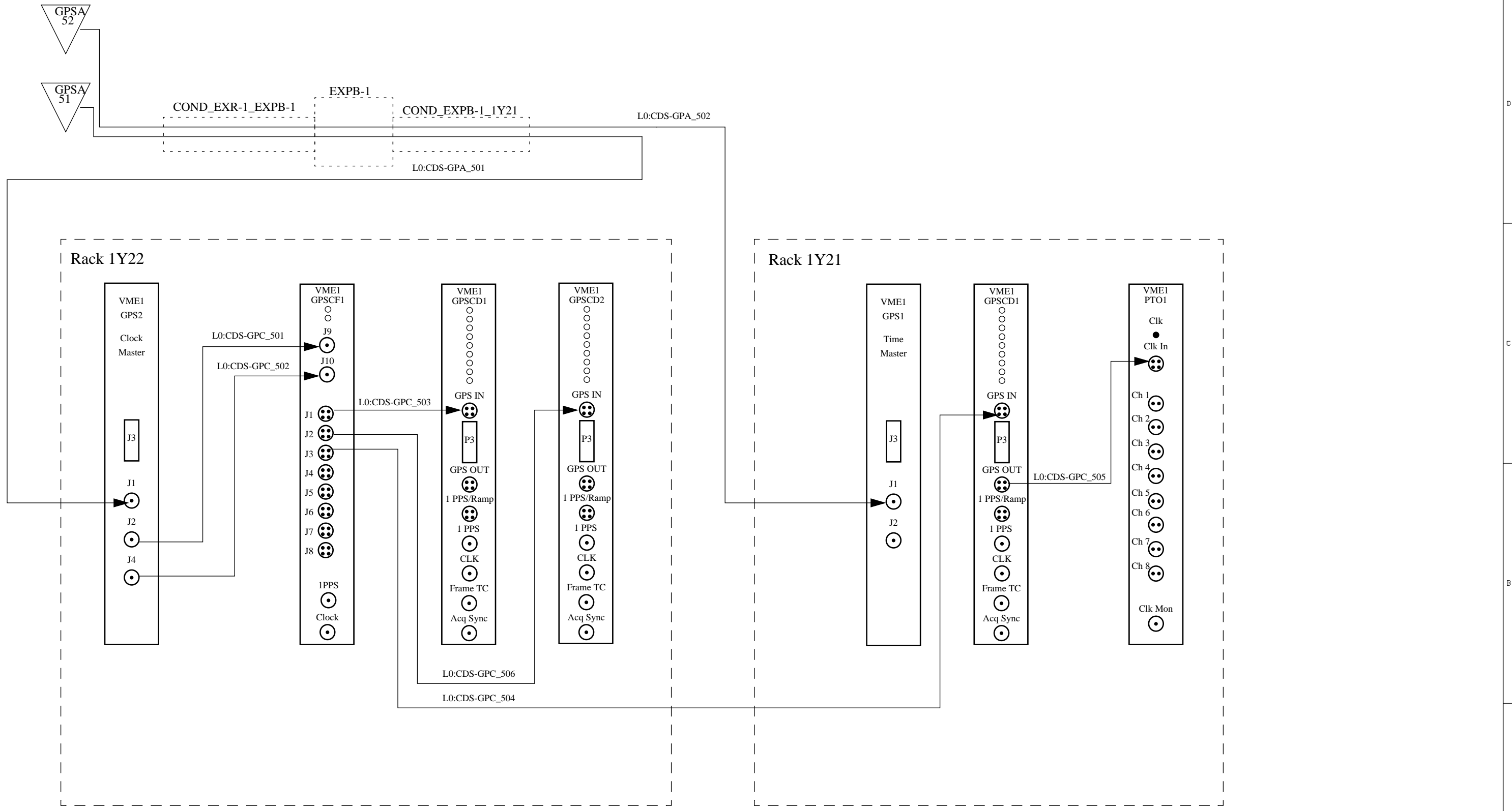
D980362-C	CDS Timing Clock Fanout Module Schematics			UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: FRACTIONAL ± ANGULAR/RACH ± BEND ± TWO PLACE DECIMAL ± THREE PLACE DECIMAL ± FINISHED SURFACE RMS BREAK CORNERS IN OUT, REMOVE ALL BURRS				CURRENT REVISION APPROVAL			LIGO CALIFORNIA INSTITUTE OF TECHNOLOGY MASSACHUSETTS INSTITUTE OF TECHNOLOGY Livingston Timing System Cable Diagram Corner Station Antenna / IRIG-B Connections
D980369-C	CDS Timing Clock Driver Module Schematics							DRAWN	GROUP	SIGNATURE	
							CHECKED	R. Bork		1/21/00	
DWG. NO.	DESCRIPTION	DWG. NO.	DESCRIPTION	USED ON:	REV	DESCRIPTION	SHEETS EFFECTED	DATE			
6	REFERENCE DRAWINGS	5		NEXT ASS'Y:		ISSUE DESCRIPTION			DCC		
											SCALE: B SIZE: B DWG. NO.: D990083-A-C SHEET: 1 of 4 STD: VER: 01



NOTES:

- 1) Connect via Ribbon to ICS-110B ADC modules. See appropriate rack drawing.
- 2) Connect as input to ICS-110B ADC channels for diagnostics. See appropriate rack drawing.
- 3) Connect via ribbon to ICS-115A DAC module. See appropriate rack drawing.
- 4) Connect to ASC Dewhitening filter modules. See ASC drawing set.
- 4) Connect to LSC Dewhitening filter modules. See LSC drawing set

				UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: FRACTIONAL ± ANGULAR/RADIUS ± BEND ± TWO PLACE DECIMAL ± THREE PLACE DECIMAL ± FINISHED SURFACE RMS BREAK CORNERS IN OUT, REMOVE ALL BURRS				CURRENT REVISION APPROVAL				LIGO CALIFORNIA INSTITUTE OF TECHNOLOGY MASSACHUSETTS INSTITUTE OF TECHNOLOGY											
								DRAWN		GROUP		SIGNATURE		DATE		Livingston Timing System Cable Diagram LVEA Master Clock Distribution							
								CHECKED		R. Bork				1/21/00									
				DO NOT SCALE THIS DRAWING				REV		DESCRIPTION		SHEETS EFFECTED		DATE		SCALE		SIZE DWG. NO. B D990083-A-C		REV.			
DWG. NO.				DESCRIPTION				USED ON:				NEXT ASS'Y:		ISSUE DESCRIPTION		SCALE		SHEET 2 of 4		STD VER. 01			
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				UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: FRACTIONAL ± ANGULAR/RADIUS ± BEND ± TWO PLACE DECIMAL ± THREE PLACE DECIMAL ± FINISHED SURFACE RMS BREAK EDGERS IN OUT, REMOVE ALL BURRS				CURRENT REVISION APPROVAL				LIGO CALIFORNIA INSTITUTE OF TECHNOLOGY MASSACHUSETTS INSTITUTE OF TECHNOLOGY											
								DRAWN		GROUP		SIGNATURE		DATE		Livingston Timing System Cable Diagram Y Arm End Station							
								CHECKED		R. Bork				1/21/00									
				DO NOT SCALE THIS DRAWING				REV		DESCRIPTION		SHEETS EFFECTED		DATE		SCALE: B SIZE DWG. NO. D990083-A-C REV.							
DWG. NO.				DESCRIPTION				DWG. NO.				DESCRIPTION				SCALE: B SHEET 4 of 4 STD VER. 01							
6				5				4				3				2				1			
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