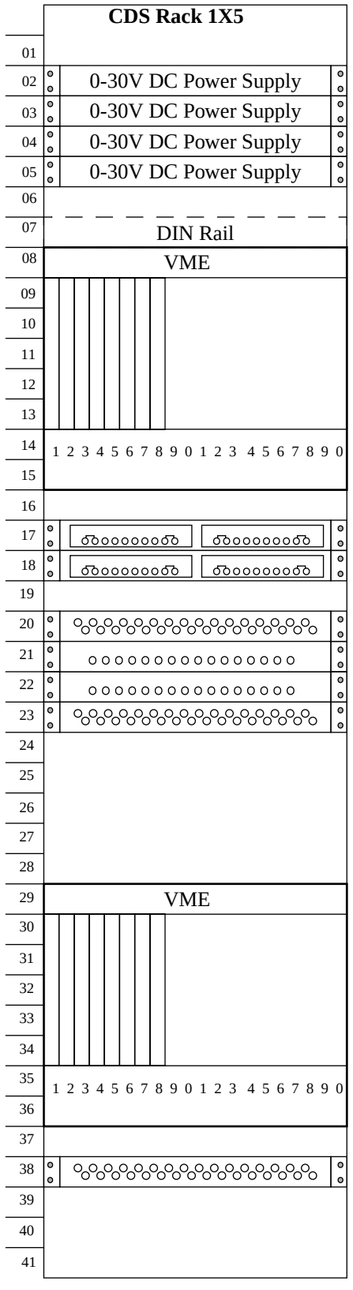

Rack Mount Components w/Locations

Loc	Description	Vendor	Model	Designator
02	+/- 0-30VDC Power Supply	Sorenson		PS-1
03	+/- 0-30VDC Power Supply	Sorenson		PS-2
04	+/- 0-30VDC Power Supply	Sorenson		PS-3
05	+/- 0-30VDC Power Supply	Sorenson		PS-4
07	DIN Rail w/terminal blocks (rear mount)			DIN-1
08	VME Crate (Data Acquisition)			VME-1
17	DAQS Interface Chassis (LEMO)	LIGO		DAQIC-1
18	DAQS Interface Chassis (LEMO)	LIGO		DAQIC-2
20	DAQS Interface Chassis (BNC/1KFilter)	LIGO		DAQIC-3
21	Accelerometer Signal Conditioner	Endevco		ACCSC-1
22	Accelerometer Signal Conditioner	Endevco		ACCSC-2
23	DAQS Interface Chassis (BNC/1KFilter)	LIGO		DAQIC-4
29	VME Crate (Global Diagnostics)			VME-2
38	GDS BNC Patch Panel	LIGO		GDSIC-1

NOTES:
1) Field cabling associated with the Global Diagnostics installed in VME2 is still TBD; therefore, for GDS, only the VME crate layout is valid for this release.
2) For timing and network connections to this rack system, see referenced drawings.

VME1 Modules / Slot Assignments

Slot	Description	Vendor	Model	Designator
1	MIPS Processor	Heurikon	4700E	CPU-1
2	MIPS Processor	Heurikon	4700E	CPU-2
3	Reflected Memory	VMIC	5588DMA	RFM-1
4	GPS Slave	Brandywine		GPS-1
5	Timing Slave	LIGO		TS-1
6	32 channel ADC	ICS	110B1	ADC-1
7	32 channel ADC	ICS	110B1	ADC-2
8	32 channel ADC	ICS	110B1	ADC-3
9	32 channel ADC	ICS	110B1	ADC-4
10				
11	Backplane Split ----------	----------	----------	----------
12	68040 Processor	Motorola	162-333	CPU-3
13-21	Empty	----------	----------	----------

VME2 Modules / Slot Assignments

Slot	Description	Vendor	Model	Designator
1	MIPS Processor	Heurikon	4700E	CPU-1
2	Reflected Memory	VMIC	5588DMA	RFM-1
3	GPS Slave	Brandywine		GPS-1
4	Timing Slave	LIGO		TS-1
5	32 channel DAC	ICS	115	DAC-1
6				

Reference Drawings

DWG Number	Description
D990083-C	Livingston Timing System Cable Diagram
D990084-C	Livingston Data Acquisition System Network
D990085-C	Livingston Control and Monitoring Network

Revision History

REV	Date	Description
A	1/31/00	Initial Release

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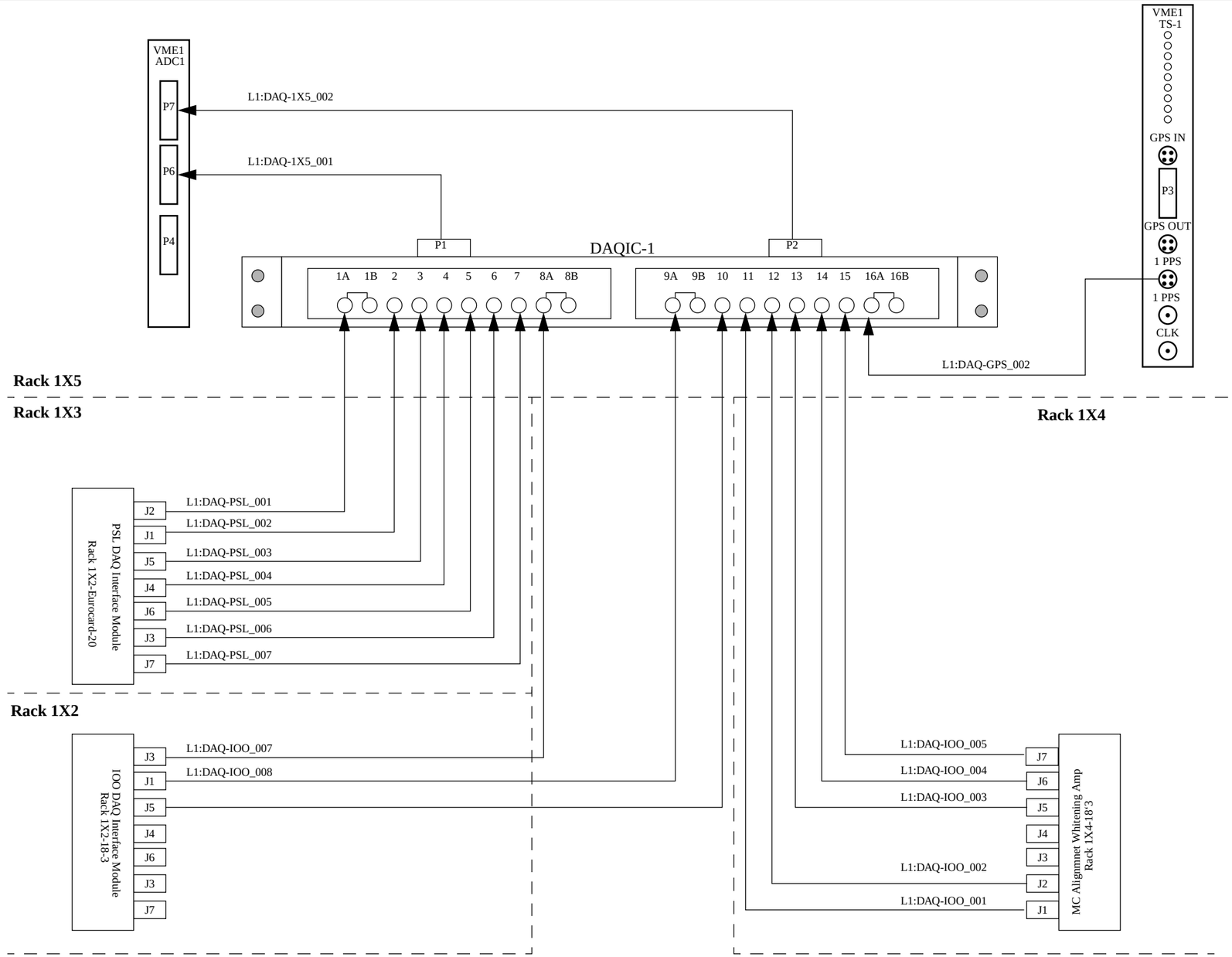
Livingston CDS Rack Layout - 1X5
Chassis Layouts

Drawn By: R. Bork
Date: 1/31/00
Dwg. No. D990163-A-C
Sheet 1 of 7

ADC-1

Conn	Chan	Name	Rate
1A	00	L1:PSL-FSS_MIXERM_F	16384
	01	L1:PSL-FSS_PCDRIVE_F	16384
2	02	L1:PSL_FSS_SADRIVE_F	2048
	03	L1:PSL-FSS_FAST_F	16384
3	04	L1:PSL-ISS_ISERR_F	16384
	05	L1:PSL-ISS_ACTM_F	16384
4	06	L1:PSL-PMC_ERR_F	16384
	07	L1:PSL-PMC_PZT_F	2048
5	08	L1:PSL-FSS_RFPDDC_F	256
	09	L1:PSL-FSS_RCTRANSPD_F	256
6	10	L1:PSL-PMC_RFPDDC_F	256
	11	L1:PSL-PMC_TRANSPD_F	256
7	12		
	13		
8A	14		
	15	L1:IOO-MCA_OUT_MON	2048
9A	16	L1:IOO-MC_I	2048
	17	L1:IOO-MC_LOOP	2048
10	18	L1:IOO-MC_AO	2048
	19	L1:IOO-MC_TEST_MON	2048
11	20	L1:IOO-WFS1_P	2048
	21	L1:IOO-WFS1_Y	2048
12	22	L1:IOO-WFS2_P	2048
	23	L1:IOO-WFS2_Y	2048
13	24	L1:IOO-MC1_P	2048
	25	L1:IOO-MC1_Y	2048
14	26	L1:IOO-MC1_REF	2048
	27	L1:IOO-MC2_P	2048
15	28	L1:IOO-MC2_Y	2048
	29	L1:IOO-MC2_REF	2048
16A	30	L1:GDS-GPS_RAMP2	16384
	31	L1:GDS-GPS_TRIG2	16384



Reference Drawings

DWG Number	Description
D980535-C	PSL Wiring Diagram
D990089-C	Mode Cleaner Whitening Filter
D990010-C	Input Optics Wiring Diagram

Revision History

REV	Date	Description

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Livingston CDS Rack Layout - 1X5
DAQIC-1 Connections

Drawn By: R. Bork

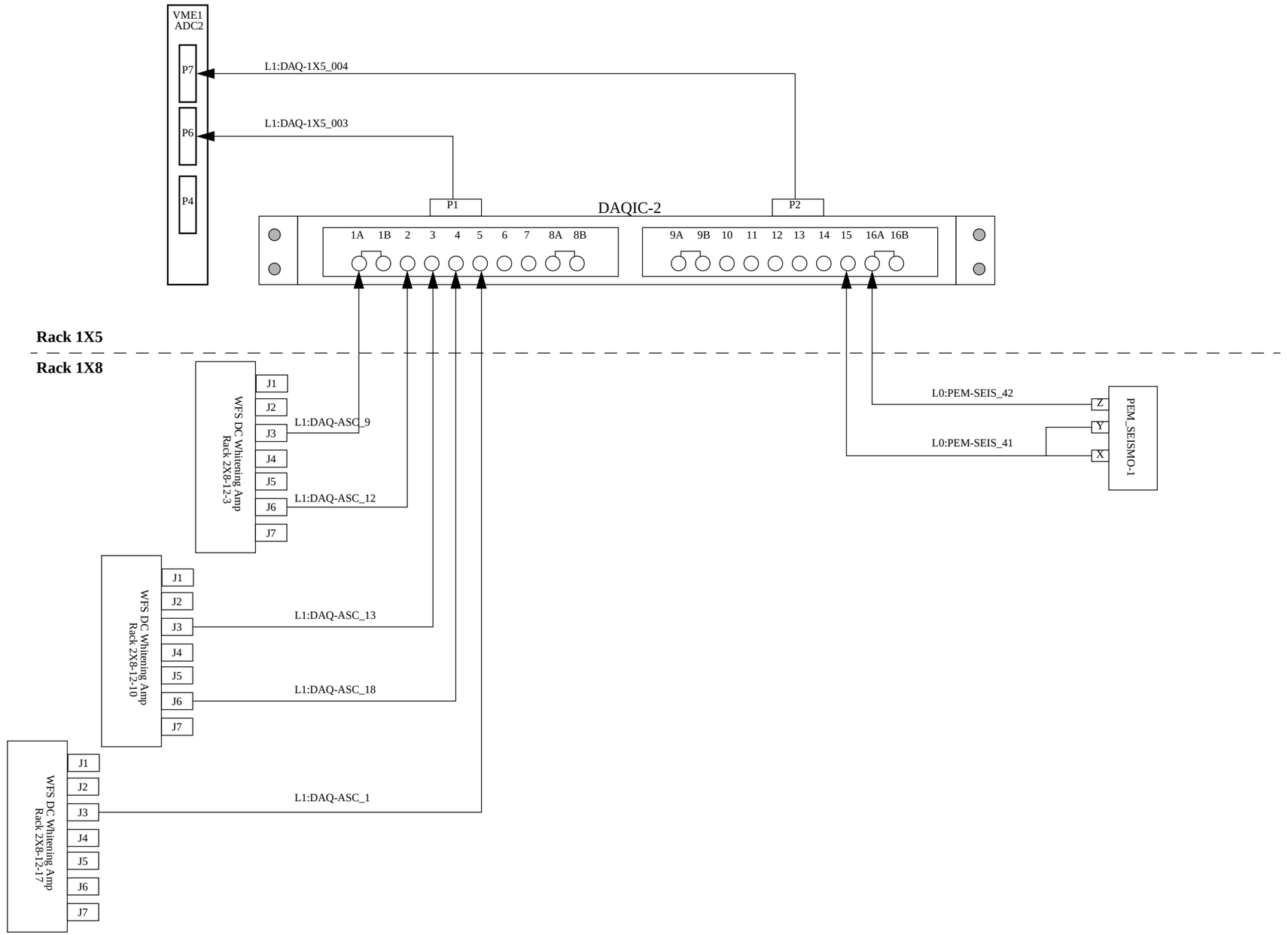
Dwg. No. D990163-A-C

Date: 1/31/00

Sheet 2 of 7

ADC-2

Conn	Chan	Name	Rate
1A	00	L1:ASC-WFS1_DCP	2048
1B	01	L1:ASC-WFS1_DCY	2048
2	02	L1:ASC-WFS2_DCP	2048
	03	L1:ASC-WFS2_DCY	2048
3	04	L1:ASC-WFS3_DCP	2048
	05	L1:ASC-WFS3_DCY	2048
4	06	L1:ASC-WFS4_DCP	2048
	07	L1:ASC-WFS4_DCY	2048
5	08	L1:ASC-WFS5_DCP	2048
	09	L1:ASC-WFS5_DCY	2048
6	10		
	11		
7	12		
	13		
8A	14		
8B	15		
9A	16		
	17		
10	18		
	19		
11	20		
	21		
12	22		
	23		
13	24		
	25		
14	26		
	27		
15	28	L0:PEM-LVEA_SEISX	256
	29	L0:PEM-LVEA_SEISY	256
16A	30	L0:PEM-LVEA_SEISZ	256
	31		



Reference Drawings	
DWG Number	Description
D990257-C	ASC Wiring Diagram

Revision History		
REV	Date	Description

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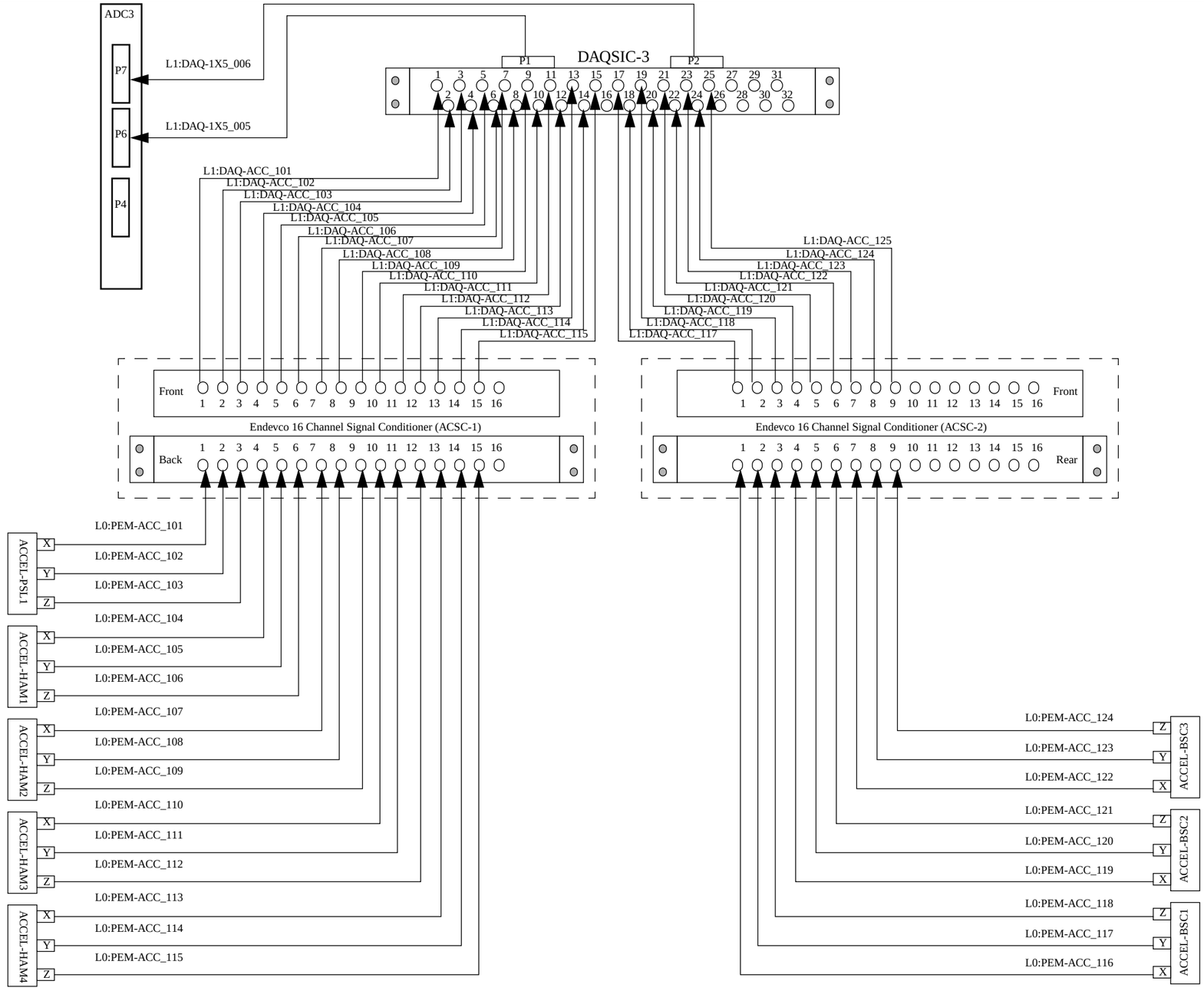
Livingston CDS Rack Layout - 1X5
DAQIC-2 Connections

Drawn By: R. Bork
Date: 1/31/00

Dwg. No. D990163-A-C
Sheet 3 of 7

ADC-3

Conn	Chan	Name	Rate
1	00	L0:PEM-PSL1_ACCX	2048
2	01	L0:PEM-PSL1_ACCY	2048
3	02	L0:PEM-PSL1_ACCZ	2048
4	03	L0:PEM-HAM1_ACCX	2048
5	04	L0:PEM-HAM1_ACCY	2048
6	05	L0:PEM-HAM1_ACCZ	2048
7	06	L0:PEM-HAM2_ACCX	2048
8	07	L0:PEM-HAM2_ACCY	2048
9	08	L0:PEM-HAM2_ACCZ	2048
10	09	L0:PEM-HAM3_ACCX	2048
11	10	L0:PEM-HAM3_ACCY	2048
12	11	L0:PEM-HAM3_ACCZ	2048
13	12	L0:PEM-HAM4_ACCX	2048
14	13	L0:PEM-HAM4_ACCY	2048
15	14	L0:PEM-HAM4_ACCZ	2048
16	15		
17	16	L0:PEM-BSC1_ACCX	2048
18	17	L0:PEM-BSC1_ACCY	2048
19	18	L0:PEM-BSC1_ACCZ	2048
20	19	L0:PEM-BSC2_ACCX	2048
21	20	L0:PEM-BSC2_ACCY	2048
22	21	L0:PEM-BSC2_ACCZ	2048
23	22	L0:PEM-BSC3_ACCX	2048
24	23	L0:PEM-BSC3_ACCY	2048
25	24	L0:PEM-BSC3_ACCZ	2048
26	25		
27	26		
28	27		
29	28		
30	29		
31	30		
32	31		



Reference Drawings

DWG Number	Description

Revision History

REV	Date	Description

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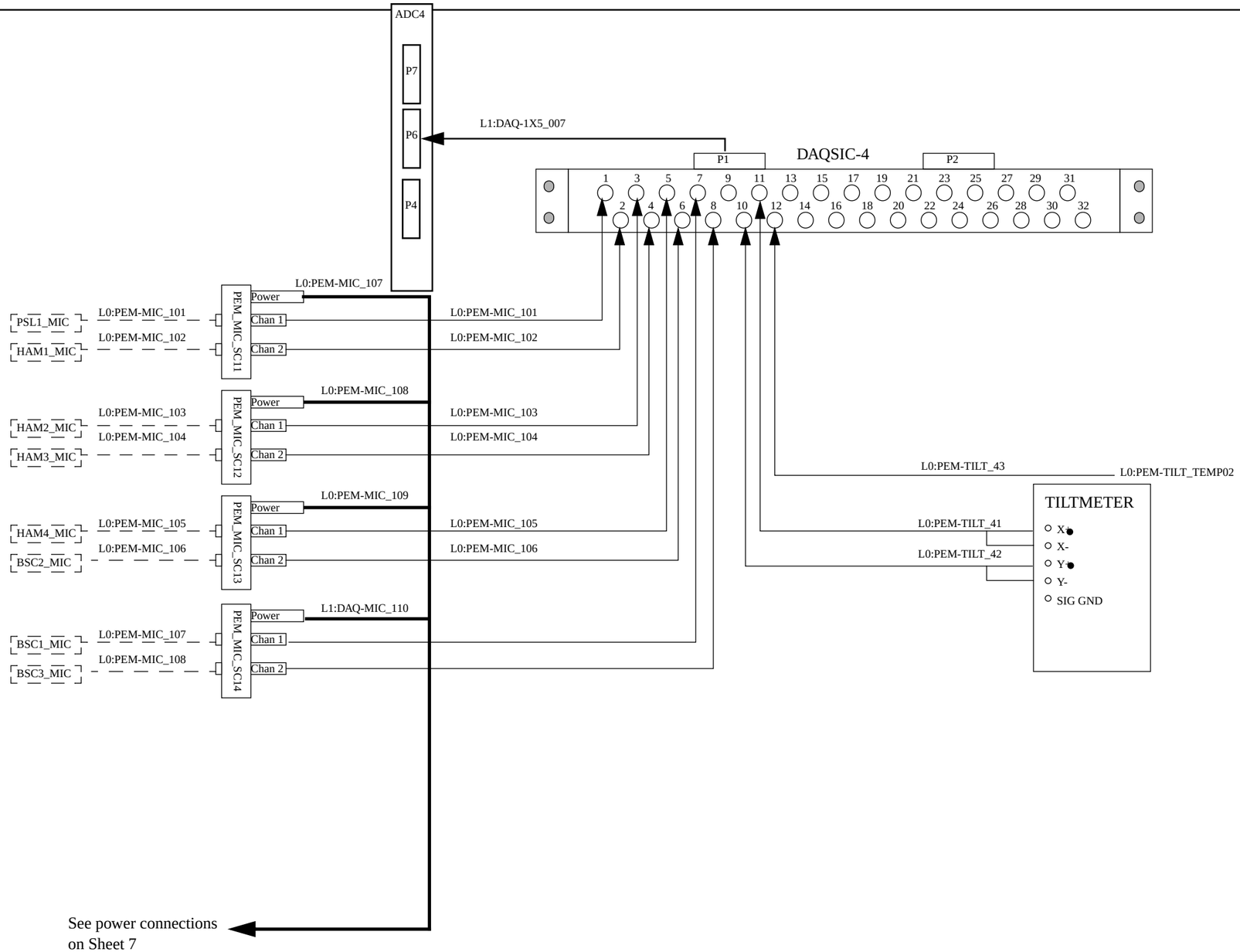
Livingston CDS Rack Layout - 1X5
DAQIC-3 Connections

Drawn By: R. Bork
Date: 1/31/00

Dwg. No. D990163-A-C
Sheet 4 of 7

ADC-4

Conn	Chan	Name	Rate
1	00	L0:PEM-PSL1_MIC	2048
2	01	L0:PEM-HAM1_MIC	2048
3	02	L0:PEM-HAM2_MIC	2048
4	03	L0:PEM-HAM3_MIC	2048
5	04	L0:PEM-HAM4_MIC	2048
6	05	L0:PEM-BSC2_MIC	2048
7	06	L0:PEM-BSC1_MIC	2048
8	07	L0:PEM-BSC3_MIC	2048
9	08		
10	09	L0:PEM-TILTY	256
11	10	L0:PEM-TILTX	256
12	11	L0:PEM-TILTT	256
13	12		
14	13		
15	14		
16	15		
17	16	L1:GDS-LVEA_DAC1	16384
18	17	L1:GDS-LVEA_DAC2	16384
19	18	L1:GDS-LVEA_TO1	16384
20	19	L1:GDS-LVEA_TO2	16384
21	20	L1:GDS-LVEA_TO3	16384
22	21	L1:GDS-LVEA_TO4	16384
23	22	L1:GDS-LVEA_TO5	2048
24	23	L1:GDS-LVEA_TO6	2048
25	24	L1:GDS-LVEA_TO7	2048
26	25	L1:GDS-LVEA_TO8	2048
27	26	L1:GDS-LVEA_TO9	2048
28	27	L1:GDS-LVEA_T10	2048
29	28	L1:GDS-LVEA_T11	2048
30	29	L1:GDS-LVEA_T12	2048
31	30	L1:GDS-LVEA_T13	2048
32	31	HPEM-NBR_2K	16384
		TOTAL (BTYES/SEC)	**302080**



Reference Drawings	
DWG Number	Description

Revision History		
REV	Date	Description

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Livingston CDS Rack Layout - 1X5
DAQIC-4 Connections

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Date: 1/31/00

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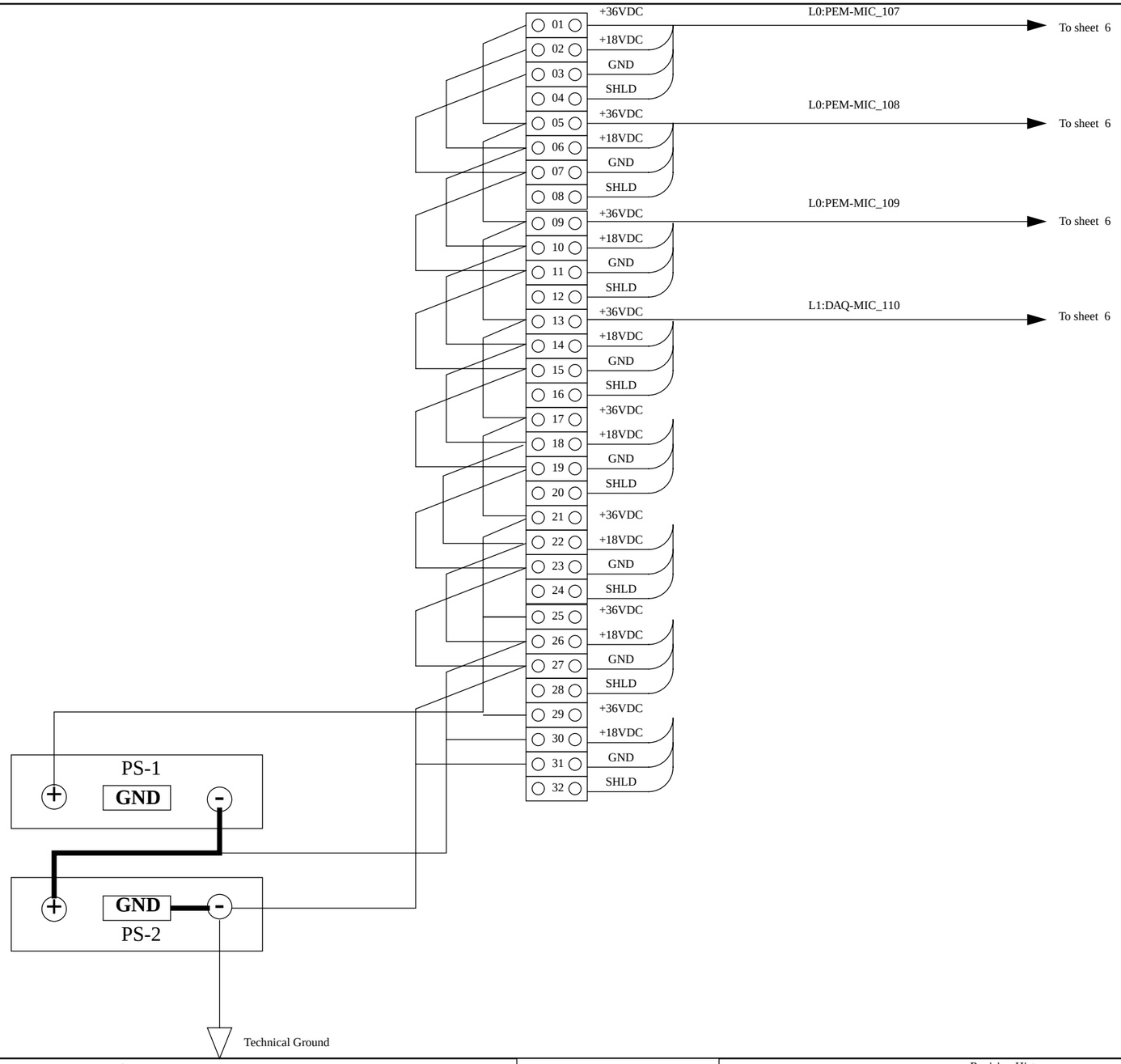
Sheet 5 of 7



Reference Drawings	
DWG Number	Description

Revision History		
REV	Date	Description

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Livingston CDS Rack Layout - 1X5
Microphone DC Power Distribution

Drawn By: R. Bork	Dwg. No. D990163-A-C
Date: 1/31/00	Sheet 6 of 7

Note:

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Reference Drawings	
DWG Number	Description

Revision History		
REV	Date	Description

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Livingston CDS Rack Layout - 1X5
GDS Connections

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Date: 1/31/00

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