LIGO Laboratory / LIGO Scientific Collaboration

LIGO-E020350-04-R 6/18/2002

EMI, Shielding and Grounding Cleanup Plan

M. Zucker

Distribution of this document:
LIGO detector commissioning team

This is an internal working note
of the LIGO Laboratory.

California Institute of Technology
LIGO Project – MS 18-34
1200 E. California Blvd.
Pasadena, CA 91125
Phone (626) 395-2129
Fax (626) 304-9834
E-mail: info@ligo.caltech.edu

Massachusetts Institute of Technology
LIGO Project – NW17-161
175 Albany St
Cambridge, MA 02139
Phone (617) 253-4824
Fax (617) 253-7014
E-mail: info@ligo.mit.edu

LIGO Hanford Observatory
P.O. Box 1970
Mail Stop S9-02
Richland WA 99352
Phone 509-372-8106
Fax 509-372-8137

LIGO Livingston Observatory
P.O. Box 940
Livingston, LA 70754
Phone 225-686-3100
Fax 225-686-7189

http://www.ligo.caltech.edu/

Introduction

Commissioning has highlighted inadequacies with the as-built site electronics architecture. We present a plan for addressing these through a phased reworking of packaging, shielding and interconnection protocols, in most cases maintaining current boards and modules as-is or with minor modifications. Our plan is grounded in a few points of philosophy:

- Most vulnerabilities became apparent only in hindsight, looking at the integrated installation. Individual components have been extensively tested offline, so most remaining problems are related to environment, connectivity and proximity interactions.
- Such interactions are usually nonstationary, and often nonlinear.
- At any given time, few will be "dominant" contributors of noise, and most will not cause measurable effects; conversely, other effects we haven't thought of are likely to be problems.
- Nonetheless, the sheer volume of phase space for potential problems is the primary obstacle to troubleshooting unknown noise. Eliminating questionable practices and opportunities for future suspicion is thus a worthy objective on its own.
- Falling back on conservative design practices and striving for excess design margin is the accepted way of accomplishing this, even though it costs time and money in the short term.

On one hand, EMI and grounding problems are intrinsically distributed, and partial or local solutions (other than correcting egregious mistakes) rarely have much impact. On the other hand, it's not practical to start over from scratch, nor can all fixes be implemented the same day. The following classifications and problem descriptions are intended to help prioritize the phasing of corrective measures. At the same time it's important to maintain a coherent vision of the machine as an integrated system and avoid interim or temporary thinking; to support this, an integrated design concept is presented for the retrofit. Finally we outline a proposed implementation sequence intended to minimize impact to ongoing commissioning and observing.

Problem Classes

We somewhat arbitrarily divide the problems into 5 classes:

- 60 Hz + harmonics line hum
- DC power supply ripple & radiation, incl. switcher noise
- Digital clock and VME bus noise
- External RFI
- RF modulation leakage

The divisions aren't crisp, since problems interact; e.g., in some cases the best solution for one (say 60 Hz line hum) is the worst for another (say RF pickup). Within a given category there are also different aspects that may conflict, for example, magnetic vs. electrostatic coupling. Nevertheless we find the context useful for discussing priorities.

The last category (line hum and RF modulation leakage, respectively) stands out in that line interference is currently disastrous. We can definitely say that the grounding and shielding practices called for in the design have *not* been uniformly followed in the field installations. As a result, while it's possible to theorize about better and worse practices in the abstract there's little usable (stable and extrapolatable) information on current performance. Furthermore, in this arena it is easy for a single minscule exception (say an unseen BNC splice barrel buried in a cable tray) to defeat the entire strategy. Therefore it's a high priority to bring both sites into uniform compliance with some given grounding and shielding protocol, before we can invest in a systematic evaluation.

Observed Problems

Clock and bus noise on ASC and LSC Pentek inputs and outputs:

We see several hundred millivolts p-p of RF hash on the input pins of the Pentek 6102 ADC's, with frequency components up to a few hundred MHz and burst rates synchronized with 4.2 MHz sample clocks. It is not stationary and depends on movement of ribbon cables, people and equipment nearby the racks. Remarkably, this has not yet caused documented "excess" noise, even though signals of this magnitude and frequency are deemed likely to be rectified by audio-frequency semiconductor devices within the analog front ends and ADC, and the burst rep rates are semi-synchronous with the acquisition sample rate. Sniffing with a probe coil points to many potential radiative/inductive sources for this energy within the VME crate, including the unused multi-pin bus connector on the Pentek front panel itself and (somewhat remarkably) the reflective memory modules. Some of the hash is also conducted or capacitively coupled directly to the Pentek input pins within the module, however. It is hard to concieve of a way to address this without redesigning the 6102 (internal inspection indicates insufficient attention was paid to proper EMC/EMI practices by its designers).

We also see excess nonstationary noise on the Pentek DAC outputs. Large periodic pulses appear to be "ground bounce" associated with polling of the VME backplane, causing deflection of the DAC "analog" ground (obviously derived from the VME backplane) with respect to the ground potential of subsequent analog modules. (Note: this is distinct from the excess and variable noise associated with high-speed DAC clocking, discussed elsewhere).

In principle we should see no out-of-band noise beyond the intrinsic Johnson noise associated with the respective characteristic impedances. Best practice would insure that the ADC input pins be protected from any interfering signal comparable to 1 LSB at any frequency (above or below the Nyquist rate). Since we rely on squeezing the full dynamic reserve out of the DAC, this principle in our case applies equally to the outputs within the signal band. Nonlinearity of the audio filter electronics at high frequencies

would argue for comparable protection of the downstream anti-image and dewhitening filters at RF as well.

Some of the observed hash results from some known and relatively obvious errors:

- the default ADC and DAC clock inputs for the Pentek 6102 are derived from pins on the analog input/output connectors, and the TTL clock signals must thus be passed through the analog whitening and dewhitening modules and travel alongside the sensitive signal lines through the long analog I/O ribbon cable. A retrofit to the Penteks which brings the clocks in on separate, shielded LEMO connectors on the front panels is in progress and partially implemented.
- Because of the peculiar multipin analog I/O connector on the 6102, unshielded flat ribbon cables were initially used to connect to/from the analog interface boards. In some cases, because of indefinite module placement and rearrangement, these cables were also made excessively long. They are gradually being replaced by rolled/shielded twisted pair ribbon cables of minimum service length, with shields grounded at the analog interface end. These corrective measures helped significantly with induced RF potentials, but have limitations. There is no provision for eliminating the bus-induced fluctuations in the VME ground potential, and a shunt current path is still provided between the VME crate and analog Eurocard crate grounds (this is bound to increase susceptibility to external RFI, line interference and switcher noise induction as well, by affording a "loop return").
- There is no way to separate the Pentek physically from the hash inherent in a VME crate environment. However, the 6102 does have crude differential ADC inputs, and its DAC is expected to be reasonably accurate with respect to its own "signal ground". What is really needed to isolate the connection between the ADC and DAC and their analog interface cards, essentially treating the ADC and DAC as "hostile" sinks and sources by rejecting all common-mode potentials and RF. We can then do best by referencing input and output signals to the Pentek reference voltages, however crappy they may be.

Loop & whip antennas with ASC and LSC remote front end wiring:

The LSC and ASC use remote sensor devices located on the ISC tables. Each sensor typically uses separate power, DC output, HV bias, RF output and test input cables, which run separately from the head to different locations within the mother rack (or even several racks). These long runs form significant loop areas which intersect magnetic flux, causing ground currents to flow through the sensor head and rack at each end.

The sensors are all designed to float from the optical table and vacuum system ground; however, many lines have been extended or otherwise modified such that an exposed connector body or shield braid can randomly touch the metallic table surface or cable tray, providing a current path from the front end to VE/facility ground. In some cases this has been patched by disconnecting the cable shield, defeating its screening effect.

LSC and ASC front ends also receive local oscillator RF from distribution systems, whose oscillators are located in the PSL/IO racks. This provides an additional group of paths for unintentional ground current.

Many current LSC and ASC boards do not have independent, contiguous Faraday shielding and/or use unshielded cables and connectors to join modules within a crate.

MC and PSL analog control line ground loops/antennas:

These signals travel from rack to rack and thus form loops with safety and powerline grounds. Currently most (though not all) these signals travel via shielded differential twisted-pairs with buffered transmitters and differential receivers. However both driver and receiver circuits are referenced to local rack cross-connect power supplies and grounds, and for RFI immunity the shields may need to be contiguous (again, actual installation practice varies here).

Back-end dewhitening, coil driver, satellite and coil wiring:

Somewhat counterintuitively, the "back end" dewhitening and coil drive circuitry is arguably our most sensitive point for induced voltages and currents. These signals demand interference levels well below the thermal noise in the driving circuits (nanovolts and picoamperes, respectively) as thermodynamics has afforded us no operating margin. The following problems with our current treatment of these signals have been observed:

- The dewhitening filters suffer from the same problems associated with other analog Eurocard implementations (above)
- For both analog and digital suspension systems, analog coil drivers are generally located in a different rack that the dewhitening filter which serves them. Although we are now usually using differential driver/receivers to transmit these signals these sets are not fully isolated (power and signal are locally referenced) so they provide some CMR but still permit current flow.
- There is anecdotal evidence that the failure of LOS controllers to meet noise specifications in the field is related to internal ground plane and layout practices within the chassis, coupled to the intense EMI/RFI environment found in the racks. It is hoped that the redesigned coil drivers (associated with the DSC) will not suffer from this problem.
- The satellite modules (which are maintained with the DSC) are subject to accidental grounding to cable trays or vacuum equipment
- Multiconductor cables from coil drivers to the satellite modules and from the modules to the VE feedthroughs is not shielded or shields are not correctly terminated

Rack cross-connect radiation & reception:

The rack cross-connects present a large cross section for magnetic and electrostatic pickup. They are optimally positioned to intersect magnetic flux from power supplies in the rack proper and bus hash from the VME crates. Wiring from supplies to cross-connect blocks and from cross-connects to devices is several meters in length, and has appreciable self-inductance, permitting end-to-end HF potential drops of a volt or more in

some cases. Wires also have high capacitive cross-coupling to each other. Within a single analog Eurocard crate there are typically several independent power supply and ground connections back to cross-connect fuse blocks; beyond its redundancy, this introduces multiple closed loop antennas.

Unshielded ribbon cables serving the EPICS ADC, DAC and DIO modules conduct VME backplane and device clock hash directly into the cross-connect area, inducing interfering broadband signals up to 0.5 Vpp in some "ground" and "DC power" lines. Direct conductive paths also join these VME devices to control and readout points within the low-level analog control cards, which generally sense and drive single-ended and may have little or no on-board isolation or filtering. TTL control points are also brought into modules without isolation, conjoining analog signal, analog power, and digital (VME) grounds. Analog grounds are also connected to the rack via mounting points, compounding stray current opportunities.

RF distribution:

The system as-built radiates relatively little RF (at least by comparison with campus lab experience). Unfortunately the susceptibility of certain sensitive boards (e.g., WFS demodulators; see below) is very high due to their own design problems. This leads to an unacceptable and highly variable DC offset problem in the ASC system.

The RF distribution also provides inadvisable current paths between widely separated racks. There's no reason to maintain DC continuity for RF distribution, so DC blocks should be installed on one end of any inter-rack run. Balancing certain runs may also be helpful.

Unshielded boards & crates:

Many Eurocard boards have essentially no shielding other than their own ground plane (where it exists). Our analog Eurocard crates have open tops, backs and sides and no provision for closing off unused front panel space or interconnection areas. Their backplane wiring is fully exposed.

Switching power supply radiation, induction and conduction

The Sorenson switching supplies radiate and conduct magnetic field pulses at their switch rates (typically 60-80 kHz). These pulses are envelope-modulated at the 60 Hz line rate and harmonics. The supplies are located directly above the sensitive electronics and cables and adjacent to the cross-connect, coupling this flux efficiently into circuits. Partial shielding and loop area variation makes the interference highly variable and unpredictable.

RF "tails" have been seen in the radiation from these supplies extending into to the main LIGO RF modulation bands (25 and 29 MHz), and picked up on ASC or LSC front-end RF signal lines. Directly demodulated, these signals will appear in our signal band with variable and unpredictable frequencies and amplitudes. In addition, there is evidence that emissions at all frequencies are rectified by analog circuits. In particular there is a conjecture that this phenomenon is responsible for the anomalous increase in suspension coil driver noise when the drivers are moved from the electronics lab out to the LVEA floor.

Although some tests have been made with the supplies removed to a separate rack, radiated emissions are not found to be adequately attenuated by this step alone. Substitution of linear-regulated supplies (if space can be found to house them) would reduce the radiated emission but might simultaneously increase direct magnetic induction due to the introduction of large 60 Hz power transformers.

Retrofit Design

The planned reorganization for analog cabling and shielding to address these problems is schematically depicted in Figure 1, which shows (as an example) how LSC system components will be redeployed. In this schematic, plain black objects represent existing modules or connections, whereas those shown in color represent new or substantially modified components. These new or modified components and their functional features are described in the sections below.

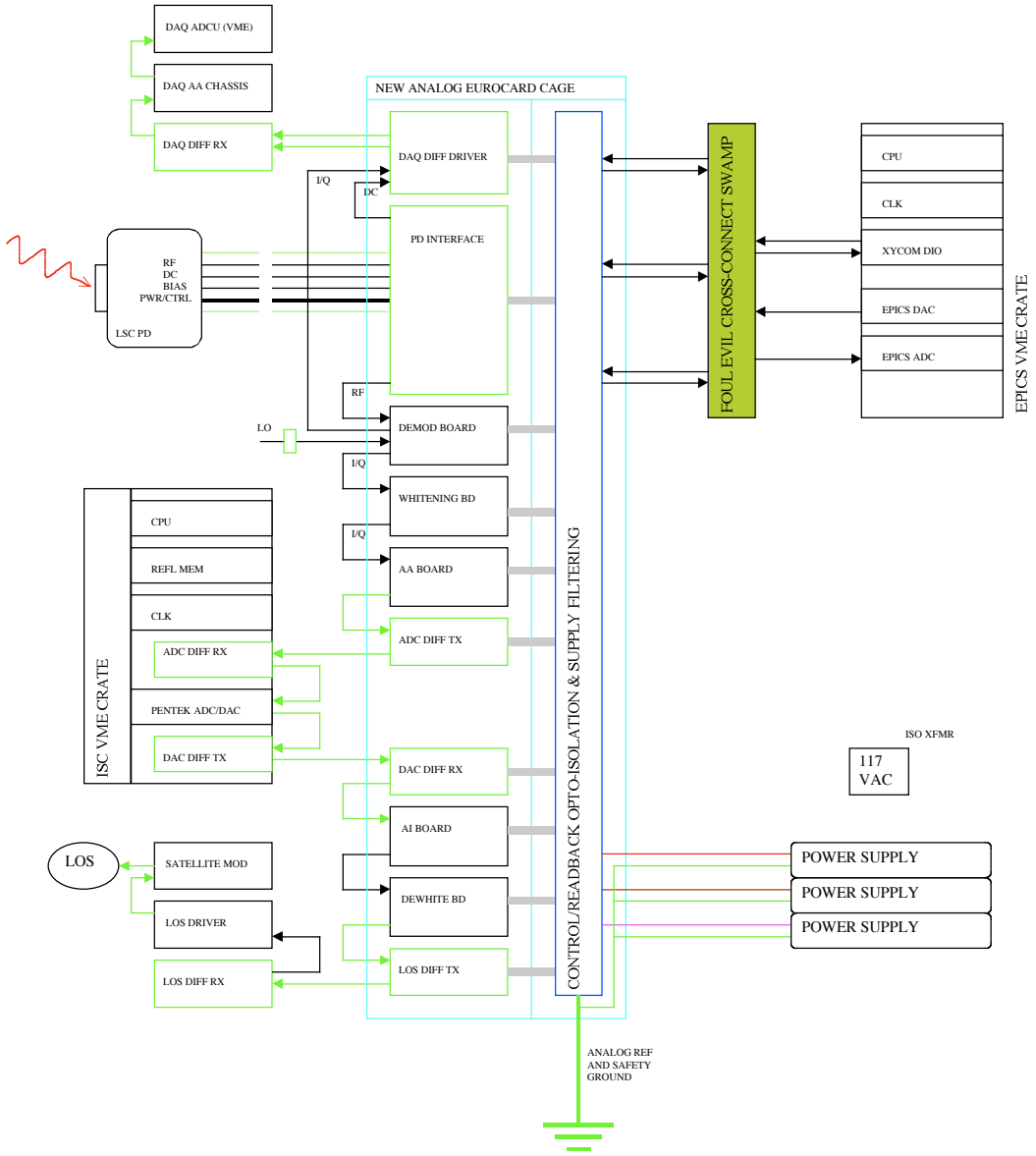

Figure 1 Schematic redeployment of LSC electronics and cabling (new or substantially modified components shown in color)

VME crates

Our current Knurr powered VME chassis are capable of improved RF containment by using their built-in EMC features to better advantage. The following measures will be taken:

- Install conductive blank panels in all open slots (this is also required for effective cooling, so should improve reliability)
- Install hinged, conductive overall front covers to enclose recessed wiring zone
- Insure rack bonding at a minimum of four front corners at front of crate, plus green wire at rear

- Shield all multiwire I/O cables and terminate shields on the front panel of the module they serve, with minimum exposed lead length
- Shield all inter-crate TTL clock cables and insure the shields are continuous and properly terminated at ends
- Sever and short to ground those conductors on multiwire cables which (through the manufacturer's stupidity) connect to internal module clock or bus signals
- Install RFI filters on external 5VDC supply entries; see below for other revised protocols affecting external power supplies.

LSC and ASC Eurocard Crates (and IO/PSL??)

Our primary objectives are:

- to implement Faraday shielding around all sensitive analog circuitry and wiring
- to eliminate DC and 60 Hz ground return paths other than the power supply connections, prohibiting "loops"
- to permit diagnostic isolation of all other conductive paths, such that the sum of all currents into any given device can be defined and accounted for
- to implement RFI mitigation on power supply forms and commons
- to isolate VME bus hash and clock noise from the analog circuits, and minimize its effect on the ADC and DAC
- to eliminate or minimize the cross section of exposed loop and whip antennas formed by "remote" sensor head connections
- to conductively AND radiatively isolate the cross-connect "antenna" system from any possible "receiver" circuit

New Crates:

All open analog/mixed signal Eurocard crates will be replaced by new, fully shielded crates. The number of crates is approximately 2 per IFO for LSC and 6 per IFO for ASC. PSL and IO controls crates are TBD, but probably add another 2 per IFO. The crates will have the following features:

- Eurocard crates will be recessed-front card cages with hinged, conductive front cover panels and options for remote ducted cooling and/or integrated DC fans.
- Chassis will be provided with optional means to isolate them electrically from the EIA mounting rack, or alternatively to electrically bond to the rack at a minimum of four corner mounting points.
- Full contiguous EMC Faraday shielding will be provided on all sides. Conductive surface finishes, finger stock gaskets, seam welding and/or multiple fasteners will be used on all panel seams and joints.
- Front panel wiring access will be guided from open troughs above and below each 6U cage.

- Conductive filler panels will be installed in all unused slots.
- An enclosed rear volume will be provided for backplane wiring, connectors and signal conditioning; this volume will itself constitute a separate shielded enclosure.
- External wiring to and from the cage backplane will enter the rear volume through a baffled plenum and/or bulkead connectors mounted in rear shield panel knockouts.
- A custom backplane will be provided consistent with existing and planned module functions.
- The backplane will incorporate a continuous groundplane to separate the rear volume and wiring plenum from the card cage volume.
- All backplane I/O signal and reference conductors will incorporate series RFI feedthrough traps (TBD), referenced to this groundplane, as close as practical to active P1 and P2 pins.
- These filters may be located on the backplane proper, or on "buddy boards" extending the P1 and P2 connector banks to meet field wiring at a secondary connector.
- The "buddy boards" may also be used to introduce optoisolators, isolation amplifiers, local voltage regulators, power supply filters or differential drivers/receivers as required to adapt or augment existing modules lacking these functions.
- The backplane will provide a single, star-connected analog ground point for the entire analog crate. If the crate is floated with respect to the rack, this star point will also connect the crate Faraday shield; alternatively if the crate is bonded the analog ground will be disconnected from the crate body.
- All DC power forms will route their commons through the crate analog ground star point.
- All DC power commons and bus connections will be sized such that they can be relied upon for safety ground in the event of a ground fault (e.g., sufficient to support sustained AC mains current that would trip the mains supply breakers).
- All DC power forms will enter the rear volume through RFI suppression feedthrough traps (TBD) mounted to chassis knockouts.
- Internal distribution of power forms will emanate from these feedthroughs via point-to-point wiring or printed backplane circuit traces.
- Additional DC power form filtering will be placed on the backplane and/or "buddy boards" to isolate pickup and crosstalk within the rear volume from each P1 and P2 connector pin, as for signal I/O lines.
- Power forms for analog Eurocard functions will no longer be distributed via the cross-connect; DC lines for each power form within a rack will be hard wired directly back to a dedicated supply (which will be placed remotely, see below).

Pentek 6102 I/O isolation:

The 6102 inputs are to be driven by balanced differential voltages, developed in a circuit entirely referenced to the analog Eurocard ground and power supply but physically

adjacent to the 6102 card in the VME crate. A minimum-length shielded ribbon cable (4 or 5 cm) will join each such module to its 6102.

RFI filtering (cutoff in the 100kHz range TBD) will be provided as close as possible to the 6102 I/O pins to trap remnant bus and clock noise, augmenting the anti-alias and anti-image filters.

Similarly, the DAC outputs will be sensed by differential amplifiers, again powered from the Eurocard end but phyhsically located in the VME crate next to the 6102. Variation in absolute potential of the DAC's ground reference will thus be subtracted out; the voltage transmitted downstream should then nearly represent the true output of the DAC with respect to its own reference pin.

Low-impedance balanced differential transmission lines to and from these local signal conditioners will be carried between VME and analog crates (about 0.5 to 1.5 meter distance) via twisted pairs within a common shield, with each pair also individually shielded to reduce crosstalk. The ground potentials of all the shields and the interface modules themselves will be defined at the analog crate end.

RF balun-type bifilar core traps will also be inserted between each 6102 channel and its differential driver or receiver, to insure that remaining induced currents are forced to be common-mode and face a high series impedance at RF frequencies.

The Pentek-adjacent driver and receiver will be fully encapsulated in Faraday shields, contiguous with the twisted pair cable shield and *floated from the VME chassis*. (This means the interface modules, while physically sitting in the VME crate, will be electrically considered "outposts" of the analog Eurocard crate). All signal lines will penetrate the shield via feedthrough filters (incorporated as part of the 'local' AA/AI filtering). All reasonable precautions will be taken to prepare these modules for life in an extreme RFI environment. Such measures may include, for example, secondary mu-metal shielding, multilayer sandwich ground planes, etc.

Sensor/photodetector head cabling and connectors:

All power supply and return, coaxial RF, control and high voltage leads for each sensor head (WFS, SPOB, LSC, etc.) will now be routed through an interface module, located in the Eurocard crate containing its corresponding demodulator and whitening board (this is already done for some, e.g., WFS). Power and EPICS controls should approach through this crate's backplane as below. No connection to any remote ground or other conductor will be permitted; all supply and signal currents going to/from the remote sensor must balance back at the crate interface.

Coax signals and individually twisted/shielded pair power and control lines will be bundled together in a common flexible braid, externally insulated. This external braid is bonded to the Eurocard interface module front panel and also to the sensor head body, such that an uninterrupted ground envelope (at Eurocard crate analog ground potential) is formed around all lines and the remote sensor head.

A custom mixed D-sub, similar to, e.g., common Sun RGB monitor cables (three 50-ohm mini coaxes plus 10 twisted pairs in a common DB-50 shell) may be an attractive alternative to homebrew bundled/shielded cabling.

High-voltage (50 and 100 V) bias for silicon detectors such as WFS and QPD heads will be provided by low-noise linear supplies, routed via the corresponding interface modules and Eurocard power conditioning facilities as detailed above.

EPICS and other non-power backplane IO :

While bypassing the cross-connects for power distribution is probably feasible, it looks impractical to eliminate the cross-connect functions for distributing control and monitoring points to and from the EPICS infrastructure. The EPICS VME crate itself and its IO modules have also been shown to be active RF and conducted emission sources. As a result, we adopt the approach of optically isolating all conductive paths to the cross-connects and EPICS crates at the analog backplane, augmented by RFI decoupling of EPICS I/O lines at the source, termination, and (optionally) cross-connect points.

Specifically, this strategy entails:

- Opto-isolators on all TTL I/O points near the point of entry/egress to the Euro backplane
- Optically coupled isolation amplifiers on all EPICS ADC analog signal readbacks
- Optically coupled isolation amplifiers on all EPICS DAC analog command voltages
- Shielding of I/O cables and local termination on the front panel of each module served (as opposed to pigtailing to a crate-wide common star point). (Note: What to do with shields at the cross-connect block ends remains TBD).
- RFI beads and decoupling caps at the VME front panel connectors for active EPICS I/O devices, if feasible
- RFI beads and decoupling feedthroughs or caps at the Eurocard cage ingress of each cross-connect wire (in addition to decoupling at the P1 and P2 pins on the backplanes; see above)
- RFI beads and decoupling caps on the cross-connect breakout blocks (where applicable).

Since the EPICS pin count is high, there is a strong motivation to find common groupings of these functions to economize on interface types. For example, one or a few general purpose “buddy board” designs might be able to support some number of analog isolation amplifiers (in each direction), some number of TTL optoisolators, and power form decoupling, with a customized mapping matrix to mate with the specific P1 and P2 pinouts serving a given analog module.

In some cases we may find it more cost-effective to modify a module design to incorporate the conductive isolation and filtering features rather than build an adapter, in which case a “plain” backplane interface would serve.

Although this is arguably the most engineering-intensive part of the program, there appears no other way to insure Kirkhoff’s law will fall on our side.

DAQ Feeds

In any remaining case where signals are currently pulled from the backplane directly to DAQ ADCU's (via cross-connect or otherwise) we propose to break these connections and route all DAQ channels via the front panel of an analog Eurocard differential driver in the originating analog crate. In cases where these signals currently run out of the backplane from a legacy card, the corresponding pins will be looped to the back of a new module sitting in the next slot, which will prepare the signals differentially and offer them to front panel connectors.

These differential twisted pairs will be organized to interface with the existing DAQ anti-alias filters per current practice. It remains TBD if the DAQ interface crate suffers from comparable contamination to the Pentek LSC/ASC crates; if so, it may be necessary to further upgrade the system to use the same suite of remote-powered differential driver/receiver modules as proposed for the input half of ISC converters.

Power supplies & safety ground:

There is a significant body of opinion that switch-regulated power supplies were not a good choice for a low-noise experiment hall. The obvious response, to simply substitute linear mode supplies, has at least two downsides besides the added cost; one is that the volume required for equivalent power is about double. Note, however, that for most DC power forms we are not using the full power capability of the Sorenson 900W units now installed; so on further analysis this may not be such a serious criterion. The other problem is that, while the insidious line-modulated 50-100 kHz and 1-50 MHz RFI will be reduced, the direct magnetic coupling at 60 Hz and harmonics is likely to be worse (and even tougher to shield against).

As a result it seems best to consider placing the DC supplies remotely, e.g., in the mechanical equipment rooms, and running heavy-gauge DC power cables out to the L/VEA racks. This has evidently been done on several high-energy experiments with good results. Substitution of linear supplies may still be warranted based on the conducted emission; this can only be evaluated fairly through experimentation, but it would be prudent to plan for the added cost and volume (if any) in case the substitution is required.

In this scenario we inherit some hard choices regarding where to tie the supply commons. We also take on some added responsibility for insuring personnel safety. The baseline we propose, TBR, is as follows (this is all independent of whether we ditch or keep the Sorenson switchers):

- Mount all DC power supplies in a new rack in the mechanical equipment room. If possible provide this rack with extra magnetic and electrostatic shielding to contain radiated emissions.
- Power each of the supplies from local "CDS" or "Clean" AC power via a dedicated isolation transformer, such that its ground pin (and hot and neutral for that matter) can float with respect to the local mains.
- Depending on how the supply is built, it may be necessary to tie the supply case to the green wire locally and float the outputs, or else it may be best to insulate each supply

from the rack and tie its case to its output common terminal which can now double as a safety ground (one or the other MUST be done!). The rack itself should be bonded to the local green wire.

- Size the DC output cables to accommodate the full rated breaker current of the mains supply circuit (this will probably be consistent with keeping IR drop reasonable for the higher-current forms).
- Run these cables out of the rack through bulkhead mounted high-current RFI/EMI feedthroughs.
- Twist each set of balanced power forms with its common, and sheath the bundle in an insulated braid for the run out to the L/VEA via the PSI cable trays.
- At the "consumer" rack, tie the DC supply commons for each form to the analog "star point" for each crate, and tie the power forms to their respective RFI feedthroughs for distribution inside the crate.
- Tie the "star point" to the L/VEA "consumer" rack's safety ground (green wire). This connection is the substitute for all those third prongs we lifted. If a power supply transformer shorts out, for example, the 117VAC hot will be connected through the DC common lead to this star point, to the rack ground, and thence back to the facility ground bus; this entire route MUST conduct cleanly enough to trip the breaker should this occur.

Inter-rack ISC analog signal transmission

Here we are mostly on the right track but need to improve and broaden the implementation. Adding some ad hoc differential driver/receivers to take ISC drive signals to LOS controllers and to the IO and PSL control rack made a significant improvement in 60 Hz and harmonics. However, these drivers and receivers are only pseudo-differential; the lines are not balanced, shields are not terminated and the receivers are not remote-powered or ground referenced to take full advantage of available common-mode rejection.

We will clean up the design for the Eurocard differential driver and build a mating receiver and cabling for all inter-rack analog transmission.

Coil driver & satellite module cabling

In principle the coil drivers should adopt the same treatment for power supplies and EPICS I/O as the analog Eurocard crates. How best to accomplish this (for both "analog" and new "digital" variants) remains TBD. It is conceivable that an optoisolated "buddy card" can be interposed between the IDC connectors on the LOS chassis and their existing cables.

Signal feeds from LSC and ADC dewhitening filters should conform to the differential drive/receive specifications detailed above, with the objective of no conductive path between the remote LOS or SOS drivers (which are powered independently on different voltages) and the Eurocard crate.

The wiring to the satellite modules should have its shielding tied at both ends such that the module itself is a floated outpost of the LOS or SOS driver chassis. The satellite modules will be mounted in a way that their isolation from the VE and cable tray grounds cannot be accidentally compromised (and also to prevent stress damage to cabling).

The wiring to the vacuum chamber feedthroughs will be tied at the satellite module end only and floated at the chamber (with insulated strain relief).

Implementation

The retrofit must be integrated without causing unacceptable losses to observing OR commissioning time in the short term (of course, in the long run the retrofit is expected to sharply reduce downtime in addition to improving performance). We will adhere to the following general rules:

- No upgrade step will be undertaken without prototype qualification and extensive bench testing of the underlying methods, as well as "dry run" installation practice.
- All upgrade steps will be integrated in a reversible way wherever feasible, to permit backtracking
- For each category of improvement (crate, cable, module) there will be a limited trial integration of one or a few instantiations, made on *one* interferometer. Expanding integration to other instances and to other interferometers will only be approved after this trial integration has proven successful[1].
- Upon qualification of an upgrade step, production and completion of the retrofit to each interferometer will be scheduled in accord with commissioning and observing timetables. In some cases it may be desirable to repeat the trial installation step for each subsystem on each interferometer, depending on initial experience.

Design development & prototyping

The following technologies will require some engineering development and prototyping investment. We expect these development activities to be distributed among the campus and observatory sites.

1. Analog Eurocard crate development, including:
    1. Crate mechanical design specification
    2. Backplane configuration, P1/P2 pin filtering, customizations to legacy boards
    3. Supply entry and filter design, star grounding

[1] Note: in this context, "success" does not necessarily require a measurable improvement in performance, just restoration of reliable operation without degradation. As a reminder, much of the plan requires complete conformance to the revised protocol to realize any benefit, and some benefits will not be apparent before future noise reductions render them visible.

4. Wiring plenum mechanical arrangement
5. Analog isolation amplifier selection for EPICS analog I/O
6. Digital optiosiolator selection for EPICS TTL I/O
7. "Buddy card" generic design and customization to existing board functions

2. Bundled ISC/IO/PSL sensor head cable shielding and/or integrated hybrid cable development
3. Eurocard/VME crate front panel shield connection mechanics
4. Power supply remoting, inc. safety grounding, isolation transformers, rack format & mechanical design
5. Differential analog signal transmitter/receiver/cabling design revision
6. Pentek isolation module suite integration testing
7. DAQ analog isolation design (if required)
8. Back-end (DAC to coil) shielding and signal transmission design & test

Phasing and resource commitment

For the moment we assume a continuous level of effort comprising about 2 FTE's, distributed as follows: about 1 FTE experienced EE (probably spread between 2 individuals, at least one resident at the "guinea pig" site); 1/2 FTE experienced IFO instrumentation scientist (Zucker, Weiss, Fritschel, Sigg, or ?); and 1/2 FTE junior engineers with experienced technical assistants. This will be approximately doubled by addition of commissioning and site staff during episodes of actual installation and field testing.

As a strawman, the following initial sequence is proposed for what are arguably the most invasive steps, the revisions to the analog Eurocard system and remoting of DC supplies. At this point no attempt was made to interleave with the science and commissioning schedules, and the choices of guinea pig interferometer (L4k) and trial instantiations are arbitrary. In actual practice, a Project plan will be established and linked with the commissioning schedule to interleave planned activities with minimum interference.

A. Crate design and prototype fab (10 weeks)
    a. Crate vendor survey & procurement
    b. Backplane specification & procurement
    c. EPICS isolation design, buddy card fabrication
    d. Pentek isolation fabrication (in progress)
    e. DC supply remoting test (standalone with dummy loads & field cabling)
B. Shop test of prototype LSC crate using spare boards (4 weeks)
C. Integration test of 1 crate instance on working IFO (L4k 1x9??) (1 week)

D. Test review (1 week)
E. Revision to protocol & designs (4 weeks)
F. Integration of revisions & retest on IFO (1 week)
G. Infrastructure installation for remote DC supplies in L4k LVEA (4 weeks)
H. Trial cutover to remote supplies and L4k IFO test (1 week)
I. Test review (1 week)
J. Production fab for full L4k retrofit all stations (10 weeks)
K. L4k retrofit and test, all stations (4 weeks)
L. Test review (1 week)
M. Production fab for H2k and H4k (may be concurrent with J.)
N. H2k retrofit and test (4 weeks)
O. **Test review (1 week)**
P. H4k retrofit and test (4 weeks)