LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

-LIGO-

CALIFORNIA INSTITUTE OF TECHNOLOGY

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Document Type	DCC Number T010152-A-C	December 18, 2001
Proposed LIGO VME DAC Specifications		
J. Heefner		

Distribution of this draft:
This is an internal working note of the LIGO Laboratory

California Institute of Technology
LIGO Project – MS 18-33
Pasadena, CA 91125
Phone (626) 395-2129
Fax (626) 304-9834
E-mail: info@ligo.caltech.edu

Massachusetts Institute of Technology
LIGO Project – MS 20B-145
Cambridge, MA 01239
Phone (617) 253-4824
Fax (617) 253-7014
E-mail: info@ligo.mit.edu

www: http://www.ligo.caltech.edu/

Proposed LIGO VME DAC Module Specifications

1 Introduction

The specifications that follow are for a VME based Digital to Analog Converter (DAC) module to be used in the real-time servo controls for the Laser Interferometer Gravitational Wave Observatory (LIGO).

2 Physical Characteristics

2.1 Module Size/Dimensions

Standard 6U VME, single slot module

2.2 Number of Channels per Module

The number of channels per module shall be 8.

2.3 Input Connectors

The input clock connector is TBD. The analog input connector is TBD.

3 Electrical Characteristics

3.1 External Clock Input

The external clock input sh**a**ll be differential, TTL compatible, and optically isolated.

3.2 Voltage Range

The output voltage shall be +/- 10V.

3.3 Analog Output

The analog outputs shall be differential capable of driving a 500 ohm load full scale. The 3 dB bandwidth shall be greater than 50KHz. The output impedance shall be 50 ohms.

3.4 Glitch Energy

The glitch energy of each output shall be less than 5nV-sec.

3.5 Output Referred Noise

The output-referred noise of a single channel shall be less than 100nV/√Hz for frequencies greater than 40 Hz and less 8192 Hz for a sampling frequency of 16384 samples per second. While this is the requirement for the noise, LIGO would like to have an output voltage noise goal of 30nV/√Hz. This measurement is made by outputting a full-scale sine wave and measuring the output noise floor of the channel using a dynamic signal analyzer. This requirement is a “broadband” average of the output noise in which line and harmonic spikes can be ignored, but in all cases the magnitude of the spikes shall be attenuated by at least 100 dB from the reference sine wave magnitude.

3.6 Output Setting Time and Pipeline Delay

The output settling time shall be less than 5 microseconds, measured from the output clock edge. The measurement of the settling time is from the time that a full-scale change has been requested to the time that the output voltage has settled to +/- 1% of its final value.

3.7 Anti-Image Filtering

The requirements for anti-image filtering are TBD and may be provided by LIGO on a separate module.

3.8 Channel to Channel Cross Talk

Inter-channel crosstalk shall be less than –90dB for frequencies less than 50KHz.

4 Sampling Characteristics

4.1 Sample Frequency

The sample frequency shall be 2048 to 16384 samples per second, externally clocked. The actual clock provided to the module will be 2^{22} Hz. The module will provide for programmable dividers that give sample frequencies of 2048, 4096, 8192 and 16384 samples per second. All channels on a module will have the same sample frequency.

4.2 Sample Storage

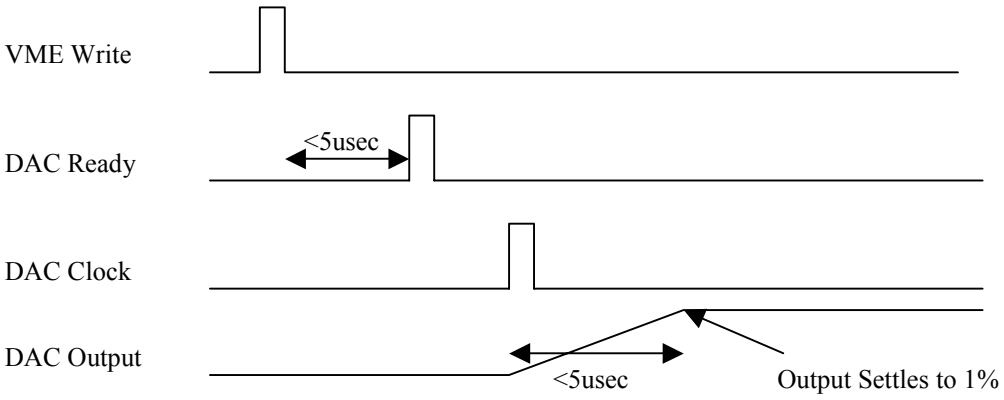
The module does not need to have any on board storage beyond a single sample per channel.

4.3 Number of Bits

The number of effective bits is TBD, but shall be sufficient to meet all noise requirements.

4.4 Pipeline Delay

The pipeline delay shall be less than 5 microseconds. The pipeline delay is measured from the VME write to the channel to the time that the data is available to clocked out. The timing diagram below illustrates the pipeline delay and settling time specification in relation to each other and the DAC clock.



4.5 16-Bit Data Write

In the 16 bit data write mode, the data for each channel shall be written in a 32 bit "packed" format to consecutive registers. Packed format is defined as two 16-bit channels per 32 bit word. The lower number channel shall occupy the lower 16 bits and the higher number channel shall occupy the upper 16 bits.

	16 bits	16 bits
Address N	Channel 1	Channel 0
Address N+1	Channel 3	Channel 2
Address N+2	Channel 5	Channel 4
Address N+3	Channel 7	Channel 6

4.6 Full Number of Bits Data Write

In this data write mode, the data for each channel shall be written in 32-bit format to consecutive registers. Each 32-bit word shall contain the data for one channel.