LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

-LIGO-

CALIFORNIA INSTITUTE OF TECHNOLOGY

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Document Type	DCC Number	December 17, 2002
	T020196-00-C	
Timing of CDS 16KHz Digital Control Systems		
R. Bork		

Distribution of this draft:
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California Institute of Technology
LIGO Project – MS 18-33
Pasadena, CA 91125
Phone (626) 395-2129
Fax (626) 304-9834
E-mail: info@ligo.caltech.edu

Massachusetts Institute of Technology
LIGO Project – MS 20B-145
Cambridge, MA 01239
Phone (617) 253-4824
Fax (617) 253-7014
E-mail: info@ligo.mit.edu

www: http://www.ligo.caltech.edu/

1 Scope

The scope of this document is to describe the timing and synchronization of LIGO CDS Digital Control Systems (DCS), in particular those subsystems that operate synchronously at 16384Hz. These DCS include the Length Sensing and Control (LSC) and large optics controllers of the Digital Suspension Controls (DSC).

The following description includes:

- Overview of common hardware and software installed in the DCS to provide timing and synchronization.
- Timing diagnostic software
- Subsystem timing measurements

Note that specifically excluded from any timing measurements stated in this document are:

- Time delays resulting from input and/or output hardware filtering, such as whitening and dewhitening filter modules.
- Time delays associated with user specified digital filters in the DCS servo loops.

2 Overview

The LIGO CDS system employs a distributed architecture of VME based subsystems for purposes of interferometer (IFO) control and data acquisition. These CDS subsystems operate at either 16384 or 2048 Hz. To effect proper control and data acquisition, certain timing and synchronization requirements are imposed on them. Among these requirements are:

- All ADC channels triggered and sampled to an accuracy of +/- 10usec relative to an absolute time source.
- All 16KHz CDS subsystems synchronous to each other such that any and all data outputs computed by one CDS controller within one 61usec cycle is available to any and all other CDS controllers prior to their use in the next 16KHz clock cycle.

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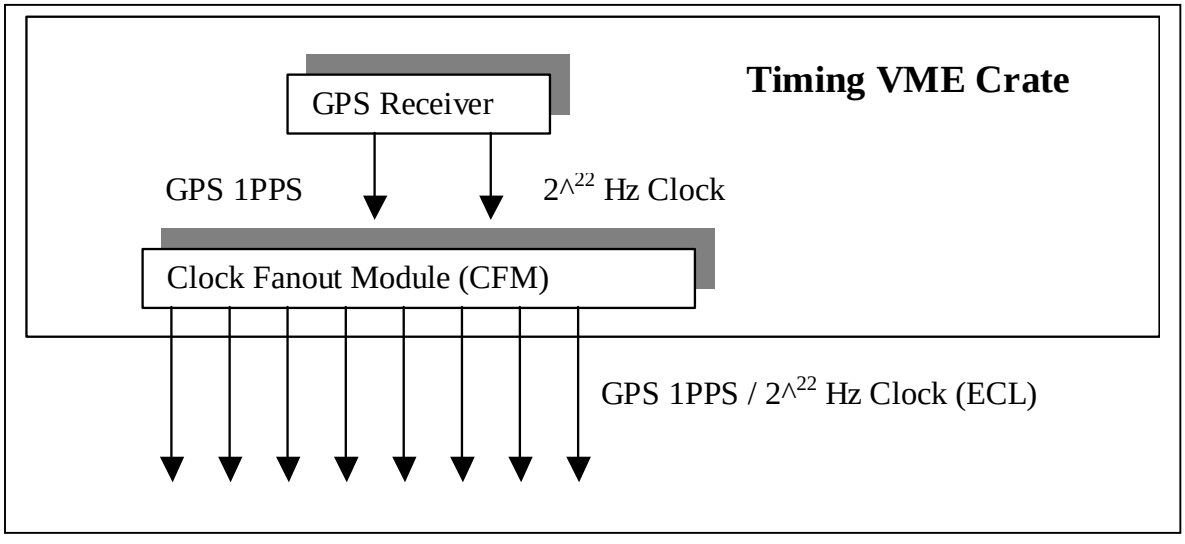
An overview of the CDS timing system used to achieve these requirements is shown in the following diagrams and further described in the following subparagraphs.

2.1 Timing System VME Crate

In order for LIGO to operate, various CDS systems need to be synchronized to each other and to absolute time. For this purpose, all synchronized CDS DCS are connected to Global Positioning System (GPS) driven timing systems. The hardware involved in the timing system consists of a number of VME modules, as shown in the following diagram. These modules are discussed in the following subsections.



2.1.1 GPS Receiver Module

The GPS receiver module employed by CDS was developed commercially to LIGO specifications. This module receives and decodes signals from GPS satellites and provides 1 PPS (1 pulse-per-second) and 2^{22} Hz clock signal outputs. The 2^{22} Hz clock is phase locked to the 1 PPS on the GPS receiver board. GPS receivers are located at each end/mid station, one for each IFO in the LVEA, and one in the Mass Storage Room (MSR). Both the 1PPS and 2^{22} Hz clock are available as outputs on the receiver front panel.

2.1.2 Clock Fanout Module (CFM)

The outputs of the GPS receiver are connected to a GPS Fanout Module (D980362-02) designed by LIGO. The function of the GPS Fanout Module is to provide for eight 4 pin LEMO outputs that each contain the 1 PPS and 2^{22} Hz clock signals. Signals output from the GPS Fanout Module, which are differential ECL, then are distributed to CDS DCS and Data Acquisition (DAQ) VME subsystems.

2.2 CDS DCS VME Crate

Each DCS VME crate contains timing modules, Analog to Digital Converters (ADC), and Digital to Analog Converters (DAC) , as shown in the following figure. (Note: Of the 16KHz DCS, only the End Test Mass (ETM) DSC contain the sigma-delta type ADC). Descriptions of the timing hardware are given in the following subparagraphs.

2.2.1 Clock Driver Module

The Clock Driver Module (CDM) provides the following functions:

- Receive the 1PPS and 2^{22} Hz clock signals from the GPS fanout module via a front panel, 4 pin LEMO connector.
- Under software control, output the 1PPS and 2^{22} Hz clock via a 4 pin LEMO output connector. These signals are fed to the Variable Delay Timing Module.
- Under software control, provide clock and control signals to CDS sigma-delta type ADC modules via a 20 pin front panel connector. (Note: Of the 16KHz DCS, only the End Station large optics controllers use this type of ADC and only for optic sensor inputs.)

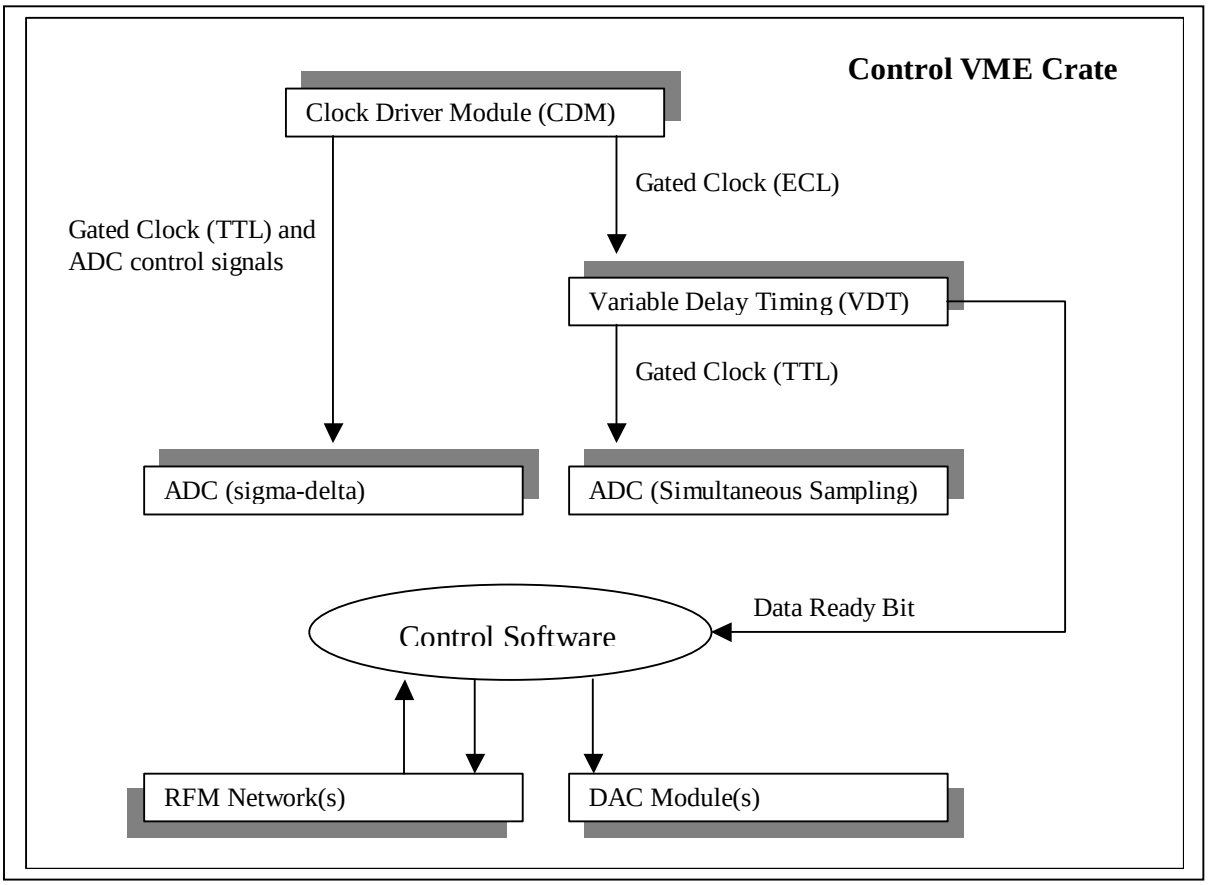
Essentially, when armed or disarmed by the DCS software, this module will start/stop the output of the 2^{22} Hz clock synchronous with the GPS 1PPS pulse.

2.2.2 Variable Delay Timing Module (VDTM)

The Variable Delay Timing Module has three main functions:

- Provide the 2^{22} Hz clock to the DCS simultaneous sampling ADC module clock inputs. This is a straight feed through of the clock from the CDM, simply converting ECL input to differential TTL output via a 2 pin LEMO connector.
- Provide a software programmable delayed clock at the fundamental sample frequency (16384 or 2048) to the DCS DAC modules.
- Provide a software programmable delayed VMEbus interrupt or polling bit that can be used in lieu of polling the status of the DCS ADC modules. This is desirable because it has been discovered

that polling or reading the DCS ADC modules during conversion causes the input referred noise of the devices to increase.



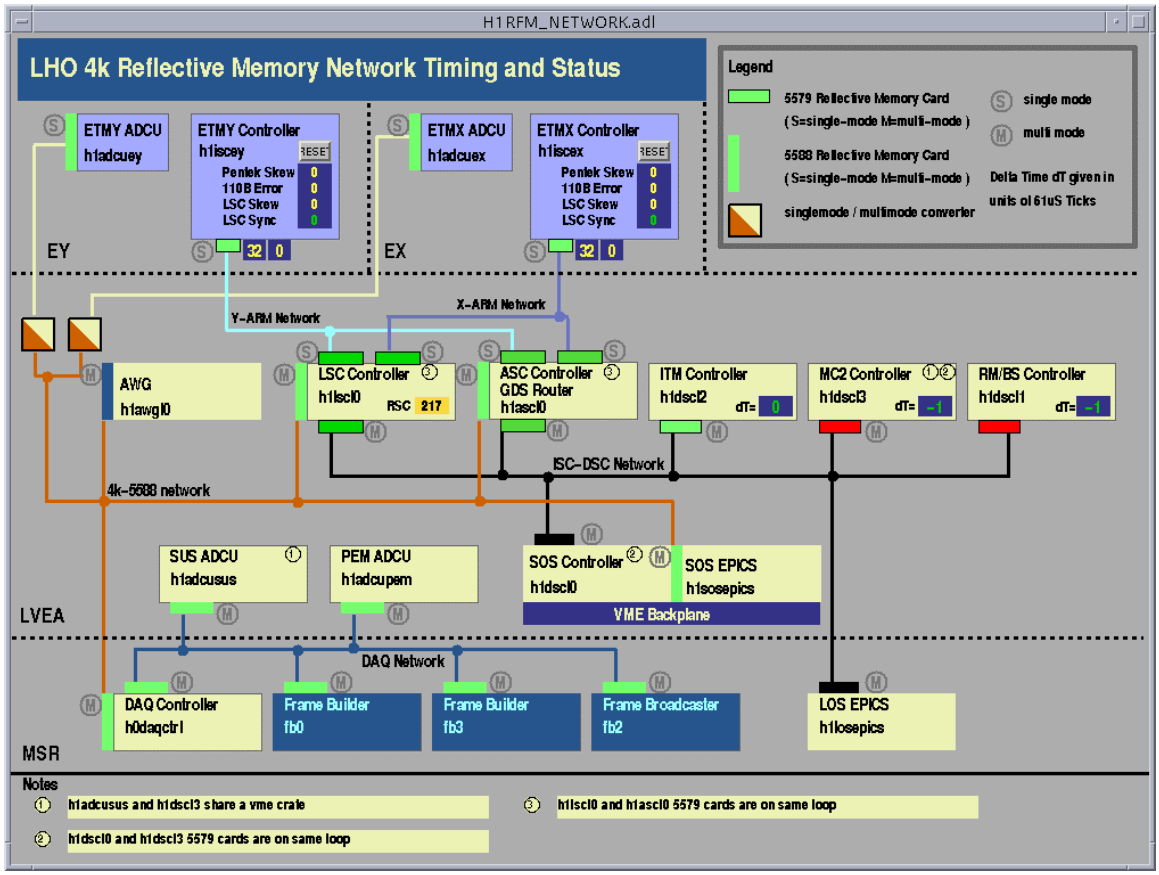
3 DCS Startup Synchronization

3.1 Overview

The following MEDM screen shot from the LHO4k interferometer shows the CDS control and DAQ subsystems and network interconnections. DCS shown are:

- LSC Controller
- ASC Controller
- DSC Controllers (ITM, MC2, RM/BS, SOS, ETMX, and ETMY Controllers)

All of these controllers are Multi-In, Multi-Out (MIMO) control systems, which must operate in close synchronization with each other. With the exception of the ASC and SOS controller (2048Hz), these subsystems operate at 16384Hz. The driving force of the 16KHz requirement is the LSC controller. The LSC must sample its inputs, run its control algorithms, and output resulting control signals to the DSC controllers, via the CDS reflected memory networks, in time for the DSC controllers to use the LSC control signals in their control algorithms prior to finally outputting signals to the various optics.



3.2 Startup Synchronization

CDS controllers, and their associated software, are synchronized internally by their ADC modules, which are in turn slaved to the GPS clocks. The synchronization of these ADC modules is achieved by starting their sampling clocks (the GPS 2^{22} clock) in coincidence with the GPS 1PPS pulse. The CDM provides for this startup synchronization.

The typical startup sequence of controllers is:

- Initialize ADC modules
- Initialize reflected memory connections
- Initialize interface to EPICs processors, including loading digital filter coefficients.
- Bump control task to highest priority on controller CPU (avoids competition for CPU time from any other vxWorks tasks, such as telnet)
- Lock VME bus access (avoids bus arbitration delays, thereby reducing I/O time).
- Arm ADC/DAC modules.
- Arm the CDM. The CDM, in turn, will enable clocks to the ADC modules synchronous with the next GPS 1PPS pulse.
- Begin polling VDTM module for “ADC data ready”

After the VDTM indicates that ADC sampling should be complete, the code goes into a continuous loop, at either 2048 or 16384 Hz:

- Read ADC inputs
- Read sensor/control inputs sent via RFM networks
- Perform control algorithms
- Output calculated control signals to RFM networks for use by other controllers and/or directly to DAC outputs.

- Output DAQ and GDS signals to DAQ network.
- Communicate operator inputs/outputs via VME backplane or RFM network to EPICS interface processor.
- Read in any active GDS excitation signals for application on next cycle.
- Return to polling VDTM for next ADC data ready.

3.3 Controller Internal Synchronization

Controller software is synchronized by being slaved to the ADC hardware, ie software will run through its control algorithm each time its ADC module indicates data ready. Data ready is determined by the control software by polling the VDTM until its data ready bit is set. Polling of the VDTM, over other possible schemes, is done for the following reasons:

- Polling the ADC module directly for "FIFO Not Empty" resulted in added ADC sampling noise.
- Having the ADC module initiate a VME bus interrupt on data ready had two problems: 1) Interrupt Service Routine (ISR) latency of 5-10usec in the controller CPU, which is significant in a system which has a total 61usec processing window, and 2) the particular ADC modules being used will not initiate a VME bus interrupt until the second sample, which results in intolerable phase delay.

It is item 2 in the last bullet that is also the reason the ADC modules are synchronized and driven as they are ie applying and removing the ADC clock instead of a more typical scheme of running the clock at all times and then starting acquisition via a trigger signal. These particular ADC modules, when started by using the external trigger, will not have data ready until the second sample.

This results in a couple of startup synchronization problems. The first is the synchronous start of the ADC clock with the GPS 1PPS. This is accomplished by the CDM. The second problem is controlling the actual sample and hold time (<4usec) of the ADC within the 61usec window. The ADC clock is the GPS 2^{22} clock, which must be down counted within the ADC module to provide the required 16384Hz sampling rate. This clock must be running during ADC module initialization, and then is turned off, via the CDM, prior to startup synchronization. However, when the clocks are removed after initialization, there are no ADC module registers which allow one to either reset this internal downcounter or to read its value. Therefore, if one now applies the GPS clock on startup, the actual ADC sample can occur anywhere within the 61usec window, instead of immediately at the start.

To minimize this timing uncertainty, a software module, run during initialization, estimates when the ADC will actually sample ie down counter is about to trigger ADC and then removes the initialization GPS clock by turning off the CDM. In this manner, when the clock is reapplied at startup, synchronous with the GPS 1PPS, the ADC should trigger immediately. Testing of this estimation code has shown +/- 1usec accuracy.

Timing of outputs from CDS controllers, be it digital via RFM or analog via DAC modules, is set by the software processing time. With the latest design of VDTM, the DAC outputs will be clocked in synchronization with the GPS system at a software selectable time. In the interim, to maintain as constant as possible time between the beginning of a 61usec cycle to the controller output, the software compute time is maintained as constant as possible. A couple of things are done to accomplish this. One is to lock the control task at the highest priority and locked in cache. Second, the code takes over VME bus ownership , to control VME bus I/O timing. Finally, all digital filter calculations and other algorithms, such as LSC lock acquisition, are computed each cycle, whether they are selected to play a part in the output or not. In various timing tests, code timing in control systems is typically constant +/- 1usec.

Code timing, however, is affected by the addition or deletion of digital filters. All CDS controllers provide the capability for users to add/remove digital filters via the controller filter configuration files while the system is running.

3.4 CDS Inter-Subsystem Synchronization

With all CDS controllers synchronized to GPS, and therefore to each other, the remaining task is to ensure that data transmission is synchronized between the various digital controllers. The requirement here is that control signals computed or sensor signals input by one controller on one 61usec cycle reach any and all other controllers that require this information for their calculations prior to the next 61usec cycle (Note: this pertains only to controllers operating at 16KHz). The key subsystems constrained by this requirement are the ETM controllers, which must send QPD input signals to the LSC controller at the LVEA and the LSC controller, which must transmit computed control signals to all DSC crates. The additional burden on both the ETM and LSC controllers is there physical separation from each other (4km). Given the speed of light, transmissions from one to the other are already delayed ~13usec in transit.

All signals between controllers are passed digitally. The data transmission media are three separate real-time RFM networks. One network interconnects the controllers within the LVEA and there is one network dedicated between each end/mid station controller and the LVEA controllers.

4 Timing Diagnostics

Various diagnostics are built into the CDS controllers to verify timing and synchronization . These are discussed in the following subsections

4.1 Absolute Timing Diagnostic

Absolute time accuracy is measured by injecting a ramp signal, triggered by the GPS 1PPS signal, into an ADC channel of various data acquisition subsystems and into the LSC control system. This ADC readout is then sent to the DAQ system for recording and monitoring by a diagnostic running on a DMT machine. This diagnostic, TimeMon, then uses this ramp signal to determine a subsystems deviation from the GPS 1PPS. The time deviation calculation is recorded in trend frames, available to the DAQ and viewable with the Dataviewer and is also available directly through a DMT web page.

4.2 Controller internal Diagnostics

4.2.1 CPU Meter

Each controller provides a CPU meter, which is displayed on controller MEDM screens. The value is an estimate of the time that it takes for the CPU to complete all of its computations and I/O within a 16384Hz or 2048Hz timing cycle. The value displayed on the meter is the longest such time measurement within a one second period. This time estimate is accurate to +/- 3usec.

The time displayed is a measurement of time from ADC ready until the process has completed all of its tasks for that cycle and has gone back to polling for ADC ready. This time includes reading in data, control algorithm processing, control signal outputs, and “housekeeping”. Housekeeping includes data acquisition, GDS signal I/O, and operator communications via the EPICS processor.

The primary diagnostic provided by this reading is whether or not the software is taking too long to complete its cycle, and therefore not ready for the next cycle on the next time mark.

4.2.2 VDTM to ADC Module Timing Variations

The basic controller timing scheme involves polling of the VDTM data ready bit. This bit should set at the same time as the ADC sample is ready for readout. As soon as the controller software sees the VDT bit set, it reads the ADC module status register to verify that data is actually ready. If the ADC module indicates that data is not available, the software will continue polling the ADC module until data is ready. A counter within the controller software will then record the number of these polls required. This diagnostic should always read zero in a properly operating system. A value of other than zero (~750nsec per count) can indicate either a timing drift between the VDTM and the ADC module, or a fault in the ADC initialization software which sets up the ADC downcounter to trigger the ADC sample immediately on startup.

4.2.3 Resync Counter

The software within a controller automatically detects if it has fallen behind by one or more processing cycles. This is detected by the fact that the ADC FIFO is not empty after an ADC read cycle. The controller software then resynchronizes itself and continues operation. The number of times that a controller missed a time mark and resynchronized is maintained in a counter, the value of which is sent to an EPICS display screen and recorded by the data acquisition system. This counter is only reset when the controller is rebooted.

4.3 Inter-system Timing Diagnostics

All 16KHz CDS DSC controllers have diagnostics for checking relative timing between themselves and the LSC controller . Each controller maintains a cycle counter (0-16383), which is reset once per second. This counter is used internally for determining when various housekeeping tasks are to be scheduled. The cycle counter value is also transmitted to the RFM networks. The DSC controllers will transmit this value on each cycle immediately after reading the ADC modules. The LSC controller will transmit its cycle count immediately after transmitting its computed control signals to the DSC.

4.3.1 LSC Controller Inter-system Timing Diagnostic

After the LSC controller completes its control algorithm processing, it will check the cycle counts transmitted by all the DSC controllers. Since the DSC transmitted their cycle count at the start of their processing cycle, the cycle count should have been received by the LSC by the time it performs its check. The DSC cycle counts should match the LSC internal cycle counter. The difference between cycle counters is displayed in an MEDM screen and recorded by the DAQ.

4.3.2 DSC Inter-system Timing Diagnostic

The DSC controllers compare their cycle count with the cycle count transmitted by the LSC controller on every cycle. Since the LSC transmits its cycle count after it transmits its control signals to the DSC, it allows the DSC to verify that data from the LSC has arrived in time for use in its control calculations. The DSC maintain an internal counter whose value is the number of times that the LSC signal did not arrive on time within a one second period. This value is passed to the EPICS processor for display on operator screens and recording by the DAQ system.

5 Timing Tests

Recently, timing tests were conducted both at LHO and LLO. The primary scope of these tests was to determine:

- Absolute timing of the LSC controller.
- Processing times within the various controllers

- Accuracy of ADC timing initialization software
- Inter-system synchronization and data delays

5.1 Absolute Timing

Using the TimeMon DMT software, the absolute timing accuracy of the LSC on both the LHO2k and LHO4k was measured at +/-1usec compared to the GPS 1PPS.

Note: Between the ramp signal output from the CDM and the LSC ADC input, there is a switchable anti-aliasing filter. If this filter is on, it introduces a 95usec delay (measured with a scope between LSC whitening filter input and output). This will result in a TimeMon DMT reporting error of –95usec.

5.2 Processing times

Digital filter Second Order Section (SOS) and overall DSC control loop processing times were made on the various 16KHz DCS. The results of these tests are listed in the following subparagraphs.

5.2.1 Digital SOS Filter Processing

The number of SOS defined in the DSC digital filter banks affects the overall processing time of the DCS. Timing tests were performed on the LSC controller (1.2GHz Pentium) to measure the time required to calculate a single SOS. The results of this measurement show that each SOS takes ~53nsec to compute.

5.2.2 Individual DCS Control Loop Processing

For the control loop processing measurements, the times listed are meant to be "representative". That is to say, the measurements were done with the DCS filters defined in the system at the time the measurements were made. These times can therefore vary dependent on the number of filters defined in a DCS.

In the following list of timing numbers, two values are given for each DCS:

1. Control algorithm processing time. This is the time from "ADC data ready" until the DCS processes this data and provides an output, either to RFM or DAC. These tests were done using two methods. One was with a VME bus analyzer, measuring times from ADC ready to DAC output sent on the VME bus. The other was to inject the GPS 1PPS into an ADC input, direct this signal thru the DCS control filters/algorithms, and finally output the signal to a DAC channel. The GPS 1PPS was also connected to one channel of a scope and the DAC output to a second channel. With the scope triggered by the 1PPS signal, the time difference was measured to the 1PPS signal appearing at the DAC output. Note that no digital filters were turned on during the tests, the GPS 1PPS was injected directly at the ADC input, and the output measured directly at the DAC module output. Therefore, no attempt was made to measure timing delays which may be introduced by whitening/dewhitening hardware or specific digital filters.
2. Total processing time. This time includes the control algorithm processing time plus the DCS "housekeeping" tasks. The latter includes:
   - Writing data to the DAQ system
   - Reading/writing operator interface information to the DCS EPICS processor, either across the VME backplane or, in the case of large optic DSC, via RFM. Typically, the DCS commute one value to the EPICS CPU each 16KHz cycle, with all input/output values updated at 16Hz.
   - Processing various system diagnostics.

Since the number of such housekeeping tasks can vary slightly from one 16KHz cycle to another, the time listed is the longest cycle processing time over a one second period.

Not included in the total processing times given below is the time required to process Global Diagnostic System (GDS) signals ie no GDS signals were active at the time these measurements were made. Typically, an additional 1usec is added to the total processing time for each active GDS signal. Note that the control loop processing times are not affected by the GDS signals.

5.2.2.1 Processing Time Measurements

	LSC	LVEA LOS Controllers	ETM	MC2
Control Algorithm Processing Time	31usec	42usec	26usec	20usec
Total processing time	46usec	56usec	45usec	27usec

5.2.2.2 Processing Time Variations Noted During Testing

During testing at both LLO and LHO, several processing time variations were noted, as captured by the LSC CPU meter diagnostic and the LSC Resync Counter diagnostic.

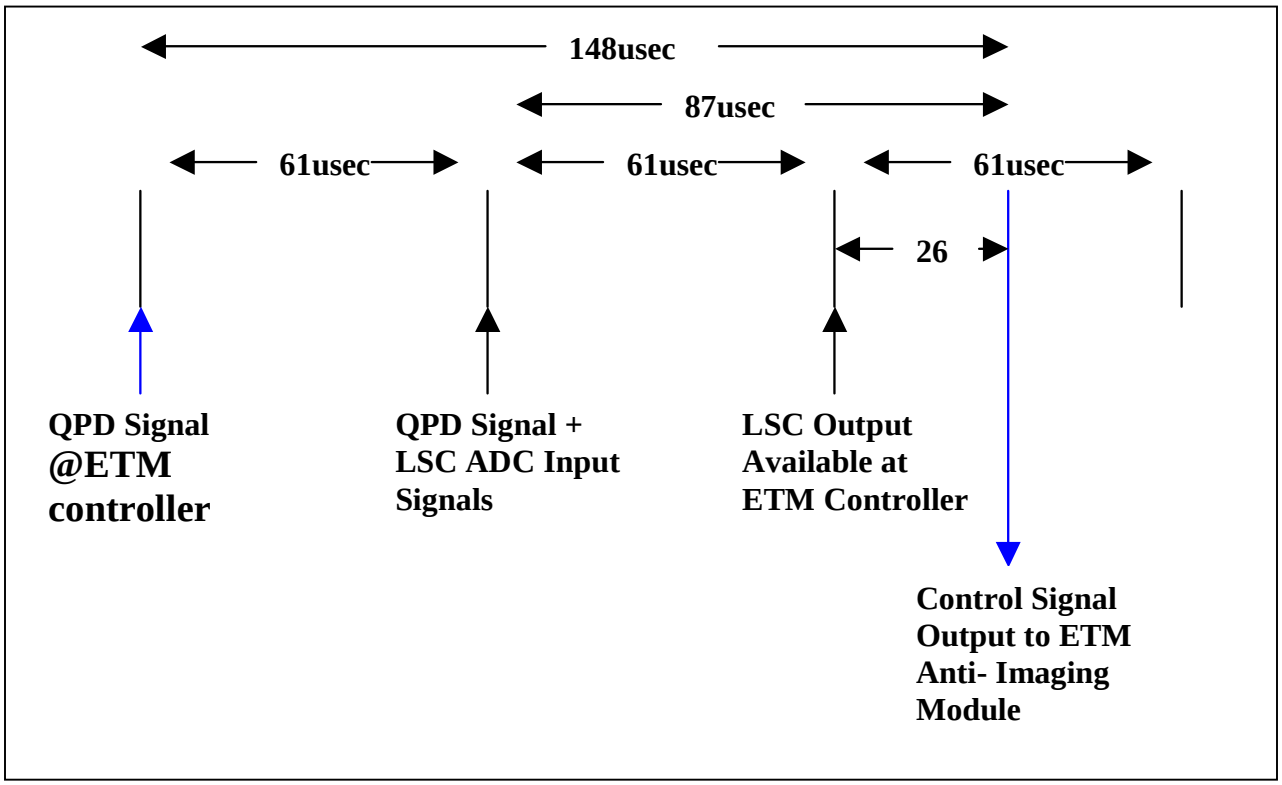
First, at LLO, it was noted that the total processing time, as shown by the LSC CPU meter, was continuously running too long after only a few GDS signals were added, and, overall was always indicating higher than the LSC meters at Hanford. This was traced to a DAQ RFM network problem. It turned out that both end station DAQ data collection units (DCU) were configured for the maximum data rate and both configured identically. Therefore, every $1/16^{th}$ of a second, they would dump their data to the DAQ RFM at exactly the same time. This was enough instantaneous traffic on the network to fill the LSC controller's FIFO, thereby slowing down the LSC's ability to write its data to the network for 3-4 cycles every $1/16^{th}$ of a second. Since the LSC is the only 16KHz system directly connected to the DAQ network, it was the only unit affected by this data flooding. For now, the problem was resolved by configuring one of the end station DCU for less data, thereby not having both end stations dumping their data at the same time.

The second problem was noted at LHO by the Resync Counters on both the LHO2k and LHO4k LSC systems. As described previously, this diagnostic counts the total number of 61usec cycles that the LSC missed and had to catch up, or resynchronize itself. Over the five day test period, the LHO2k is showing 99 counts and LHO4k 191 counts. Through observation, for lack of a known DAQ channel to correlate against, this again appears to be a problem where the RFM network FIFO overflows and the LSC is delayed in its ability to write data onto the network. Playback of trend data indicates that when this occurs, it is not a slow trend, but rather significant jumps of missing up to 100 cycles at a time. This was observed to occur primarily, though not always, when an LVEA large optic controller was rebooted. When this occurs, the LOS EPICS processor sends a fair amount of traffic on the network in the form of filter coefficients as the large optic controller comes back on line. Again, further investigation will be required to track the problem and correct it.

5.2.3 Overall LSC Loop Timing

Given the above processing times, an overall LSC loop timing diagram is shown below. The time period covered is 183usec, or three 16384Hz cycles. What it shows is that if a QPD signal is read in, at time 0, or left end of diagram, its contribution to the LSC control signal will be output by the ETM controller DAC 148usec later. Likewise, signals read in directly by the LSC via its ADC inputs will be reflected in the ETM controller output 87usec later. To reiterate, these times do not include any delays due to input signal

whitening filters, digital filters in the DCS processors, or output signal conditioning. These times are strictly ADC input to DAC analog signal output.



5.3 VDTM to ADC Synchronization

As of the time of the document, the VDTM/ADC timing diagnostic, described in paragraph 4.2.2 above and shown on the Timing MEDM screen as “Pentek Skew”, has been running for 5 days on the LHO interferometers and outputs recorded by the DAQ system. The dataviewer trend plots are shown in the following figures. Note that the vertical scale on these plots should be 750nsec, not 61usec as shown.

Trend plots over these 5 days for the LHO2K DSC show no more than 1 count (750nsec) variation between the VDTM polling bit ready and ADC FIFO ready. The LHO2K and LHO4K LSC controllers showed no variation for ~4 days, but the diagnostic is showing fluctuations between 0 and 1 count (750nsec) over the past 12 hours, which may indicate a slight drift trend.

For the LHO4K, the trend plots are basically flat for the ETM DSC. However, the large optic DSC in the LVEA indicate large variations.

From the plot, it can be seen that both the RM/BS and MC2 controller diagnostics gradually drifted up, until they hit a maximum where, in essence, the VDTM polling bit was being ignored, and all timing was done by polling the ADC module. In the case of MC2, it looks like it eventually recovered and has begun another drift cycle. During this time period, the diagnostics (LSC Synch and LSC Skew), which measure synchronization differences between the LSC and DSC, showed no errors. This indicates that the systems were still synchronous to the extent that data transmitted between systems was still on time.

The diagnostic results could indicate either a bad VDTM or cabling problem between VDTM and the ADC clock input. The MC2 controller VDTM module is up to date with the latest revisions intended to prevent

drift and was installed at the beginning of this diagnostic run. The RM/BS controller VDTM module does not have the latest revision.

The ITM controller does not show drift, just a sudden jump to the maximum, where it is being timed by the ADC polling instead of VDTM polling bit. Also, the LSC Synch and LSC Skew diagnostics both indicate that the ITM controller is at least one full 61usec cycle behind the other controllers. Further investigation will be required to understand this instantaneous change.