LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

-LIGO-

CALIFORNIA INSTITUTE OF TECHNOLOGY

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Document Type	DCC Number **DRAFT**	February 3, 2004
LLO DAQ Network Upgrade Description of Changes and Installation Plan		
R. Bork		

Distribution of this draft:
This is an internal working note of the LIGO Laboratory

California Institute of Technology
LIGO Project – MS 18-33
Pasadena, CA 91125
Phone (626) 395-2129
Fax (626) 304-9834
E-mail: info@ligo.caltech.edu

Massachusetts Institute of Technology
LIGO Project – MS 20B-145
Cambridge, MA 01239
Phone (617) 253-4824
Fax (617) 253-7014
E-mail: info@ligo.mit.edu

www: http://www.ligo.caltech.edu/

1 Scope

The scope of this document is to provide a description and installation and test plan for a new Data Acquisition (DAQ) system network architecture at LLO during the period Feb. 17 through Feb. 27, 2004. This also includes the initial installation, for software and system integration testing, of the new HEPI control VME components.

2 Overview

For purposes of overall performance enhancement and to allow the inclusion of the new HEPI control system, the LLO DAQ network is to be modified. The primary change is to obsolete the existing DAQ network, based on the older VMIC5588 VME network modules with the later VMIC5579 and VMIC5565 PCI based networking modules.

The present scheme involves connecting realtime front ends and Analog Data Collection Units (ADCU) to the DAQ controller via a VMIC5588 reflected memory (RFM) network. The controller, in turn, realigns data from this network and then moves that data to the Framebuilders via a separate VMIC5579 network. The new design replaces these with two new networks, one based on the existing VMIC5579 modules and one based on the newer VMIC5565 network modules. An overview diagram is provided in the following figure. The key changes are described in the following subsections.

2.1 Network Connections

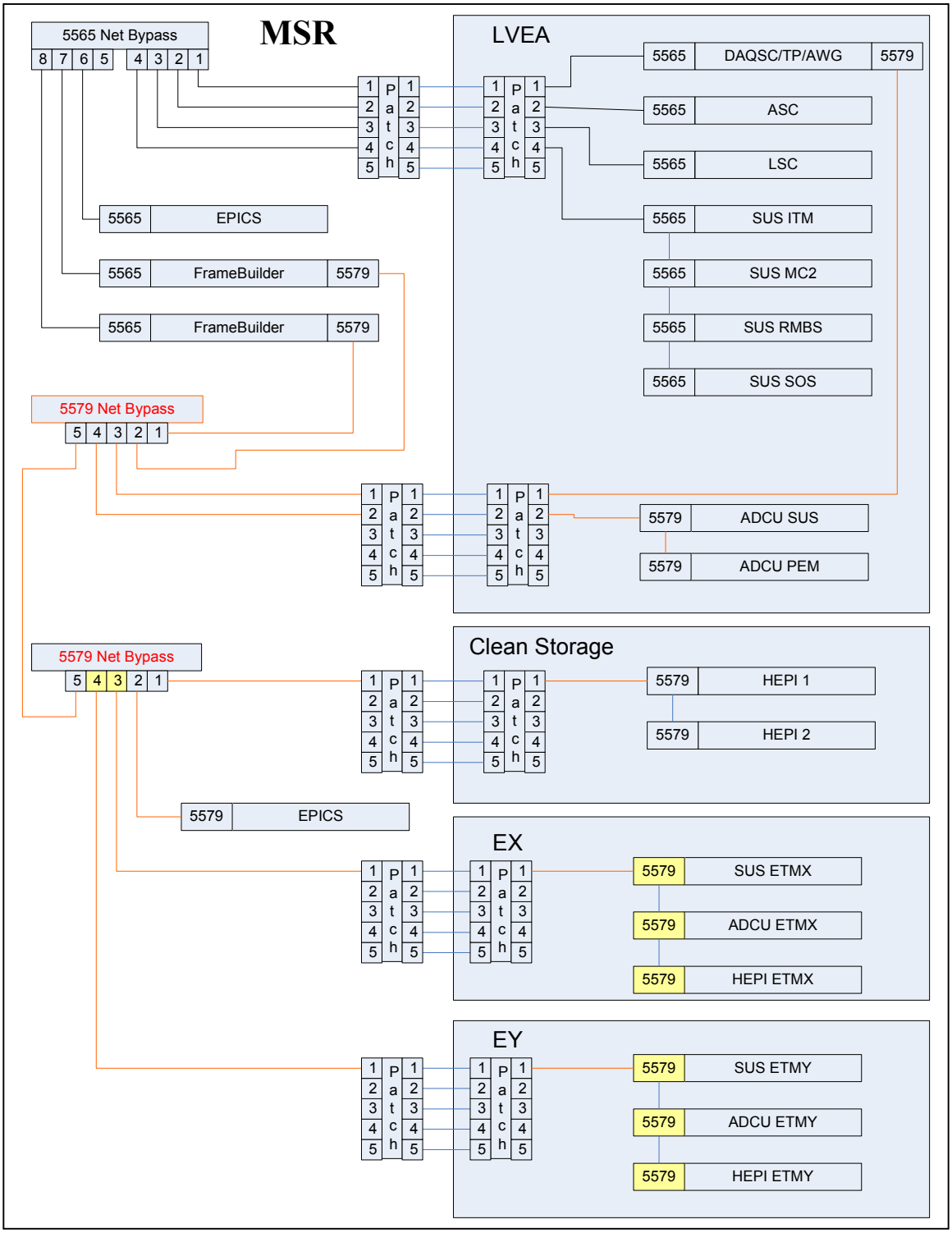
All realtime front end VME systems and ADCU are now directly connected to one of the two DAQ networks. In the present DAQ configuration, some VME processors, such as the large optic suspension (LOS) controllers, had to have their DAQ and Global Diagnostic System (GDS) signals routed through the Alignment Sensing and Control (ASC) or Small Optics Suspension (SOS) controllers. This required special coding and additional system dependencies, which now go away. This routing was necessary because the cost of placing a VME5588 module into every system needing to connect to DAQ was prohibitive (5 times cost of newer modules) and the memory space was limited to 4Mbyte (64Mbyte in new cards).

These new networks also provide two functions in addition to DAQ/GDS connections. One, they provide for the connection of the front end processors with their EPICS interface software, located on LINUX PCs in the Mass Storage Room (MSR). Secondly, in the case of the LVEA realtime systems, this network provides for the communication of real time control signals between the ASC, LSC and suspension controllers. Particularly to provide this latter function, the design calls for the faster VMI5565 (2Gbit/sec) network to be used for the interconnection of these particular systems. Costs prohibit the installation of all new VMI5565 network modules, therefore the second DAQ network makes use of existing VMI5579 modules which will be removed from various subsystems during this upgrade.

2.2 DAQ Controller

In the new architecture, with the framebuilders having direct connections to all data collection units (DCU), the scope of the DAQ controller functions is reduced. In the old system, the controller was responsible for system configuration and copying data from all the DCUs on the VMI5588 network to the framebuilders via a VMI5579 network. This was required in that system because the VMI5588 and its software drivers were not fast enough to pick up the individual data blocks from the DCUs directly and pack them into the frame in time. Therefore, the DAQ controller did the data packing. With the new modules and drivers, the framebuilders are now able to perform this task and it is no longer required of the DAQ controller.

Since the DAQ controller functionality is now reduced to system monitoring, it can be built with the GDS Test Point Monitor (TPM) and Arbitrary Waveform Generator (AWG) into a single VME processor. This processor has connections to both networks such that all GDS connections can be serviced from a single CPU.


MSR
5565 Net Bypass
8 7 6 5 4 3 2 1
5565 EPICS
5565 FrameBuilder 5579
5565 FrameBuilder 5579
5579 Net Bypass
5 4 3 2 1
5579 Net Bypass
5 4 3 2 1
5579 EPICS
Patch
LVEA
5565 DAQSC/TP/AWG 5579
5565 ASC
5565 LSC
5565 SUS ITM
5565 SUS MC2
5565 SUS RMBS
5565 SUS SOS
5579 ADCU SUS
5579 ADCU PEM
Clean Storage
5579 HEPI 1
5579 HEPI 2
EX
5579 SUS ETMX
5579 ADCU ETMX
5579 HEPI ETMX
EY
5579 SUS ETMY
5579 ADCU ETMY
5579 HEPI ETMY

2.3 FrameBuilders

Presently, there are two FrameBuilders, an EPICS Data Collection Unit (EDCU) and a FrameBroadcaster. These are Sun computers of various types. In the new architecture, the EDCU and FrameBroadcaster computers are removed. Using new software, the FrameBuilders will collect EPICS data directly. The FrameBuilder running on the Sun450 will pick up the additional task of broadcasting frame data to the GDS DMT machines. Among other things, this cuts down the number of RFM modules required in the new system.

2.4 System Configuration

Several significant changes have been made to the way the DAQ system is configured. In the past, a single master.config file was read by the DAQ controller, which, in turn, passed on configuration information to the FrameBuilders and the DCUs via the RFM networks. In the case of realtime control front end processors, all the DAQ channels provided by these processors were hard coded and therefore not reconfigurable by simply changing this master.config file. Also, signals defined as GDS test points could not be saved to frames without special code modifications.

In an attempt to improve the DAQ configuration capabilities, a couple of changes have been made. First, DAQ channel definitions are no longer hard coded into front end systems. Rather, all signals available from a front end process are now defined as "test points" in the same manner as GDS test points were defined in the past. This means that every signal now has a unique test point number associated with it along with a unique name. This change allows for several new features to be implemented:

1. All front end signals are available as test points through GDS test point selections, including those that had once only been defined as DAQ channels.
2. All front end signals are available to be stored to frames, including those that had only once been defined as test points and therefore could not be saved to frames.
3. Dynamic DAQ reconfiguration. Without recoding or shutting down front end processes, a new set of DAQ channels can be configured.

To facilitate this change, the configuration files have changed. The present master.config file is no longer used. In its place are a group of configuration files, all using the GDS file format:

1. Gds.par file: This file lists every signal available in LIGO as a GDS test point, including unique signal names and associated unique test point numbers.
2. DCU configuration files(*.ini): Each processor on the DAQ network now has its own DAQ channel configuration file. Along with other information, this file contains the test point numbers of the channels to be sent to DAQ by a DCU, along with the name the signal is to be given when stored to frames. These files are read in by EPICS sequencers and pertinent information passed on to the front ends via the DAQ networks.

2.5 CRC Checksums

A number of CRC checksums are computed in the new system to facilitate system integrity checks. First, a CRC checksum is performed on the DAQ configuration file loaded to a front end processor. Both the EPICs CPU loading the configuration to the front end and the FrameBuilders perform this checksum to verify that these systems are working with the same configuration. If the FrameBuilders detect a difference between their file checksum calculations and those being transmitted by the DCUs, they will mark all of that DCUs data as invalid in the stored frames and raise an alarm to the operator.

Each DCU also calculates and transmits a checksum with each 1/16 second data block. The FrameBuilders compute the same checksums on the received data to verify that the correct data was received.

For GDS excitation signals, checksums are performed on a per channel basis. This has to be done as multiple processors may be extracting only single channels from the AWG block.

2.6 ADCU

ADCUs now read data at 16KHz instead of the previous once every 1/16 second. In most every aspect, they appear now as a 16KHz front end control processor, making use of the same DAQ and GDS code libraries developed for control front ends. This being the case, ADCU will now have the added capability to read GDS excitation signals from the DAQ RFM and write them out to ICS115 DAC modules. This will preclude the need to place the AWG unit in the LVEA. Instead, the previous AWG's ICS115 module will be placed into one of the LVEA ADCU. ICS115 modules will also be added to the end station ADCUs.

3 Installation

3.1 Additional Equipment Required

The installation of the new DAQ network and initial HEPI system requires the shipment to LLO of the following equipment.

Description	Quantity
VMIC5565 PMC RFM Modules	7 + 1 spare
VMIC5565 PCI RFM Module	3 + 1 spare
Linux PC	1 (spare)
VMIC5579 PMC RFM Modules (Modified for single mode)	4
Single mode fiber transceivers to upgrade existing units	4 + 1 spare
VMIC5565 Network Bypass Unit (8 port)	1
ST to LC multimode fiber (single, various lengths)	16 + 2 spare
LC to LC multimode fiber (single)	3 + 1 spare
LC to LC multimode fiber (pairs)	3 + 1 spare
FC to SC single mode fiber (single)	8 + 2 spare
SC to SC single mode fiber (single)	4 + 2 spare
SC to SC multimode fiber (pair)	4 + 1 spare
VME processor (VMIC7805)	4
VME Clock Driver Module (Mod to rev. G)	4
VME Xycom 220 Module	3
VME Xycom 212 Module	3
VME Pentek Fanout Module	4
VME ICS110B Module	6
4pin LEMO timing jumper cables	4
20pin ICS timing jumper cables	4
VME Pentek Modules	7 (test use in HEPI only)

3.2 Installation Plan

The installation of the new systems is described in the following subsections. It is divided into three primary phases. The phases are laid out such that integrated subsystem testing can begin at the end of each installation phase while the next phase of installation proceeds. These test procedures are given in Section 4.

3.2.1 Site Survey

The first task of the new installation is to survey the present system layout. This needs to be done to:

1. Determine best available locations for new computers and network hubs in the mass storage room.
2. Verify presently installed fiber plant and routing through fiber patch panels. As part of this, it is to be checked on which fibers may still be used with the new configuration and to document the fiber runs and cable numbers on the new system layout drawings.
3. Determine what hardware, such as VME crates, is to be moved or removed.
4. Establish a new MSR room rack layout drawing.
5. Backup all copies of existing software.

3.2.2 Installation – Phase 1

The first phase is to install the new VMIC5565 network infrastructure. This will involve the shutdown of all realtime controls, therefore the interferometer must first be brought to a safe condition (all optics in shutdown mode).

3.2.2.1 Phase 1 – Hardware

The following hardware installations, removals and replacements are needed to move to the new VMIC5565 based DAQ network:

	Component	Add	Remove	Comments
1	All DAQ/ control front end systems.			Shutdown operation of all units connected to the present DAQ system.
2	5588 bypass VME crate	5579 VME Bypass unit w/single mode xceivers	Shutdown and/or remove crate and fiber optic connections.	Remove fiber connections from previous end station sm/mm converters; connect these fibers to sm xceivers on new unit.
3	5565 Network Hub	Install in MSR Rack. Install LC to ST fibers from ports 1 thru 4 to MSR/LVEA fiber patch panel.		Power up unit and make CDS network connections to web browser
4	DAQ Controller	VMIC7697A cpu w/PCI expander, 5579 and 5565 network cards.	5588 networking hardware	This unit will now function as DAQSC/TPM/AWG. Set 5565 node id to 4.
5	Framebuilders	5565 network PCI module		Connect LC fiber pair to 5565 net bypass unit, transceiver number 7 & 8. Verify connections to existing 5579 hub. Set Node ID to 1 and 2.
6	EPICS PC	Install new unit w/5565 module in MSR rack above existing 5579 based unit.		Connect LC fiber pair to 5565 net bypass unit, transceiver number 6. Set Node ID to 3.
7	5579 Network Hub	Fiber connection to present EPICS PC w/5579 card; fiber connection to new 5579 VME hub.	All present connections except those to Framebuilders.	Leave connection to Framebroadcaster as backup, though it is not planned for use.
8	ITM LOSC	5565 PMC; LC/ST fiber connect to patch panel and MC2 controller.	5579; SC/ST fibers.	Set Node ID to 7.
9	MC2 LOSC	5565 PMC; Connect LC/LC fibers to ITM LOSC and RMBS controller.	5579	Set Node ID to 8.
10	RMBS LOSC	5565 PMC; Connect LC/LC fibers to MC2 LOSC and SOS controller.	5579	Set Node ID to 9.
11	SOS Controller	5565 PMC; Connect LC/LC fiber from RMBS; connect LC/ST fiber to patch	PMC5579, VME5588 and their connecting fiber optics.	Set Node Id to 10. Modify CDM to rev. G or replace rev. F unit with rev. G. Requires new 20pin ribbon for P4

		panel. CDM rev. G.	CDM rev. F.	connector.
12	AWG		VME5588 Module and ST/ST fiber connection to patch panel.	This unit needs to be shutdown for now. If tests of new AWG in MSR are successful, parts of this system can be removed later.
13	ASC VME	PMC5565 and LC/ST fiber connect to patch panel.	VME5588 and ISC net PMC5579, along with their fiber connections.	Set Node ID to 5.
14	LSC VME	PMC5565 and LC/ST fiber connect to patch panel.	VME5588 and ISC net PMC5579, along with their fiber connections.	Set Node ID to 6.

3.2.2.2 Phase 1 – Preliminary Hardware Check

Once the hardware has been installed per the table above, the hardware is ready for a preliminary system integrity check:

1. Power up all computers and VME systems, along with the VMI5565 network hub.
2. Verify proper network link lights on VMI5565 hub for all ports connected.
3. Bring up VMI5565 hub web interface and verify proper status of all ports.
4. Verify link status lights on all VMIC5565 modules in MSR and LVEA processors.
5. Log into all CPUs on network and verify Node Ids are as assigned.

3.2.2.3 Phase 1 – Software

All processors connected to the new VMI5565 network (and 5579 network described later) require new software to interface to this network. The new software files required are listed in the following table, along with changes made to this software beyond that necessary to interface to the new DAQ network. Startup scripts for the various processors also need to be regenerated.

Subsystem	**Files Required**	**Changes**
ASC	Asc.o	Removed routing of DAQ/GDS signals to/from end stations.
LSC	Lsc.o	
SUS ITM	CoilStage2Itm.o	Removed data route thru SOS.
SUS MC2	CoilStage2Mc2.o	Removed data route thru SOS.
SUS RMBS	CoilStage2Rmbs.o	Removed data route thru SOS.
SOS	Sus90GDS.o 110b_drv	Removed routing of LOS DAQ/GDS signals. ICS110b now set as Master and decimated to 4096Hz, code reading module only on data ready ie not blindly assuming 110b ready if Pentek ready. This requires the CDM change to Rev. G. This is being done to try to resolve the channel glitching/hopping problems noted in the past.
DAQSC/TPM/AWG		
EPICS		This unit provides the EPICS interface via the 5565 network for all LVEA realtime control front ends. Code is unchanged except for network connection.

Once the appropriate executable software files have been copied to the applicable target directories, the last installation task prior to the start of testing is the downloading and verification of the initial DAQ and GDS configuration files. These files are to reside in the /cvs/cds/llo/chans/daq directory. The file names and association between a file and a processor connected to the DAQ network is listed in the following table.

	File Name	Subsystem	Max. Data Rate	Comments
	gds.param	Framebuilders and TPM		Complete list of all GDS excitation and test point signals.
1	L1LSC.ini	LSC front end VME processor	16384	These files all describe those signals which are to be sent to the Framebuilders as data to be stored to frames. The primary fields within these files are: 1. Signal test point number; every signal within the system must now have a unique test point number as well as unique name. 2. DAQ channel name: This is the name that this signal will be associated with in the data frame and resulting data retrieval. 3. Data storage rate. (<= max data rate of subsystem. 4. Data storage type. Presently supported data types are SHORT (16 bit integer) and FLOAT (32 bit floating point). 5. Channel gain settings (only applicable to ADCUs) NOTE: ***A signal may appear in either the gds.par file or one of the .ini files. A signal by same name and number cannot reside in both the .par file and .ini files. If this should occur, the Framebuilders will report an error.***
2	L1ASC.ini	ASC front end VME processor	2048	
3	L1SOS.ini	Small Optics Controller	2048	
4	L1SUS1.ini	LOS controller for ITMX and ITMY	16384	
5	L1SUS2.ini	LOS controller for recycling mirror and beam splitter.	16384	
6	L1SUS3.ini	LOS controller for MC2	16384	
7	L1ADCU_SUS.ini	Suspension coil data	16384	
8	L1ADCU_PEM.ini	LVEA PEM and PSL signals	16384	
9	L1SEI1.ini	HEPI controls for MC1,MC2,RM and OMC	2048	
10	L1SEI2.ini	HEPI controls for ITMX, ITMY,BS	2048	
11	L1SEI_EX.ini	HEPI end station X	2048	
12	L1SEI_EY.ini	HEPI end station Y	2048	
13	L1ADCU_EX.ini	End station X ADCU	16384	
14	L1ADCU_EY.ini	End station Y ADCU	16384	
15	L1SUS_EX.ini	ETMX Controller	16384	
16	L1SUS_EY.ini	ETMY Controller	16384	

3.2.3 Installation – Phase 2

The second phase of installation is to move the ADCUs over to the new VMI5579 network and add the end station LOS controllers to this new network.

3.2.3.1 Phase 2 – Hardware

The following hardware installations, removals and replacements are needed to move to the new VMIC5579 based DAQ network:

	Component	Add	Remove	Comments
1	Existing 5579 Net Hub	Fiber pair to connect port 5 to port 5 of new 5579 VME hub. Fiber pair to connect to MSR/LVEA fiber patch panel.		Existing hub should now have the following connections: 1. Framebuilder 2. Framebuilder 3. LVEA fiber patch panel. 4. EPICS PC 5. VME5579 hub
2	ADCU SUS	PMC5579 w/SC/ST connect to patch panel and SC/SC connect to ADCU PEM.	VME5588 and associated fibers.	Set Node Id to 4.
4	ADCU PEM	PMC5579 w/SC/ST connect to patch panel and SC/SC connect to ADCU SUS.	VME5588 and associated fibers.	Set Node ID to 5.
5	EPICS PC	Fiber pair SC/SC to 5579 hub.	Previous fiber connections to old framebuilder network.	Set Node ID to 3.
6	ADCU EX	PMC5579 w/SC/FC connect to patch panel and SC/SC connect to ETMX LOS.	VME5588 and associated fibers.	Requires single mode 5579. Set Node ID to 6.
7	ETMX LOS	PMC5579 w/SC/FC connect to patch panel and SC/SC connect to ADCU EX. CDM Rev. G.	MV162 processor. CDM Rev. F. Pentek module 3.	Requires single mode 5579. Set Node ID to 7. Pentek module goes to HEPI EX.
8	ADCU EY	PMC5579 w/SC/FC connect to patch panel and SC/SC connect to ETMY LOS.	VME5588 and associated fibers.	Requires single mode 5579. Set Node ID to 8.
9	ETMY LOS	PMC5579 w/SC/FC connect to patch panel and SC/SC connect to ADCU EY. CDM Rev. G	MV162 processor. CDM Rev. F. Pentek Module 3.	Requires single mode 5579. Set Node ID to 9. Pentek module goes to HEPI EY.

3.2.3.2 Phase 2 – Preliminary Hardware Check

Once the hardware has been installed per the table above, the hardware is ready for a preliminary system integrity check:

1. Power up all computers and VME systems, along with the VMI5579 network hubs.
2. Verify proper network link lights on VMI5579 hubs for all ports connected.
3. Verify link status lights on all VMIC5579 modules in MSR, end station and LVEA processors.
4. Log into all CPUs on network and verify Node Ids are as assigned.

3.2.3.3 Phase 2 – Software

All processors connected to the new VMI5579 network require new software to interface to this network. The new software files required are listed in the following table, along with changes made to this software beyond that necessary to interface to the new DAQ network. Startup scripts for the various processors also need to be regenerated.

Subsystem	Files Required	Changes
ADCU SUS	DcuDma.o 110b_drv	All ADCU now run at 16KHz w/DMA of data from ICS110B modules. ***NOTE: DCU_ID numbers and number of installed ICS modules is required in the startup scripts for all ADCUs.***
ADCU PEM	DcuDma.o 110b_drv	
ADCU EX	DcuDma.o 110b_drv	
ADCU EY	DcuDma.o 110b_drv	
SUS ETMX	IscEsx.o 110b_drv	Removed data route thru ASC. Removed VME module DMA reads. Removed Microseismic control and Pentek module 3. ICS110B read only when data ready. EPICS now from 5579 RFM network instead of embedded MV162.
SUS ETMY	IscEsy.o 110b_drv	Removed data route thru ASC. Removed VME module DMA reads. Removed Microseismic control and Pentek module 3. ICS110B read only when data ready. EPICS now from 5579 RFM network instead of embedded MV162.
EPICS	hepiepics	This unit provides the EPICS interface via the 5579 network for all HEPI and ES LOS controller realtime control front ends. Epics code has been removed from MV162 in LOS controllers onto the new PC.

Once the appropriate software files have been copied to the applicable target directories, these systems are ready for test.

3.2.4 Installation – Phase 3

The final installation involves putting the new HEPI controls in place. The permanent rack locations will not be ready at this time, so four VME crates will need to be set up in a temporary location. The purpose of this temporary installation is to test the new HEPI software, to the extent possible, integrated with the other LLO systems on the new DAQ networks.

3.2.4.1 Phase 3 – Hardware

Four VME crates need to be set up with the VME modules listed in the following tables.

3.2.4.1.1 HEPI 1

Final location is clean storage room. This unit will control four chambers: MC1, MC2, RM and Output mode cleaner chambers.

	Component	Comments
1	VMIC7751 CPU w/5579 PMC module	Requires CDS network connection plus 5579 fiber connection to VME5579 hub.
2	Clock Driver Module (CDM) Rev. G	Requires 1pps/4MHz clock connection from nearest clock fanout module (MSR?)
3	ICS110B modules (2)	First module needs to be set as MASTER, second as SLAVE, with bus addresses of 0xa00000 and 0xb00000, respectively. Connect 20 pin ribbon between P4 of both modules and CDM. Note: Slave unit and CDM module need to be at the ends of this ribbon with Master unit in between.
4	Pentek clock fanout	Connect 4 pin LEMO to output of CDM.
5	Pentek 6102 ADC/DAC modules (4)	Addresses set to 0xff00, 0xfe00, 0xfd00 and 0xfc00. Connect 2 pin Lemos from each module to Pentek clock fanout module.

3.2.4.1.2 HEPI 2

Final location is clean storage room. This unit will control three chambers: ITMX, ITMY and Beam Splitter chambers.

	Component	Comments
1	VMIC7751 CPU w/5579 PMC module	Requires CDS network connection plus 5579 fiber connection to VME5579 hub.
2	Clock Driver Module (CDM) Rev. G	Requires 1pps/4MHz clock connection from nearest clock fanout module (MSR?)
3	ICS110B modules (2)	First module needs to be set as MASTER, second as SLAVE, with bus addresses of 0xa00000 and 0xb00000, respectively. Connect 20 pin ribbon between P4 of both modules and CDM. Note: Slave unit and CDM module need to be at the ends of this ribbon with Master unit in between.
4	Pentek clock fanout	Connect 4 pin LEMO to output of CDM.

5	Pentek 6102 ADC/DAC modules (3)	Addresses set to 0xff00, 0xfe00, and 0xfd00. Connect 2 pin Lemos from each module to Pentek clock fanout module.
6	Xycom 220 Binary Output Module	Set address to 0xc800.
7	Xycom 212 Binary Input Module	Set address to 0xa000.

3.2.4.1.3 HEPI EX and HEPI EY

These two units are identical and will eventually be installed in the end stations to control the ETM chambers.

	Component	**Comments**
1	VMIC7797A CPU w/5579 Single Mode PMC module	Requires CDS network connection plus temporary 5579 single mode fiber connection to VME5579 hub.
2	Clock Driver Module (CDM) Rev. G	Requires 1pps/4MHz clock connection from nearest clock fanout module (MSR?)
3	ICS110B modules (1)	Module needs to be set as **STAND ALONE MASTER** with bus addresses of 0xa00000. Connect 20 pin ribbon between P4 and CDM.
4	Pentek clock fanout	Connect 4 pin LEMO to output of CDM.
5	Pentek 6102 ADC/DAC module (1)	Addresses set to 0xff00, 0xfe00, 0xfd00 and 0xfc00. Connect 2 pin Lemos from each module to Pentek clock fanout module.
6	Xycom 220 Binary Output Module	Set address to 0xc800.
7	Xycom 212 Binary Input Module	Set address to 0xa000.

3.2.4.2 Phase 3 – Preliminary Hardware Check

Once the hardware has been installed per the table above, the hardware is ready for a preliminary system integrity check:

1. Power up all VME systems.
2. Verify proper network link lights on VMI5579 hubs for all ports connected.
3. Verify link status lights on all VME processor VMI5579 PMC modules.
4. Log into all CPUs on network and verify Node Ids are as assigned.

3.2.4.3 Phase 3 – Software

The following table lists the software required to be loaded into each of the 4 HEPI VME processors. The EPICS software required should have been loaded during phase 2.

Processor	**Files Required**	**Comments**
HEPI1	Hepi1.o / 110b_drv	
HEPI2	Hepi2.o / 110b_drv	
HEPI_EX	Hepiex.o / 110b_drv	
HEPI_EY	Hepiey.o / 110b_drv	

4 Test Plan

Unfortunately, time does not permit the development of a complete test plan prior to installation. This section will be further developed during the installation process and will hopefully be more complete prior to the LHO installation. Therefore, this section is written as more of an overview of tests to be performed rather than detailed test procedures.

4.1 Phase 1

After Phase 1 installation, most of the previously existing systems should be back on line, with the exception of the end station LOS controllers. However, the end station controllers should still be compatible with the new system with the exception of DAQ capabilities, and therefore can be run during this test.

The key items to be tested during this phase:

1. DAQSC/TPM/AWG operation: This system should come on line and present the proper status indications to the new LLO DAQ overview MEDM screen. This includes green status indicators and running cycle counters.
2. Framebuilders: Verify proper loading of gds.par and subsystem .ini files. Should come on line with green status indicator, running cycle counter and channel count and network information. Verify proper writing of data files to local and LDAS disk drives and connections to GDS and Dataviewer tools.
3. EPICS: Verify all EPICS BURT files have been restored for all front end systems controlled/monitored by the EPICS PC w/5565 interface installed.
4. Verify all startup scripts are correct for the various front end controllers. These should be auto generated after modifying the appropriate files in the target area.
5. SOS controller: This unit should be brought back on line first. Verify that the DAQ connection is operating properly. This is indicated on the DAQ overview display. The system should both be on time and the CRC check sum should be correct.
6. Each GDS TP and DAQ channel needs to be verified through the use of Dataviewer and SOS control settings. Proper connections to DTT should also be verified at this time.
7. Once DAQ/GDS testing of the SOS controller is complete, each optic should be brought back on line, one at a time, and verify that each optic damps properly.
8. LOS controllers: The LOS controllers should now be brought on line, one at a time. Along with the DAQ/GDS connections, the sensor signals from the SOS controllers need to be verified to operate correctly. Once this is complete, the optics should be enabled and damped.
9. ASC/LSC: These systems are the last to be restored. Again, DAQ/GDS connections need to be verified. Also, verify all LSC/ASC data connections are correct to optic controllers.

This completes a brief list and description of items to be done to bring the LLO systems back on line with the new DAQ 5565 network. There are still a number of integrity checks that need to be performed on this part of the system while Phase 2 and 3 installation are in progress. Among these are:

1. Power systems up and down and verify proper reconnections to DAQ and other systems. As systems go up and down, verify DAQ controller and Framebuilders detect and report the status changes.
2. Modify .ini configuration files and verify both that front ends read in the new files properly and that the new configurations are detected by the Framebuilders.
3. Disconnect various fiber connections and ensure that system detects the fault and that these disconnections do not disrupt DAQSC/Framebuilder operations.
4. After a number of hours of operation, verify capability to recall data from disk, both full frames and trend frames.

The preliminary testing listed thus far should take one to two days. If the systems successfully complete these tests, the IFO should be brought on line. One of the main reasons this upgrade is being performed prior to shutdown for HEPI installation is to verify that all of the new hardware and software being

installed does not degrade the performance of the IFO. Therefore, it is desirable to bring the IFO into a full Science Mode state and noise spectrum taken. This can be done it this point, or wait until Phase 2 installation and preliminary testing are complete. The difference after Phase 2 is that the end station LOS controllers will be operational on the new software and DAQ network at that time.

4.2 Phase 2

Phase two testing involves the testing of the ADCUs and end station LOS controllers added to the new VMI5579 network.

1. Verify that the startup scripts for the ADCUs are correct. In the new system, the startup script requires the setting of the DCU_ID number and NUM_ICS_MODS. This allows the same executable code to run on any ADCU.
2. Start up each ADCU individually. Primarily, signals should be "sanity" checked, using previous data as necessary. Verify that any channels that have gain applied at the ADC module are operating properly.
3. The end station LOS controllers should be brought on line and again DAQ and EPICS connections verified. Also, verify communications with the LSC and ASC systems. Once this is done, the optic should be enabled and checked for proper damping.

At this point, all previously existing LLO control systems should be back on line with the new DAQ/GDS connections. The IFO should be brought on line to Science Mode and spectrum taken to verify new systems operation.

4.3 Phase 3

Phase 3 involves the testing of HEPI integrated with the rest of the LIGO systems. This is a completely new system, with test plans to be covered in separate documentation. The testing to be performed at this time include:

1. Proper connections to DAQ and GDS without degradation of other control systems' performance.
2. Proper connection to HEPI EPICS PC.
3. Initial functional checkout without connection to HEPI electronics. Software is also to be demonstrated for overall match to requirements with any deviations noted such that software can be modified prior to final HEPI installation.