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Technical Note **LIGO-T070034-A - D** 2/19/07

Voltage Regulation and Power Supplies

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1 SUMMARY

The following 4 approaches were investigated for suitability in building power supplies for advanced LIGO:

1. Noise eater: A circuit to suppress low frequency noise on analog power supplies.
2. Voltage regulator: A very low noise LDO regulator for post-regulation of analog supplies.
3. Point-of-load regulator: A non-isolated power module for digital supplies.
4. Synchronous buck regulator: A power supply to generate local supplies from a 48V DC input.

Fig. 1 shows the concept of the advanced LIGO power distribution system.

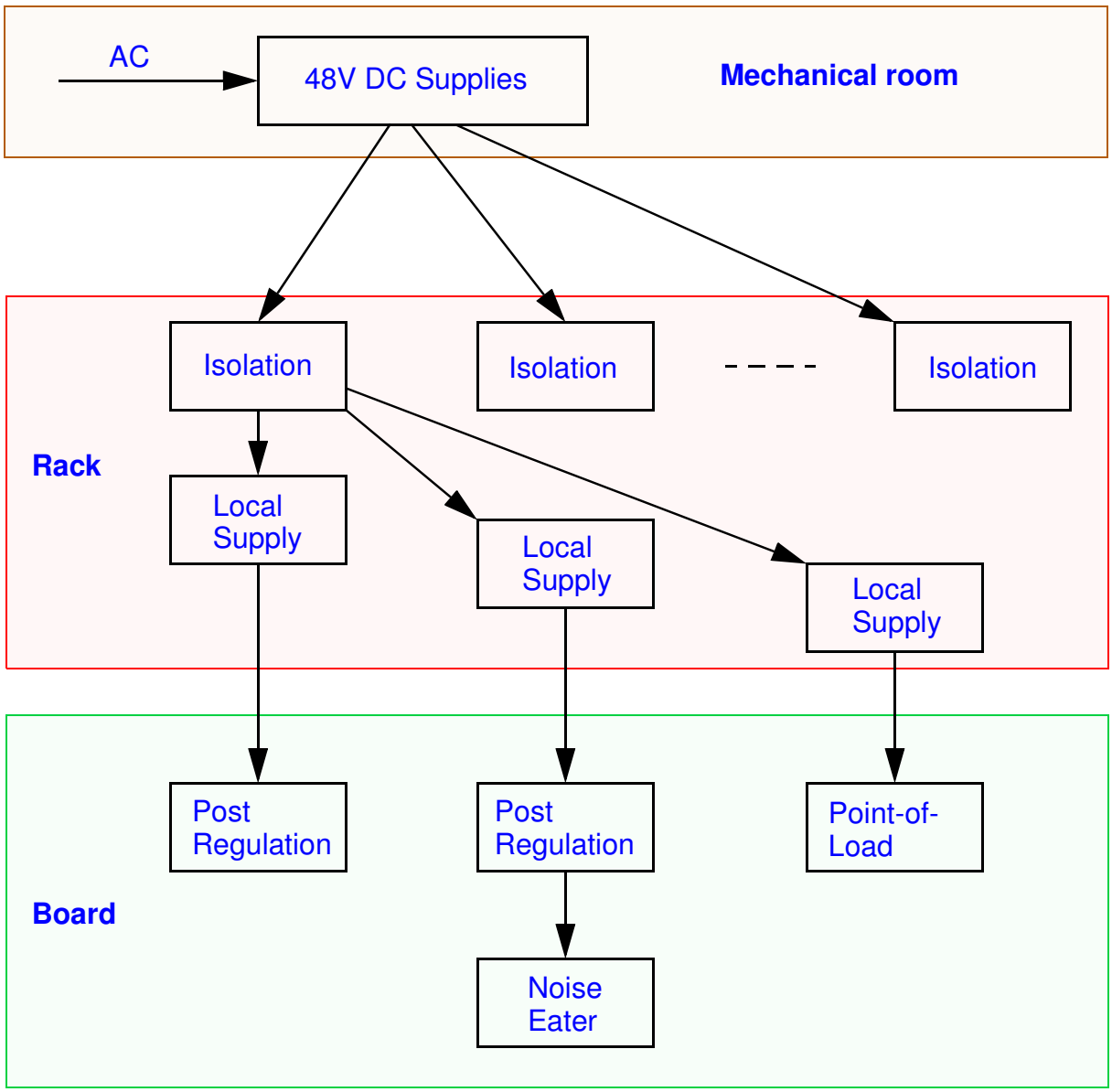

Figure 1: Concept of Power Distribution.

2 NOISE EATER

The noise eater circuit can be used to cleanup an analog power supply. It works by employing a current shunt and a feed forward system which measure the incoming noise level (see Fig. 2). Up to 30dB of suppression can be expected without trimming, but balancing the bias currents is tricky and the required board real estate is excessive. This design is not recommended. If a low noise supply is required a better option is the regulator described in the next section.

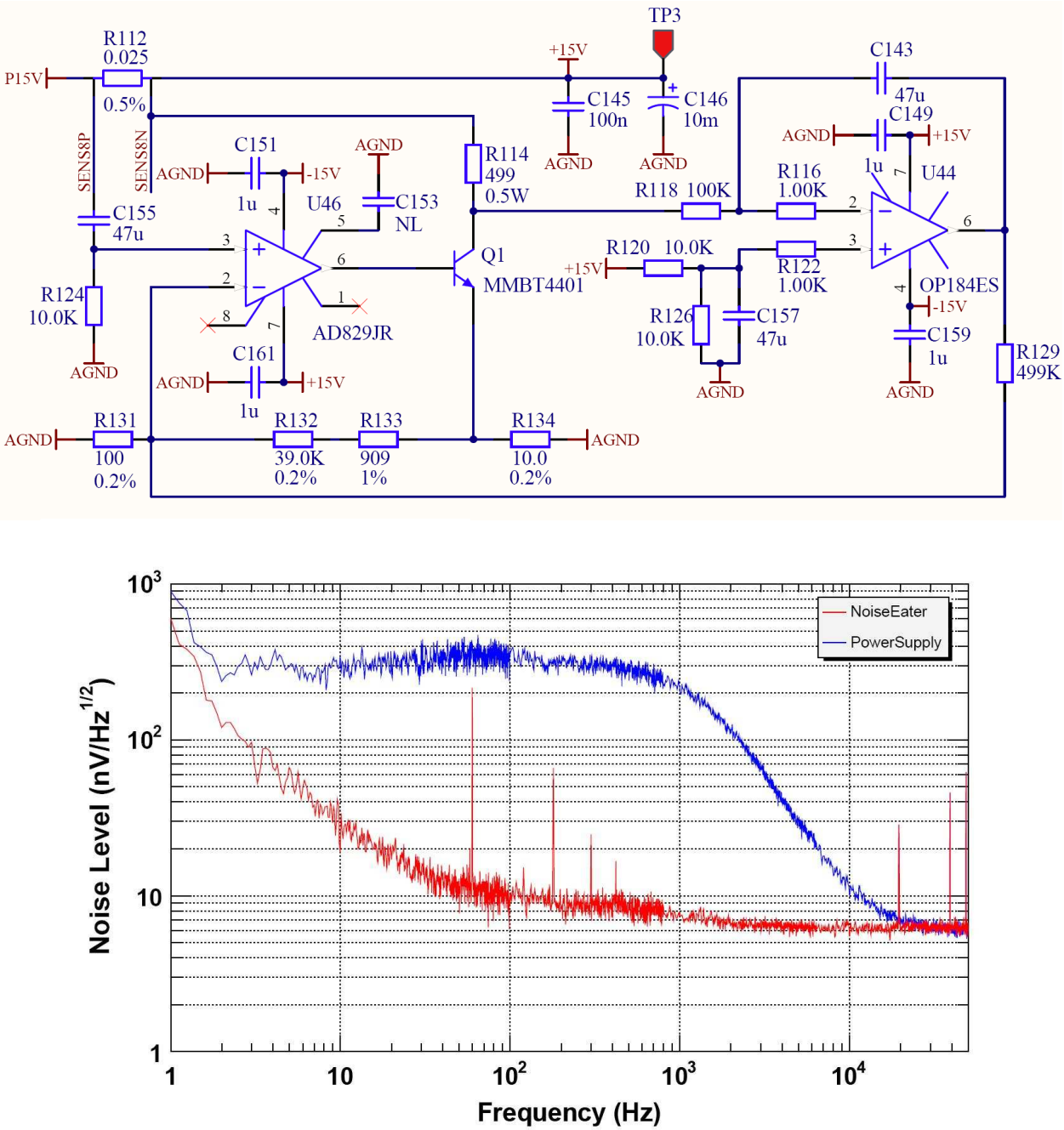

Figure 2: Schematics and performance of noise eater implemented after a standard +15V linear regulator.

3 LINEAR POST REGULATION

A schematics can be found in document LIGO-D060293 (see Fig. 3). Since commercial linear LDO regulators typically use a noisy internal voltage reference and are of limited availability for negative rails, D060293 demonstrates a simple regulator based on a low noise voltage reference. Its disadvantage is the requirement of an additional power rail above the nominal input value to power the feedback circuit. However, its performance is superior to commercial units.

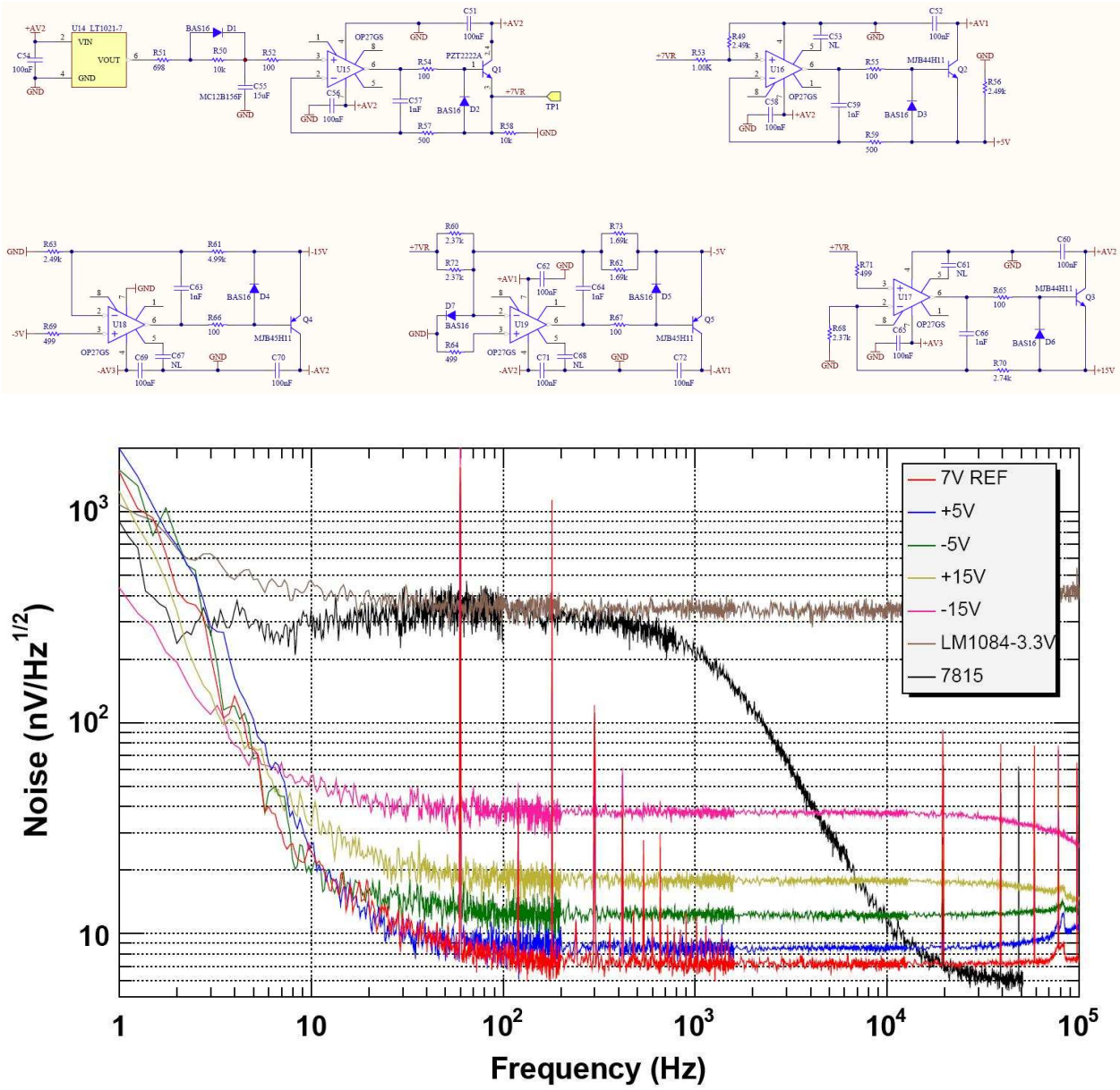

Figure 3: Schematics and performance of a very low noise linear voltage regulator.

The typical supply voltages are $\pm 6.5\,\mathrm{V}$, $\pm 16.5\,\mathrm{V}$ and $\pm 24\,\mathrm{V}$ to generate low noise supplies for analog $\pm 5\,\mathrm{V}$ and $\pm 15\,\mathrm{V}$. At $1\,\mathrm{A}$ of current draw the typical voltage drop is about $160\,\mathrm{mV}$.

4 POINT-OF-LOAD REGULATOR

For digital systems—especially modern FPGA based ones—a series of low voltage rails is required. However, current draws can be quite substantial. This makes it no longer feasible to generate this rails externally. In our application we instead chose a +12V supply rail for all digital supplies. One or multiple point-of-load regulators will then generate the required voltages—such as +5V, +3.3V, +2.5V, +1.8V or +1.2V—locally. We evaluated a commercial module from Texas Instrument, the PTH08T240W. This is a DC-DC converter with up to 10A output and efficiencies up to 95%. One of its advantage is that it works from an external synchronization signal and can be locked to the GPS clock. This makes sure that the lines from the switching frequency is either aliased at DC or the Nyquist frequency and therefore does not add in-band noise. A schematics with 4 different supplies sharing an input capacitor bank is shown in Fig. 4 (D060295).

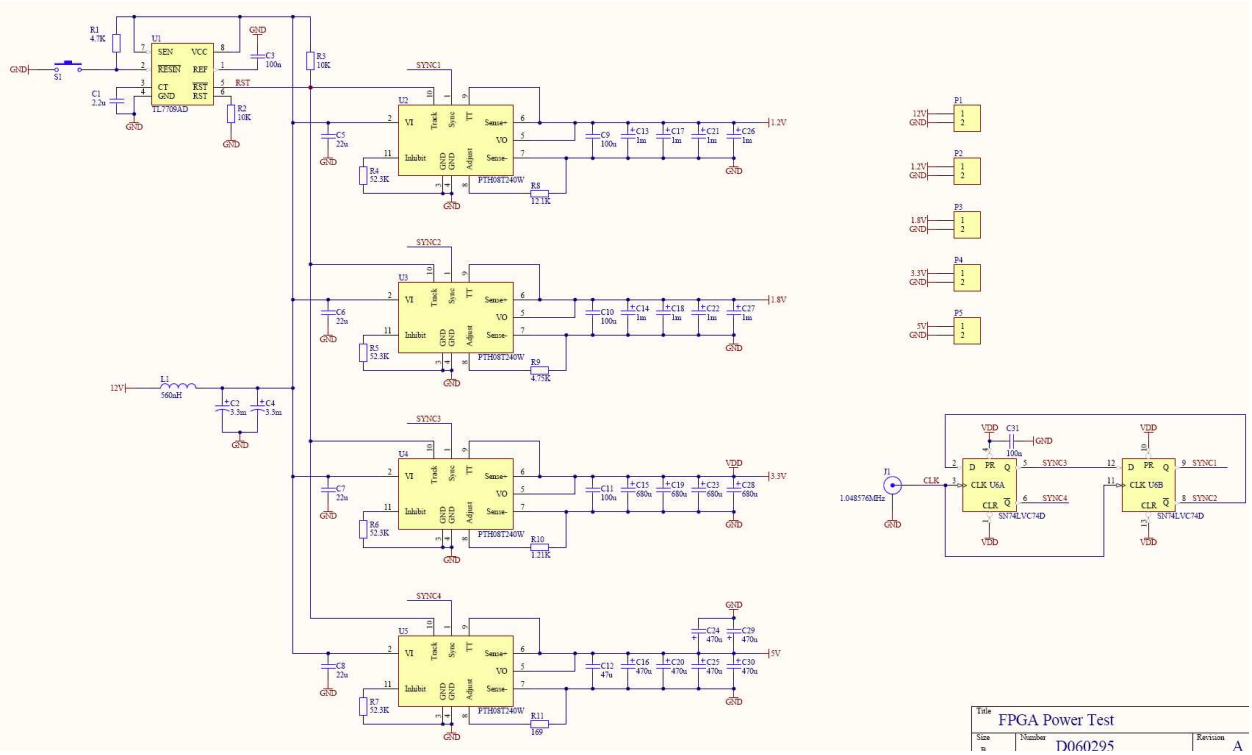

Figure 4: Schematics of point-of-load regulators for digital voltages.

Performance data is shown in Fig. 5. The switching transients are at the couple of mV level and are out-of-band.

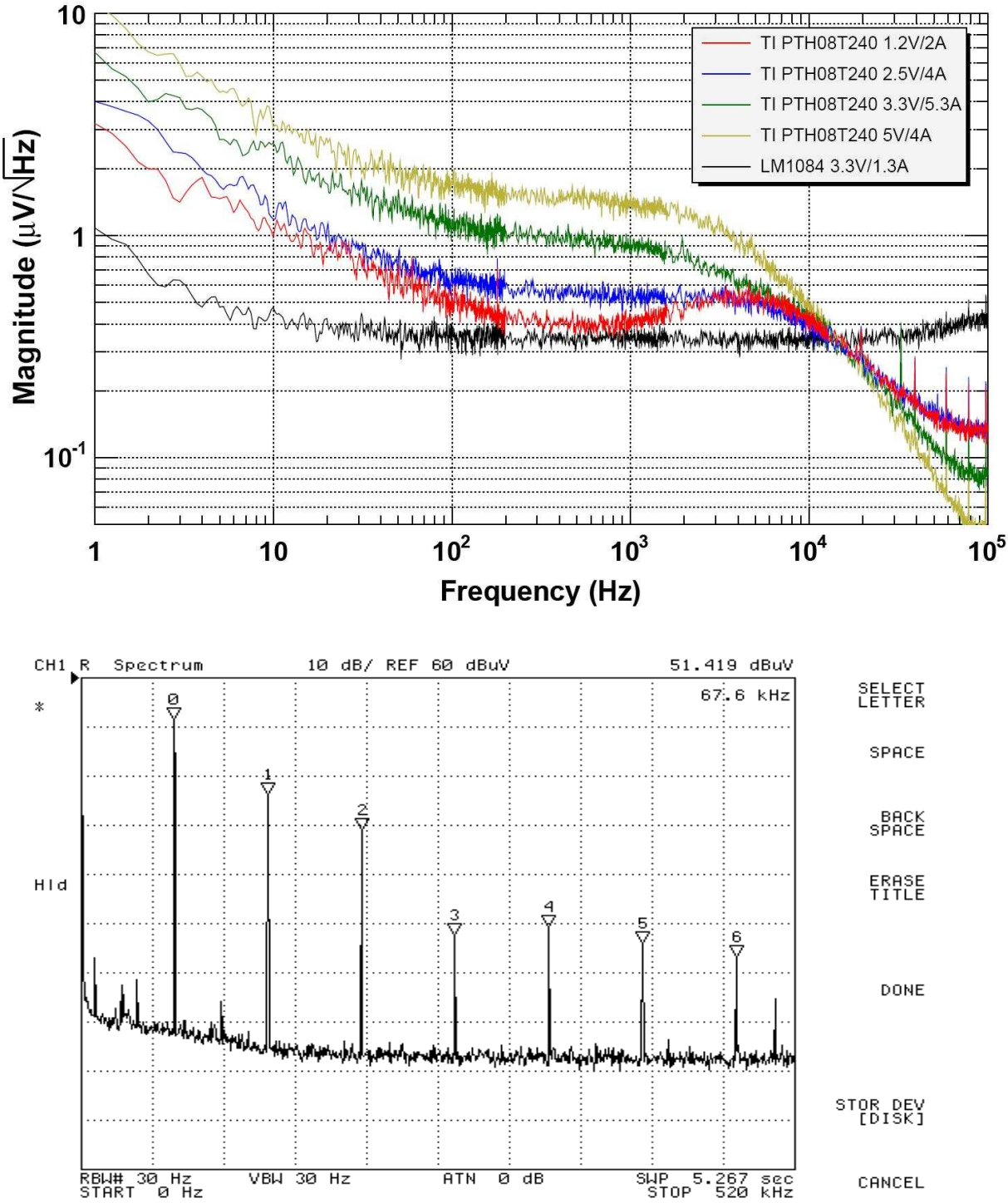

Figure 5: Performance of the point-of-load regulator. Top graph shows the in-band spectrum, whereas the bottom one shows the spectrum of the switching transients.

5 SYNCHRONOUS BUCK REGULATOR

A schematics of the synchronous buck regulator can be found in D060421. The circuit has a wide input range starting a few Volts above the desired output level up to 72V. It is intended to run from a 48V DC power supply. There is PM version which generates both positive and negative rails. Its is intended for ±6.5V , ±16.5V and ±24V . Its maximum output rating is 10A for the positive rail and 8A for the negative rail. The PP version (D060512) implements a positive rail only and is intended for +12V . Its maximum output rating is 20A.

A picture of the PM version (rev B) is shown in Fig. 6.

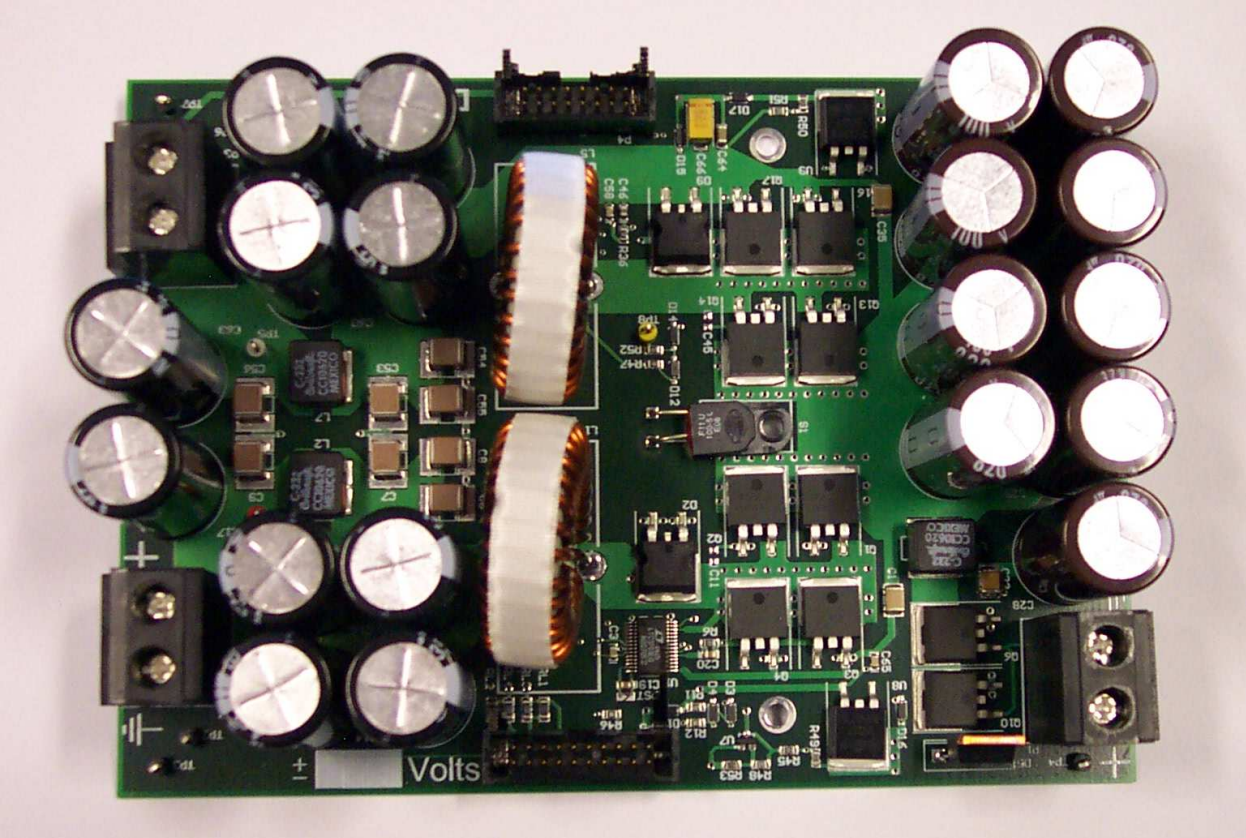

Figure 6: Picture of the synchronous buck regulator.

Plots for efficiencies, total loss and maximum temperatures as function of load current are shown in Fig. 7 and Fig. 8. The data were taken with a PM version implementing revision B at ±16.5V . Fig. 8 also shows a FLIR image of the module with 8A load on each rail. The circuit board was mounted on a 1.5” x 1.5” aluminum bar which served as a heatsink. The hottest points are the top MOSFETs of the negative rail.

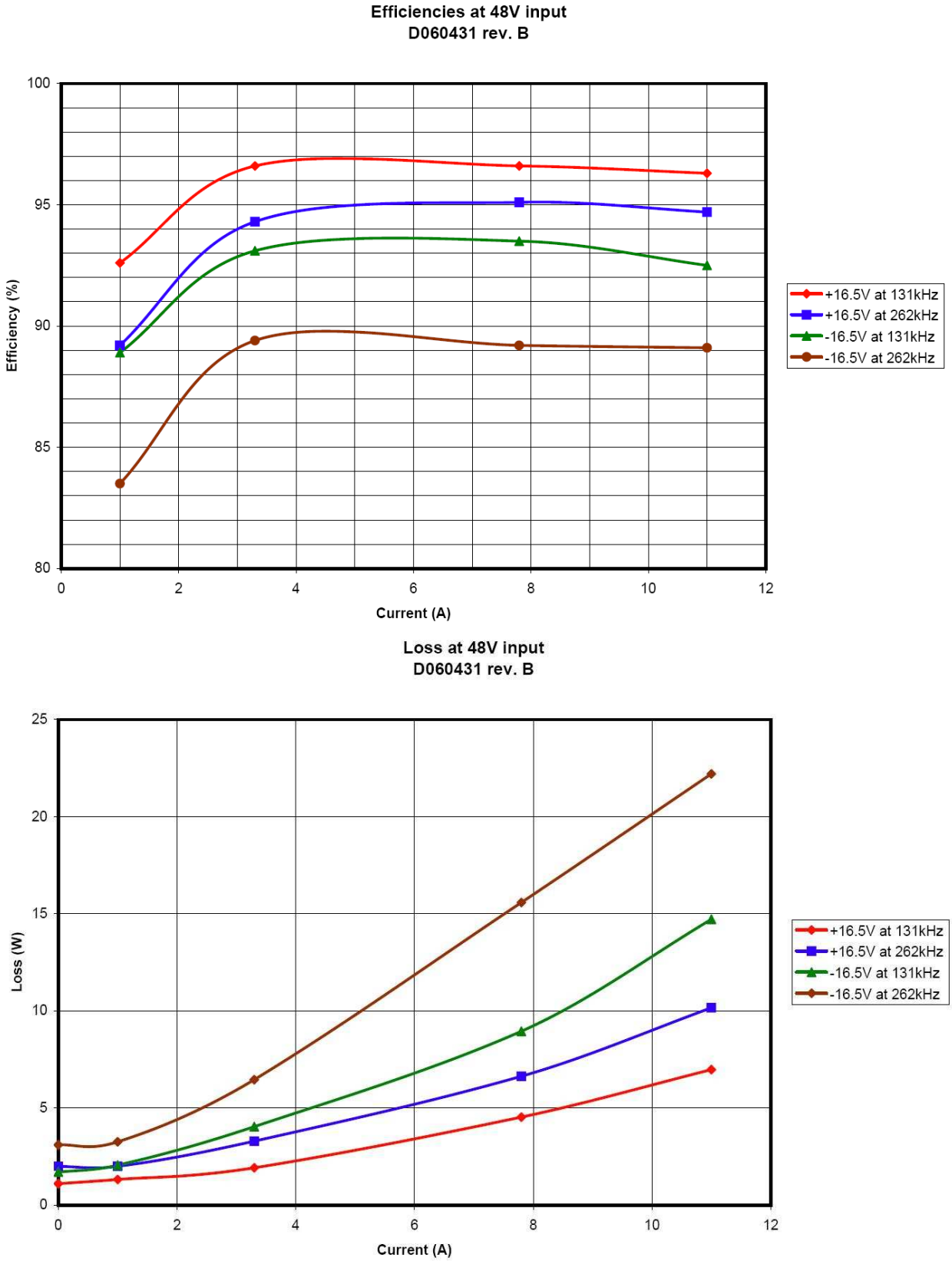

Figure 7: Efficiency and loss for synchronous buck regulator: PM version at 16.5V.

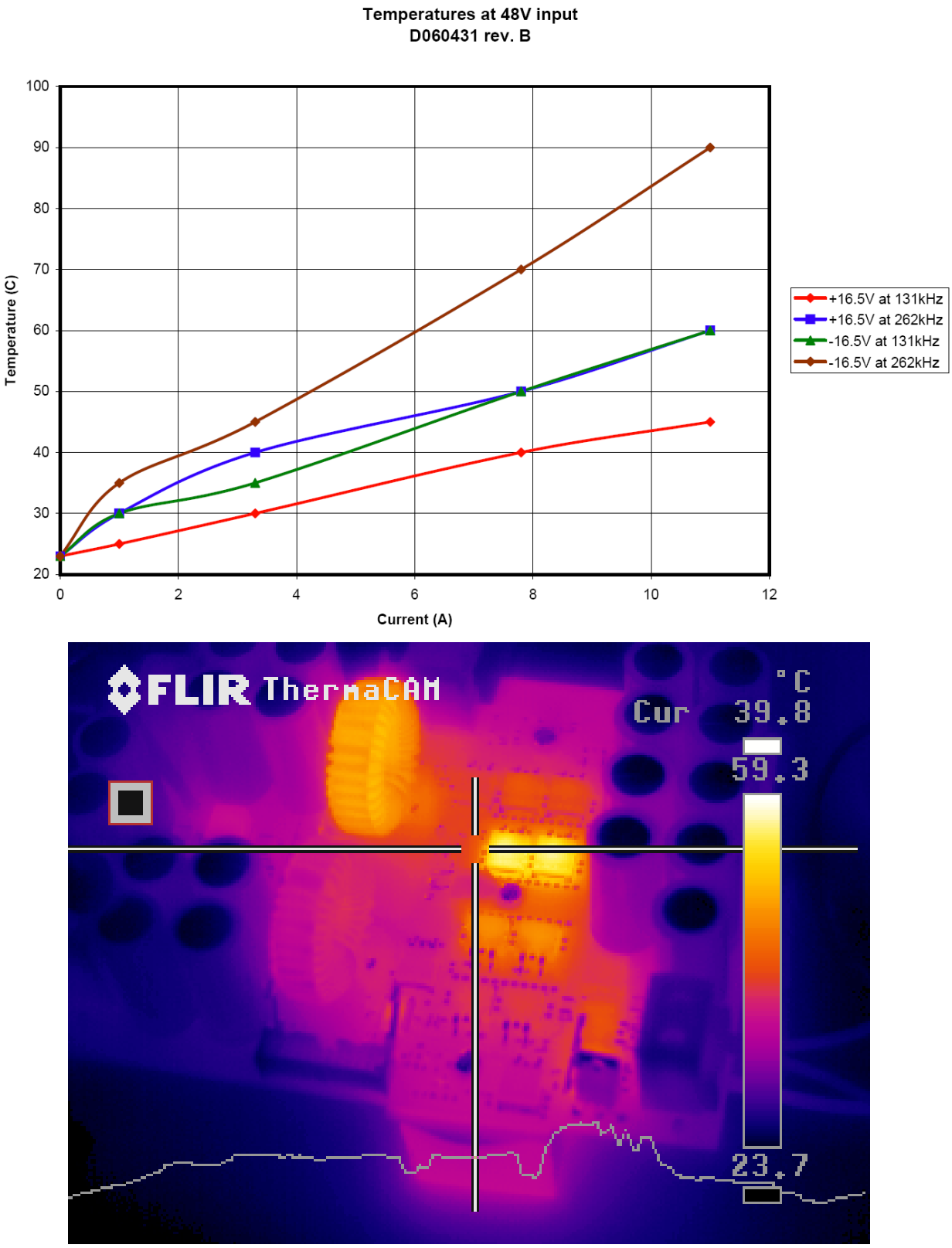

Figure 8: Maximum temperature of the synchronous buck regulator: PM version at 16.5V. The FLIR image shows the module loaded with 8A on each rail.

Similar plots are represented in Fig. 9 and Fig. 10 for the PP version at +12V. The current sense error rises from about –4% at low load to about +4% at maximum load. The temperature coeffcient of the resistivity of copper is about $0.4\%/°C$ which most lilkely explains the observed effect.

The plots for the $\pm 24V$ supply are shown in Fig. 11 and Fig. 12. Due to the current limit and the saturation of the coil the maximum current of the $-24V$ rail is $8A$ with the current limit kicking in around $8.6A$.

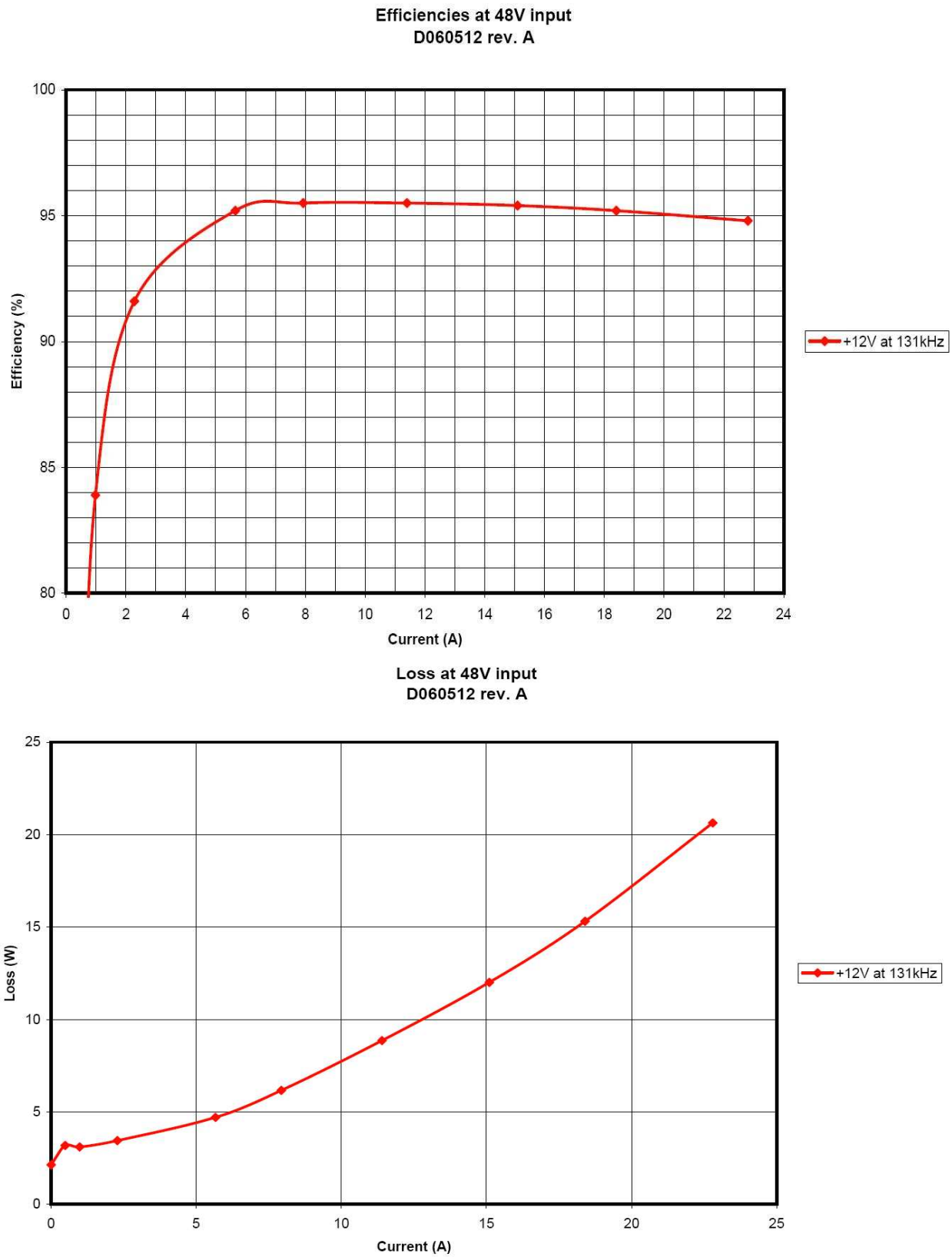

Figure 9: Efficiency and loss for synchronous buck regulator: PP version at 12V.

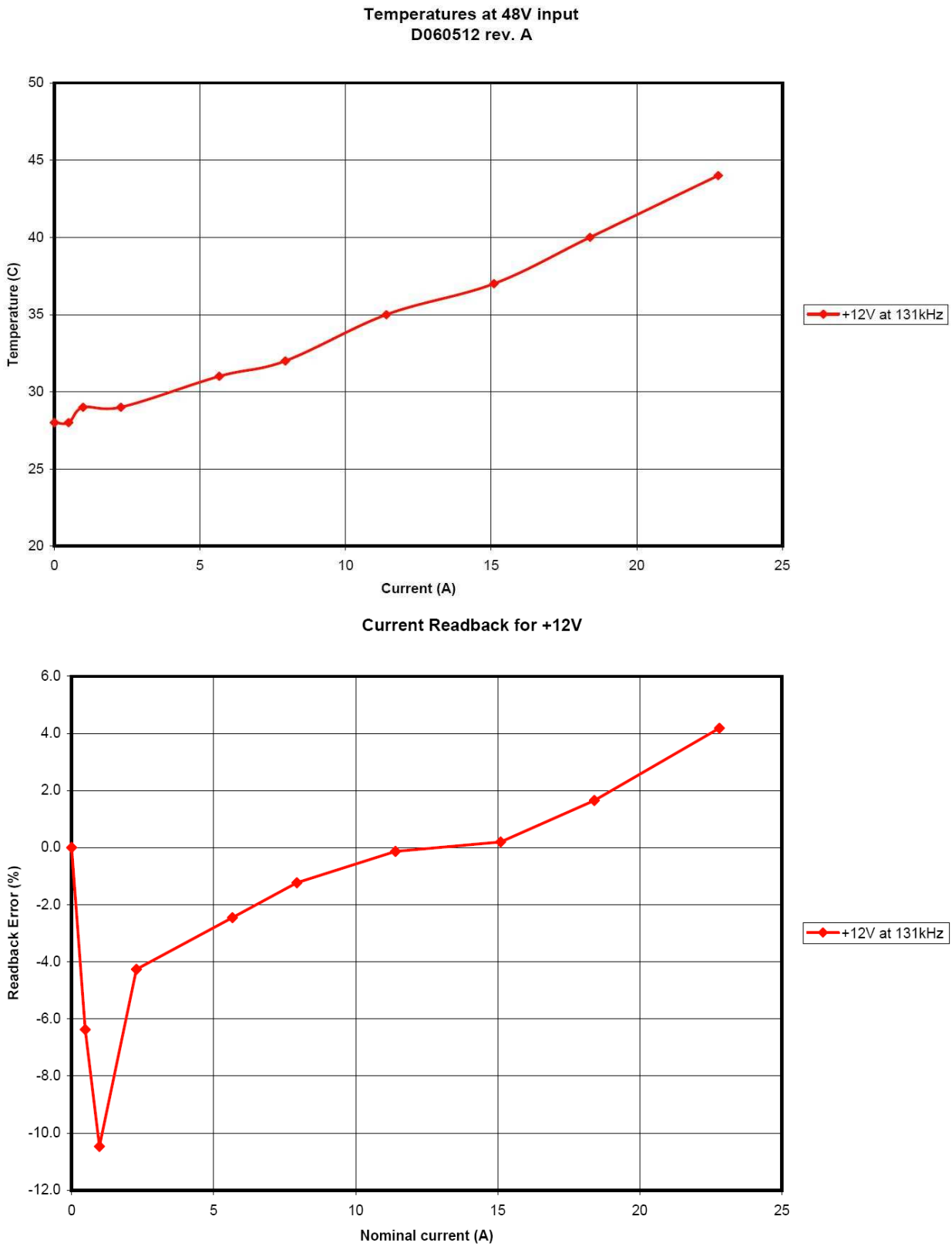

Figure 10: Maximum temperature of the synchronous buck regulator: PP version at 12V. The current sense readback error is shown in the lower plot.

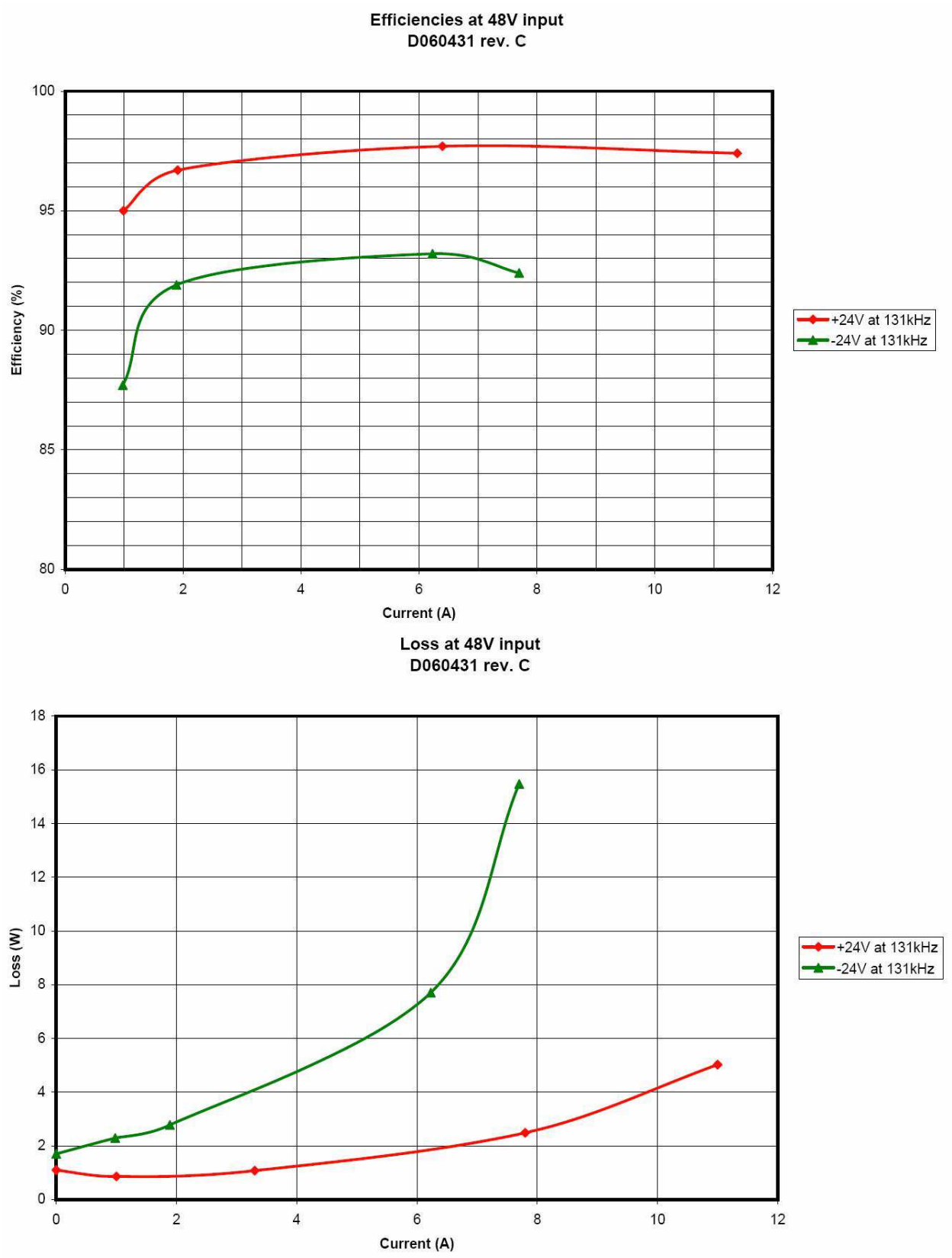

Figure 11: Efficiency and loss for synchronous buck regulator: PM version at 24V.

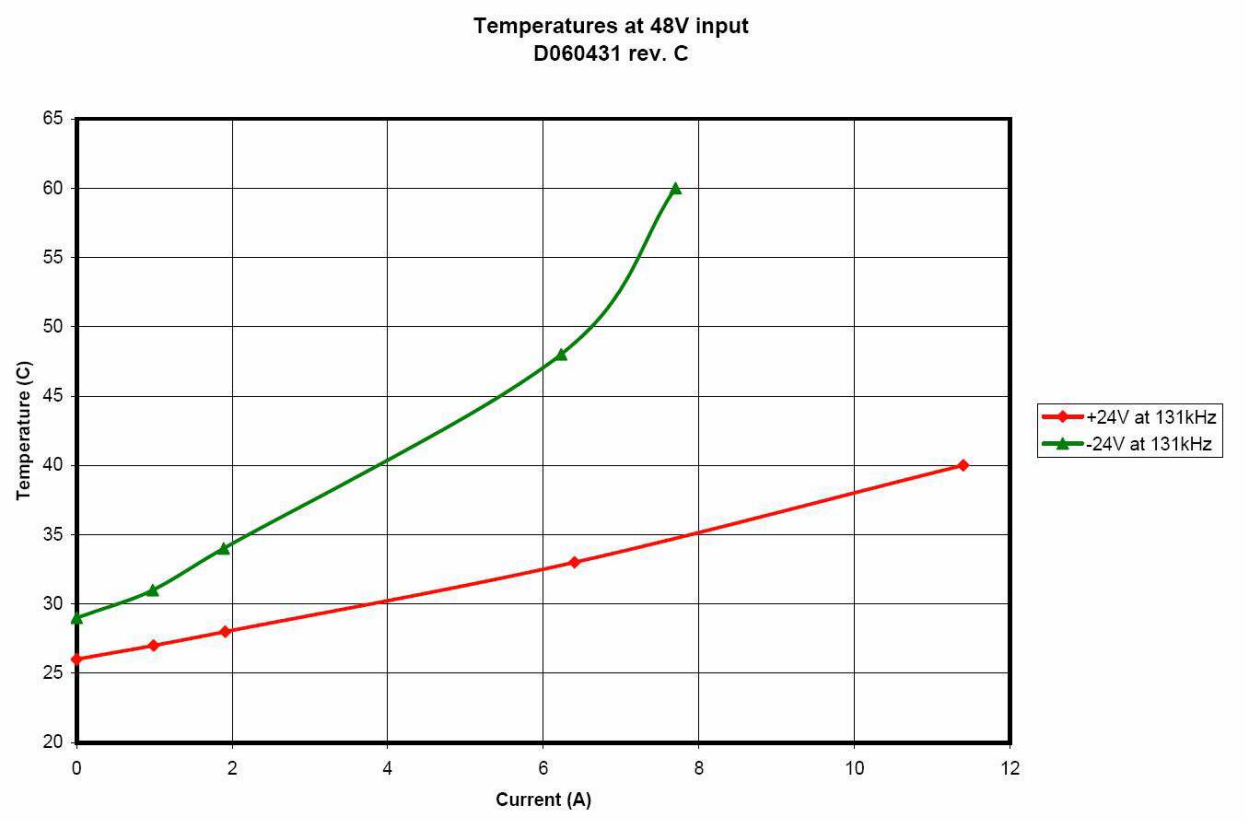

Figure 12: Maximum temperature of the synchronous buck regulator: PM version at 24V.