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GDS REFLECTIVE MEMORY ORGANIZATION

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DAQ and diagnostics system

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1 Introduction and Overview

This is a companion document to the “Data Acquisition System: Reflected Memory Network Design” (T980017-00) and details the organization of the part of the reflective memory which controlled by the GDS. One DAQ/GDS reflective memory ring is provided per interferometer (see Fig. 1 of T980017-00). The reflective memory is divided into a DAQ and a GDS section with a size of 2 MB each (see Fig. 2 of T980017-00).

The reflective memory is further subdivided into the following regions:

- IPC (DAQ): interprocess communication
  Used to send messages and status information between DCUs and the DAQ system controller.
- MAP (DAQ): memory allocation pointer area
  Used to describe the layout in the reflective memory
- DDA (DAQ): data definition area
  Used to describe the information associated with data channels
- Data (DAQ)
  Used to store data channels
- TPI (GDS): test point interface
  Used to organize and store test points and test point data from digital subsystems
- FFT (GDS): FFT spectrum data and interface
  Used to store FFT information and spectra
- Flag data (GDS)
  Used to store flag channels generated by the GDS search tool
- ISC (GDS): fast interprocess communication between LSC and ASC
  Currently not used

1.1 MAP Area Extensions

The above layout requires the following extension to the MAP area (as defined in T980017-00):

Table 1: MAP area extensions introduced by GDS.

Data Class	Variable Name	Descriptor & comments
char*	tpLookupPtr	Pointer to the test point lookup table
int	tpLookupCount	Total number of entries in the test point lookup table
char*	tpIndexPtr	Pointer to the test point index
int	tpIndex16kCount	Total number of 16384 S/s test points
int	tpIndex2kCount	Total number of 2048 S/s test points
char*	tpDataPtr	Pointer to first test point data block
int	tpBlockOffset	Offset between test point data blocks
int	tpBlockCount	Total number of test point data blocks
char*	fftInfoPtr	Pointer to FFT information table

Table 1: MAP area extensions introduced by GDS.

Data Class	Variable Name	Descriptor & comments
int	fftInfoCount	Total number of FFT channels
char*	fftDataPtr	Pointer to FFT data
char*	fastFlagDataPtr	Pointer to first block of fast flag channel data
int	fastFlagBlockOffset	Offset between fast flag channel data blocks
int	fastFlagBlockCount	Number of fast flag channel data blocks
char*	slowFlagDataPtr	Pointer to first slowData structure used by slow flag channels
int	slowFlagDataCount	Total number of slow flag channels
char*	iscIPC	Pointer to fast interprocess communication area reserved for LSC/ASC communication
int	iscIPCSize	Size of this area
For describing channel blocks reserved for digital subsystems:		
int	lscOffset	Offset to LSC digital subsystem fast data
int	lscCount	Number of LSC digital subsystem fast data channels
int	ascOffset	Offset to ASC digital subsystem fast data
int	ascCount	Number of ASC digital subsystem fast data channels
int	iooOffset	Offset to IOO digital subsystem fast data
int	iooCount	Number of IOO digital subsystem fast data channels

The last six entries of Figure 1 are describing offsets and channels counts for data written by the LSC, ASC and IOO digital subsystem into the fast data block owned by the DAQ. Data of each of these subsystems will require a contiguous memory block. Digital subsystems will use these pointers rather than the channel information stored in the DIA to determine the memory location for their channel data. It is the responsibility of the DAQ system controller to guarantee that

- these memory pointers are correct at the beginning of each second and agree with the channel information stored in the DIA and that
- the digital subsystem channels described in the DIA are occupying a contiguous memory block of the right size.

Digital subsystems will read these offsets at the beginning of each second and will use them during the rest of the second. In case the size of the reserved memory block does not correspond to the one which the digital subsystem intend to use, the digital subsystem will write back an error code only.

1.2 DDA Usage and Extensions

Since the data channels stored in the TPI and flag areas is part of the data acquisition, they have associated dataInfo structs which are stored in the DDA. To distinguish these channels from channels acquired by a DCU, they will have dcuID’s which are greater than 1000. FFT channels do not have their own channel definition, but use their associated time series channels to define name ('_FFT' extension) and data rate. Information exclusive to FFT channels is stored in a separate fftInfo area (see Section 4).

Table 2: Extensions to the DDA introduced by GDS.

Data Class	Variable Name	Descriptor & comments
Test points	dcuID	Unique dcu number which identifies the test point interface
	chNum	Used for the test point ID number
Excitation system	dcuID	Unique dcu number which identifies the test point interface
	chNum	Used for both test point ID number and DAC channel number
Flag channels	dcuID	Unique dcu number which identifies the search tool which is calculating the flag channel
	chNum	reserved
LSC channels	dcuID	Unique dcu number which identifies the LSC crate
	chNum	Used for the LSC channel number
ASC channels	dcuID	Unique dcu number which identifies the ASC crate
	chNum	Used for the ASC channel number
IOO channels	dcuID	Unique dcu number which identifies the IOO crate
	chNum	Used for the IOO channel number

1.3 GDS Reflective Memory Layout

An estimate of the memory block sizes of TPI, flag, FFT and ISC sections is presented below:

- test point interface: 400 kB (4 buffers)
- FFT channels: 1 MB (16 spectra with 16384 points each)
- flag channels: 256 kB (4 buffers)
- ISC interprocess communication: 10 kB
- normal ISC data channels: ~100 kB/buffer (located in the DAQ data area)

2 Flag Channels

The only difference between a flag channel and a normal data channel acquired by a DCU is that flag channels are generally written late, since they are processed channels. Flag channels are written by the search tool into separate data block located in the GDS section of the reflective memory. Flag channels are defined by an associated dataInfo struct located in the DDA area. Flag channels can be accessed by the RTDD (real-time data distribution) system and might be stored to disk using the frame builder.

3 Digital Servo Test Points

This section presents the implementation of digital test points in those subsystems containing digital controls. Test points (TP) are internal servo signals of digital subsystems and can be outputs or inputs. Outputs are used for reading out internal servo signals; they are written by the digital subsystem and read out by the DAQS. Inputs are used to inject excitations signals; they are written by the GDS excitation system and are read by both the digital subsystem and the DAQS.

Digital servo test points are used to perform the following functions:

1. Measure closed loop gains. These measurements are used for:
   - determination of phase and gain margins
   - adjustment of gains to achieve intended unity gain frequencies
   - diagnostic tests that make estimates of noise couplings (frequency noise, e.g.)
   - calibrations
2. Strain calibration, performed with various types of excitation:
   - swept sine
   - fixed sine(s)
   - pseudo-random noise
3. Measure cross-couplings:
   - length-length
   - length-angle
4. Measure sensing matrices:
   - alignment sensing
   - length sensing

3.1 Test Point Interface

All digital test points are given an ID number and a corresponding dataInfo structure. The dataInfo structure definition follows that given in T980017-00, with the extensions listed in Table 2. The ID numbers and dataInfo structures are given in a table, tpLookup. The zero entry of the table is used to designate the version number of the table (thus zero is an invalid TP ID#). The ID numbers are grouped by subsystem and are separated into inputs and outputs; blocks of ID numbers are assigned as follows:

- 1 – 99: LSC; test inputs
- 100 – 499: LSC; test outputs
- 500 – 699: ASC; test inputs
- 700 – 1499: ASC; test outputs
- 1500 – 1599: IOO; test inputs
- 1600 – 1999: IOO; test outputs
- 2000 – 2047: excitation system DAC channels

The ID numbers for all the test points and some of the dataInfo information are given in Table 5 in Appendix A.

There are many more (potential) test points in digital subsystems than will ever be used simultaneously, so we define a (re)configurable subset which is deemed large enough to accommodate maximum usage of simultaneous test points:

- Rates: TPs can either be 16384 S/sec (16k) or 2048 S/sec (2k).
- Number: the TP subset allows a maximum of 16 16k and 64 2k TP channels.

Test point subsets will be configured through an index (TPindex), which will list the TP ID#s for each data channel in the index. The index has 80 entries; unused channels will be marked with 0.

The TPindex can change at each 1 second interval. There is no notification when this happens, so each subsystem containing digital test points must update its TPindex (160 bytes) every 1 second. The TPindex will be maintained and configured by the GDS system controller.

Test point data will be stored in the GDS half of the reflective memory network in four 1/16 sec buffers:

- tp16k1: first 1/16 sec buffer for 16k test point data. The buffer length is 16 channels of single precision floating point numbers. Total size: 64 kByte.
- tp2k1: first 1/16 sec buffer for 2k test point data. The buffer length is 64 channels of single precision floating point numbers. Total size: 32 kByte.
- tp16k2/tp16k3/tp16k4: second, third, and fourth buffers for 16k test point data.
- tp2k2/tp2k3/tp2k4: second, third, and fourth buffers for 2k test point data.
- Total memory size: 384 kByte

Within each 1/16 sec buffer, the inputs are grouped at the beginning (end) of the buffer, and the outputs at the end (beginning). The boundary between inputs and outputs will change depending on the diagnostic test being run (defined by the TPindex).

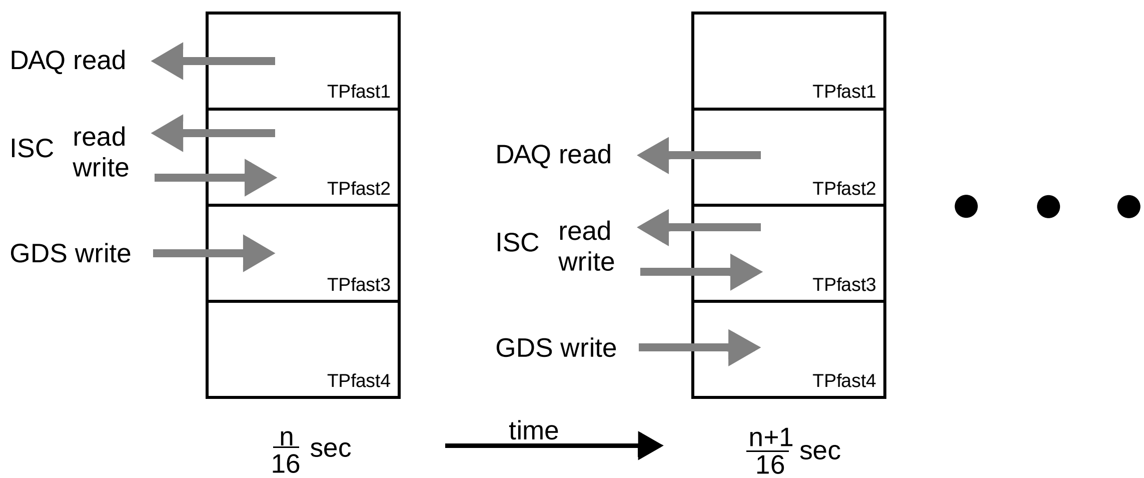

Figure 1: Reflective memory test point buffer usage. The figure shows how data is written to and read from the four ‘fast’ buffers over two 1/16 sec intervals. The extra buffer is included for timing flexibility, and may be used differently than shown here.

3.2 Digital Subsystem Test Points

Loop gain measurements during servo operation can generally be made by forming the ratio between the signal after a summing junction and the injected test signal, giving $1/(1 + G)$, where G is the total open loop gain. In some cases, such as when correcting an error signal spectrum for loop gain, the value of $(1 + G)$ is desired. In other cases the value of G itself is desired; while this can be calculated from the above measurement, it can be directly measured by forming the ratio between the signals before and after the summing junction. For each sensed degree-of-freedom in a MIMO (multiple-input multiple-output) digital servo, we thus include a TP input with readouts before and after the summing point (typically the normal DAQ channel for that degree-of-freedom provides the readout before the summing point, and a TP output gives it after). Excitations to perform the other types of measurements listed in the Introduction can also be applied at these TP inputs. It is also useful to be able to excite degrees-of-freedom after the servo functions are applied, and TP inputs are supplied here in both the sensing and the individual mirror bases. Note that because the sensing basis is different from the mirror basis for each of the subsystems, there is generally no single test input that allows excitation of a single mirror within the servo band. However by applying an excitation simultaneously to several test inputs in the proper ratio, a given single optic can be stimulated.

For all three digital subsystems, the individual raw sensor signals are available as test points; these are the outputs from each photodetector channel, demodulated in two, (nearly)-orthogonal phases. Each signal corresponding to a given degree-of-freedom is provided to the DAQS for writing to frames. In between the signal types may be software for summing and/or mixing the two phases of the individual raw sensor signals; this is indicated by the box labeled Σ–ϕ in Figures 2–4.

3.2.1 LSC TPs

A block diagram of the digital portion of the LSC servo is shown in Figure 2. It shows the test points as well as the normal sensor and control outputs that the DAQS always stores to disk. In the LSC there are some instances of more than one control path for a given degree-of-freedom (in addition to the straightforward sensor-to-mirror basis rotation performed on all channels). Where there is a split in the control path, test inputs are inserted in each path at the split, and a test output is included just before the split. These allow for convenient measurement of the (open) loop gain of the individual paths (in combination with the total closed loop gain measurement).

Two additional test inputs are included in the LSC, though they are not part of the LSC servo (and not shown in Figure 2). These are modulation signals for the photon calibrator laser diodes – one channel each for the X and Y arm calibrators (located at the ETMs). These channels make use of the LSC corner station-end(mid) station reflective memory network. The stimulus data is copied by the corner station LSC processor from a GDS TP buffer to the LSC RM ring; at the end(mid) stations the local LSC processor sends it to a (otherwise unused) DAC output of the LSC I/O board. This arrangement avoids needing to implement waveform generators at the end & mid stations.

3.2.2 ASC Test Points

A block diagram of the digital portion of the ASC servo is shown in Figure 3. The block diagram shows the current conception of how the wavefront sensor signals will be processed, and the test points have been chosen in this context. If some of the servo filters and rotation matrices are done differently, the test points may change.

3.2.3 IO Mode Cleaner Test Points

A block diagram of the digital portion of the Mode Cleaner servo is shown in Figure 4. It is functionally equivalent to two channels of the ASC system. Feedback control is applied to PZT-controlled mirrors at the input of the mode cleaner.

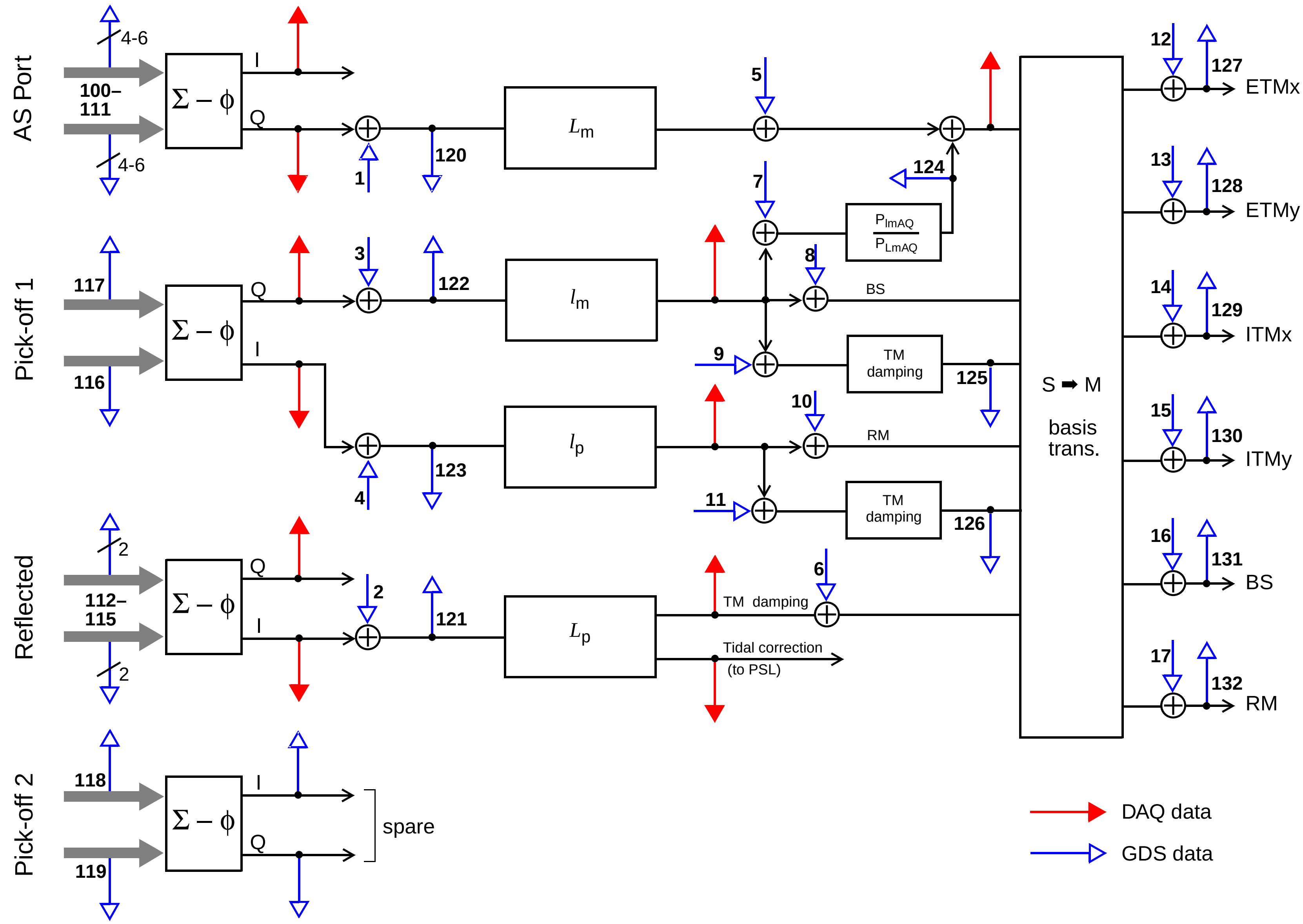

Figure 2: Digital portion of LSC servo, showing ID#s for test points.

Note: all TPs are pairs (for pitch & yaw), unless otherwise noted.

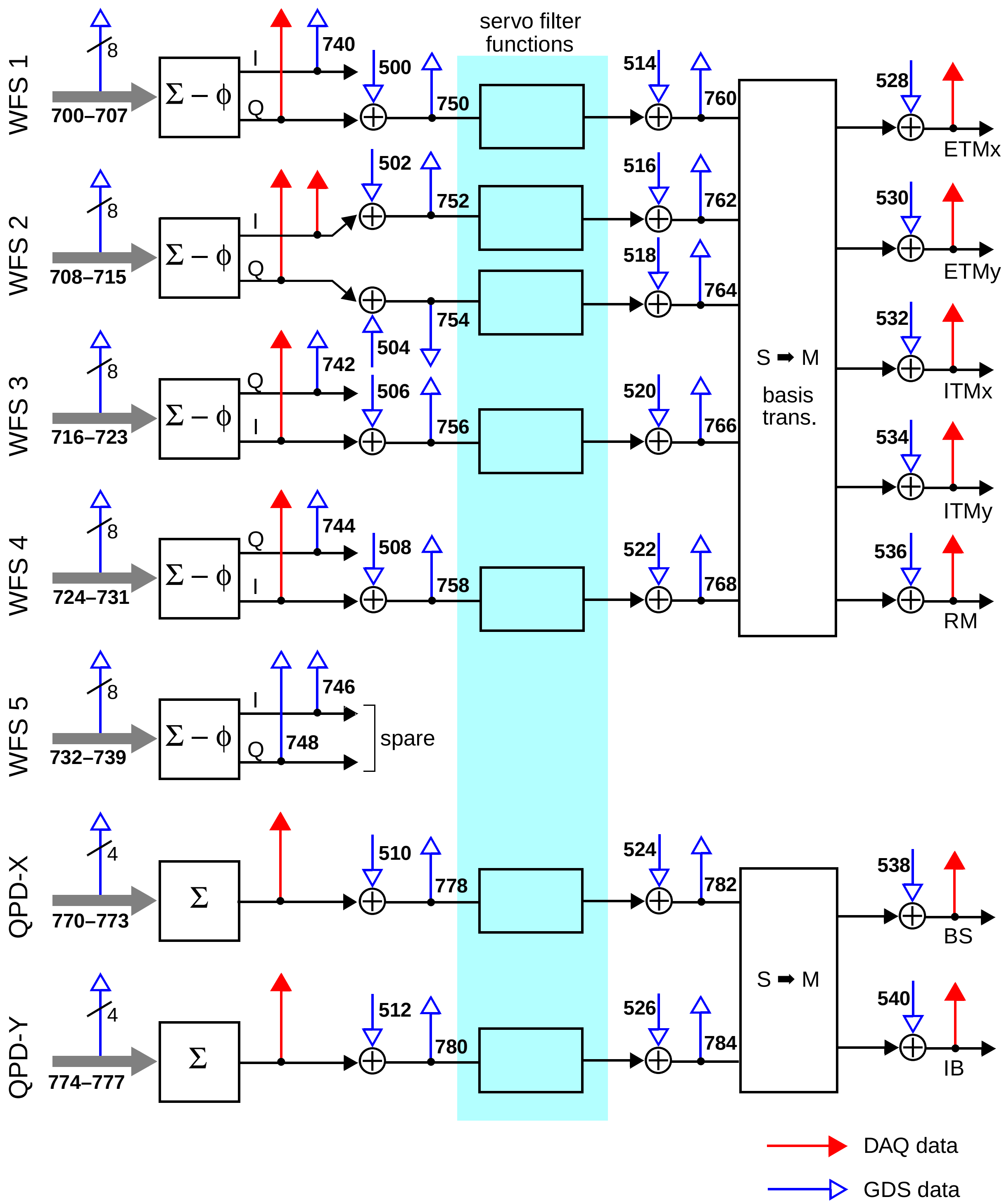

Figure 3: Digital portion of ASC servo, showing ID#s for test points (except for the raw sensor signals, only the even TP IDs, corresponding to the yaw signals, are shown).

Note: all TPs are pairs (for pitch & yaw), unless otherwise noted.

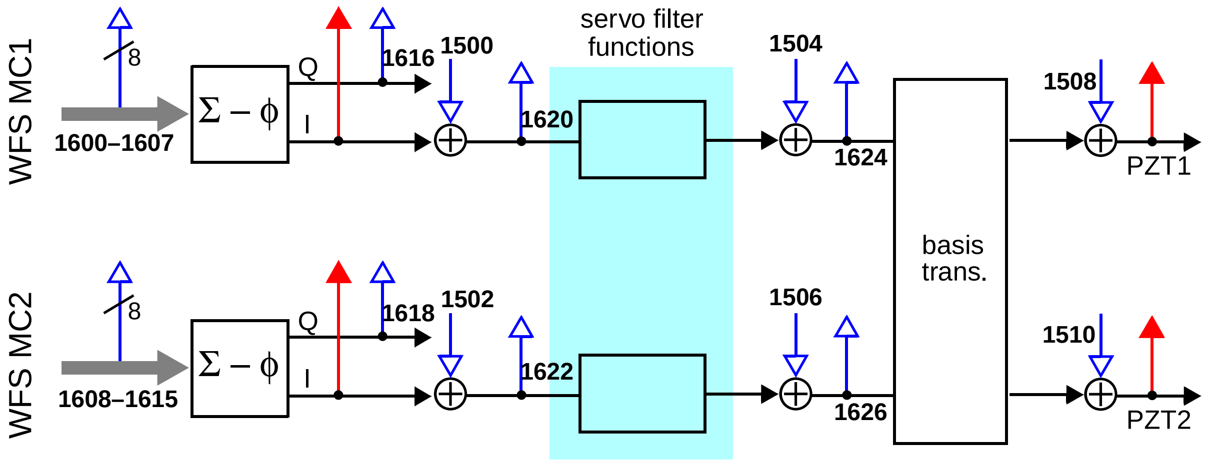

Figure 4: Digital portion of Mode Cleaner servo, showing ID#s for test points (except for the raw sensor signals, only the even TP IDs, corresponding to the yaw signals, are shown).

4 FOURIER TRANSFORM CHANNELS

4.1 REQUIREMENTS

The GDS system and its computing engine provide a number of general purpose FFT channels which are calculated in real-time. They are located in the GDS part of the reflective memory and can be accessed by any subsystem — such as the RTDD — which has access to it. To limit both the amount of processing power and the amount of needed reflective memory, the number of general purpose FFT channels can not exceed 16 per interferometer and the maximum number of points is 16384.

4.2 FFT INFORMATION AREA

The FFT information area is organized as a table with each entry describing one of the general purpose FFT channels. The following fftInfo struct is used:

Table 3: struct fftInfo.

Data Class	Variable Name	Descriptor & comments
*dataInfo	chPtr	Pointer to the dataInfo struct which describes the time series of the FFT spectrum
int	fftType	Determines whether the FFT or the amplitude power spectrum is calculated
int	fftPoints	Number of FFT points
int	fftRefresh	Number of samples which have to be acquired before a new FFT is calculated
int	fftWindow	Determines the window function
char*	fftDataPtr	Pointer to the FFT data location within the FFT data block

4.3 FFT DATA AREA

FFT spectra are saved in the FFT data area. They are stored contiguously as:

- status word
- array of FFT values (single precision floating point numbers)

Table 4: struct fftData.

Data Class	Variable Name	Descriptor & comments
int	status	Data status; bit0 = valid/invalid
int	reserved	used to force proper D64 alignment of FFT data
float[n]	data	array of FFT points

APPENDIX A TP LOOKUP TABLE

Table 5: Definition of test points.

Sys.	Sub.	ID #	TPName	buffer	Description
		0	invalid		
H1	LSC	1	GW_E_TI	16k	Test In, GW (L-) error signal
H1	LSC	2	CARM_E_TI	16k	Test In, Common arm (L+) error signal
H1	LSC	3	MICH_E_TI	16k	Test In, Michelson (l-) error signal
H1	LSC	4	REC_E_TI	16k	Test In, Recycling cav (l+) error signal
H1	LSC	5	GW_C_TI	16k	Test In, GW (L-) control signal
H1	LSC	6	CARM_C_TI	16k	Test In, Comm arm (TM damping) control signal
H1	LSC	7	MICH_CC_TI	16k	Test In, Michelson correction control signal
H1	LSC	8	MICH_BSC_TI	16k	Test In, Michelson beamsplitter control signal
H1	LSC	9	MICH_TMC_TI	16k	Test In, Mich. TM damping control signal
H1	LSC	10	REC_RMC_TI	16k	Test In, Rec cav, rec mirror control signal
H1	LSC	11	REC_TMC_TI	16k	Test In, Rec cav, TM damping control signal
H1	LSC	12	ETMX_TI	16k	Test In, End Test Mass, X arm
H1	LSC	13	ETMY_TI	16k	Test In, End Test Mass, Y arm
H1	LSC	14	ITMX_TI	16k	Test In, Input Test Mass, X arm
H1	LSC	15	ITMY_TI	16k	Test In, Input Test Mass, Y arm
H1	LSC	16	BS_TI	16k	Test In, Beamsplitter
H1	LSC	17	RM_TI	16k	Test In, Recycling mirror
H1	LSC	18	PHCAL_ETMX_TI	16k	Test In, Photon calibrator laser, ETM X
H1	LSC	19	PHCAL_ETMY_TI	16k	Test In, Photon calibrator laser, ETM Y
H1	LSC	100	AS1_I	16k	anti-symmetric port, diode 1, I-phase
H1	LSC	101	AS1_Q	16k	anti-symmetric port, diode 1, Q-phase
H1	LSC	102	AS2_I	16k	anti-symmetric port, diode 2, I-phase
H1	LSC	103	AS2_Q	16k	anti-symmetric port, diode 2, Q-phase
H1	LSC	104	AS3_I	16k	anti-symmetric port, diode 3, I-phase
H1	LSC	105	AS3_Q	16k	anti-symmetric port, diode 3, Q-phase
H1	LSC	106	AS4_I	16k	anti-symmetric port, diode 4, I-phase
H1	LSC	107	AS4_Q	16k	anti-symmetric port, diode 4, Q-phase
H1	LSC	108	AS5_I	16k	anti-symmetric port, diode 5, I-phase
H1	LSC	109	AS5_Q	16k	anti-symmetric port, diode 5, Q-phase
H1	LSC	110	AS6_I	16k	anti-symmetric port, diode 6, I-phase
H1	LSC	111	AS6_Q	16k	anti-symmetric port, diode 6, Q-phase
H1	LSC	112	RFL1_I	16k	reflection port, diode 1, I-phase
H1	LSC	113	RFL1_Q	16k	reflection port, diode 1, Q-phase
H1	LSC	114	RFL2_I	16k	reflection port, diode 2, I-phase
H1	LSC	115	RFL2_Q	16k	reflection port, diode 2, Q-phase

Table 5: Definition of test points.

Sys.	Sub.	ID #	TPName	buffer	Description
H1	LSC	116	POX1_I	16k	RC pick-off from ITM X, I-phase
H1	LSC	117	POX1_Q	16k	RC pick-off from ITM X, Q-phase
H1	LSC	118	POY1_I	16k	RC pick-off from ITM Y, I-phase
H1	LSC	119	POY1_Q	16k	RC pick-off from ITM Y, Q-phase
H1	LSC	120	GW_E_TO	16k	Test Out, GW (L-) error signal (after sum junction)
H1	LSC	121	CARM_E_TO	16k	Test Out, Com arm (L+) error sig (after sum junc.)
H1	LSC	122	MICH_E_TO	16k	Test Out, Mich (l-) error signal (after sum junction)
H1	LSC	123	REC_E_TO	16k	Test Out, Rec cav (l+) error sig (after sum junc.)
H1	LSC	124	MICH_CC_TO	16k	Test Out, Michelson correction control signal
H1	LSC	125	MICH_TMC_TO	16k	Test Out, Mich. TM damping control signal
H1	LSC	126	REC_TMC_TO	16k	Test Out, Rec cav TM damping control signal
H1	LSC	127	ETMX_TO	16k	Test Out, End Test Mass, X arm (after sum junc.)
H1	LSC	128	ETMY_TO	16k	Test Out, End Test Mass, Y arm (after sum junc.)
H1	LSC	129	ITMX_TO	16k	Test Out, Input Test Mass, X arm (after sum junc.)
H1	LSC	130	ITMY_TO	16k	Test Out, Input Test Mass, Y arm (after sum junc.)
H1	LSC	131	BS_TO	16k	Test Out, Beamsplitter (after sum junc.)
H1	LSC	132	RM_TO	16k	Test Out, Recycling mirror (after sum junc.)
H1	ASC	500	WFS1_YE_TI	2k	Test In, wavefront sensor 1 yaw error signal
H1	ASC	501	WFS1_PE_TI	2k	Test In, wavefront sensor 1 pitch error signal
H1	ASC	502	WFS2a_YE_TI	2k	Test In, wavefront sensor 2a yaw error signal
H1	ASC	503	WFS2a_PE_TI	2k	Test In, wavefront sensor 2a pitch error signal
H1	ASC	504	WFS2b_YE_TI	2k	Test In, wavefront sensor 2a yaw error signal
H1	ASC	505	WFS2b_PE_TI	2k	Test In, wavefront sensor 2b pitch error signal
H1	ASC	506	WFS3_YE_TI	2k	Test In, wavefront sensor 3 yaw error signal
H1	ASC	507	WFS3_PE_TI	2k	Test In, wavefront sensor 3 pitch error signal
H1	ASC	508	WFS4_YE_TI	2k	Test In, wavefront sensor 4 yaw error signal
H1	ASC	509	WFS4_PE_TI	2k	Test In, wavefront sensor 4 pitch error signal
H1	ASC	510	QPDX_YE_TI	2k	Test In, X-arm quad. pos. sensor yaw error signal
H1	ASC	511	QPDX_PE_TI	2k	Test In,X-arm quad. pos. sensor pitch error signal
H1	ASC	512	QPDY_YE_TI	2k	Test In, Y-arm quad. pos. sensor yaw error signal
H1	ASC	513	QPDY_PE_TI	2k	Test In,Y-arm quad. pos. sensor pitch error signal
H1	ASC	514	WFS1_YC_TI	2k	Test In, wavefront sensor 1 yaw control signal
H1	ASC	515	WFS1_PC_TI	2k	Test In, wavefront sensor 1 pitch controlr signal
H1	ASC	516	WFS2a_YC_TI	2k	Test In, wavefront sensor 2a yaw control signal
H1	ASC	517	WFS2a_PC_TI	2k	Test In, wavefront sensor 2a pitch control signal
H1	ASC	518	WFS2b_YC_TI	2k	Test In, wavefront sensor 2a yaw control signal
H1	ASC	519	WFS2b_PC_TI	2k	Test In, wavefront sensor 2b pitch control signal
H1	ASC	520	WFS3_YC_TI	2k	Test In, wavefront sensor 3 yaw control signal
H1	ASC	521	WFS3_PC_TI	2k	Test In, wavefront sensor 3 pitch control signal
H1	ASC	522	WFS4_YC_TI	2k	Test In, wavefront sensor 4 yaw control signal

Table 5: Definition of test points.

Sys.	Sub.	ID #	TPName	buffer	Description
H1	ASC	523	WFS4_PC_TI	2k	Test In, wavefront sensor 4 pitch control signal
H1	ASC	524	QPDX_YC_TI	2k	Test In, X-arm quad. pos. sensor yaw control sig.
H1	ASC	525	QPDX_PC_TI	2k	Test In,X-arm quad. pos. sensor pitch control sig.
H1	ASC	526	QPDY_YC_TI	2k	Test In, Y-arm quad. pos. sensor yaw control sig.
H1	ASC	527	QPDY_PC_TI	2k	Test In,Y-arm quad. pos. sensor pitch control sig.
H1	ASC	528	ETMXY_TI	2k	Test In, End test mass, X arm, yaw angle
H1	ASC	529	ETMXP_TI	2k	Test In, End test mass, X arm, pitch angle
H1	ASC	530	ETMYY_TI	2k	Test In, End test mass, Y arm, yaw angle
H1	ASC	531	ETMYP_TI	2k	Test In, End test mass, Y arm, pitch angle
H1	ASC	532	ITMXY_TI	2k	Test In, Input test mass, X arm, yaw angle
H1	ASC	533	ITMXP_TI	2k	Test In, Input test mass, X arm, pitch angle
H1	ASC	534	ITMYY_TI	2k	Test In, Input test mass, Y arm, yaw angle
H1	ASC	535	ITMYP_TI	2k	Test In, Input test mass, Y arm, pitch angle
H1	ASC	536	RECY_TI	2k	Test In, Recycling mirror, yaw angle
H1	ASC	537	RECP_TI	2k	Test In, Recycling mirror, pitch angle
H1	ASC	538	BSY_TI	2k	Test In, Beamsplitter, yaw angle
H1	ASC	539	BSP_TI	2k	Test In, Beamsplitter, pitch angle
H1	ASC	540	IBY_TI	2k	Test In, Input beam, yaw angle
H1	ASC	541	IBP_TI	2k	Test In, Input beam, pitch angle
H1	ASC	700	WFS1_1_I	2k	wavefront sensor 1, channel 1, I-phase
H1	ASC	701	WFS1_2_I	2k	wavefront sensor 1, channel 21, I-phase
H1	ASC	702	WFS1_3_I	2k	wavefront sensor 1, channel 3, I-phase
H1	ASC	703	WFS1_4_I	2k	wavefront sensor 1, channel 4, I-phase
H1	ASC	704	WFS1_1_Q	2k	wavefront sensor 1, channel 1, Q-phase
H1	ASC	705	WFS1_2_Q	2k	wavefront sensor 1, channel 2, Q-phase
H1	ASC	706	WFS1_3_Q	2k	wavefront sensor 1, channel 3, QI-phase
H1	ASC	707	WFS1_4_Q	2k	wavefront sensor 1, channel 4, Q-phase
H1	ASC	708	WFS2_1_I	2k	wavefront sensor 2, channel 1, I-phase
H1	ASC	709	WFS2_2_I	2k	wavefront sensor 2, channel 2, I-phase
H1	ASC	710	WFS2_3_I	2k	wavefront sensor 2, channel 3, I-phase
H1	ASC	711	WFS2_4_I	2k	wavefront sensor 2, channel 4, I-phase
H1	ASC	712	WFS2_1_Q	2k	wavefront sensor 2, channel 1, Q-phase
H1	ASC	713	WFS2_2_Q	2k	wavefront sensor 2, channel 2, Q-phase
H1	ASC	714	WFS2_3_Q	2k	wavefront sensor 2, channel 3, Q-phase
H1	ASC	715	WFS2_4_Q	2k	wavefront sensor 2, channel 4, Q-phase
H1	ASC	716	WFS3_1_I	2k	wavefront sensor 3, channel 1, I-phase
H1	ASC	717	WFS3_2_I	2k	wavefront sensor 3, channel 2, I-phase
H1	ASC	718	WFS3_3_I	2k	wavefront sensor 3, channel 3, I-phase
H1	ASC	719	WFS3_4_I	2k	wavefront sensor 3, channel 4, I-phase
H1	ASC	720	WFS3_1_Q	2k	wavefront sensor 3, channel 1, Q-phase
H1	ASC	721	WFS3_2_Q	2k	wavefront sensor 3, channel 2, Q-phase

Table 5: Definition of test points.

Sys.	Sub.	ID #	TPName	buffer	Description
H1	ASC	722	WFS3_3_Q	2k	wavefront sensor 3, channel 3, Q-phase
H1	ASC	723	WFS3_4_Q	2k	wavefront sensor 3, channel 4, Q-phase
H1	ASC	724	WFS4_1_I	2k	wavefront sensor 4, channel 1, I-phase
H1	ASC	725	WFS4_2_I	2k	wavefront sensor 4, channel 2, I-phase
H1	ASC	726	WFS4_3_I	2k	wavefront sensor 4, channel 3, I-phase
H1	ASC	727	WFS4_4_I	2k	wavefront sensor 4, channel 4, I-phase
H1	ASC	728	WFS4_1_Q	2k	wavefront sensor 4, channel 1, Q-phase
H1	ASC	729	WFS4_2_Q	2k	wavefront sensor 4, channel 2, Q-phase
H1	ASC	730	WFS4_3_Q	2k	wavefront sensor 4, channel 3, Q-phase
H1	ASC	731	WFS4_4_Q	2k	wavefront sensor 4, channel 4, Q-phase
H1	ASC	732	WFS5_1_I	2k	wavefront sensor 5, channel 1, I-phase
H1	ASC	733	WFS5_2_I	2k	wavefront sensor 5, channel 2, I-phase
H1	ASC	734	WFS5_3_I	2k	wavefront sensor 5, channel 3, I-phase
H1	ASC	735	WFS5_4_I	2k	wavefront sensor 5, channel 4, I-phase
H1	ASC	736	WFS5_1_Q	2k	wavefront sensor 5, channel 1, Q-phase
H1	ASC	737	WFS5_2_Q	2k	wavefront sensor 5, channel 2, Q-phase
H1	ASC	738	WFS5_3_Q	2k	wavefront sensor 5, channel 3, Q-phase
H1	ASC	739	WFS5_4_Q	2k	wavefront sensor 5, channel 4, Q-phase
H1	ASC	740	WFS1_Y_I	2k	wavefront sensor 1, yaw signal, I-phase
H1	ASC	741	WFS1_P_I	2k	wavefront sensor 1, pitch signal, I-phase
H1	ASC	742	WFS3_Y_Q	2k	wavefront sensor 3, yaw signal, Q-phase
H1	ASC	743	WFS3_P_Q	2k	wavefront sensor 3, pitch signal, Q-phase
H1	ASC	744	WFS4_Y_Q	2k	wavefront sensor 4, yaw signal, Q-phase
H1	ASC	745	WFS4_P_Q	2k	wavefront sensor 4, pitch signal, Q-phase
H1	ASC	746	WFS5_Y_I	2k	wavefront sensor 5, yaw signal, I-phase
H1	ASC	747	WFS5_P_I	2k	wavefront sensor 5, pitch signal, I-phase
H1	ASC	748	WFS5_Y_Q	2k	wavefront sensor 5, yaw signal, Q-phase
H1	ASC	749	WFS5_P_Q	2k	wavefront sensor 5, pitch signal, Q-phase
H1	ASC	750	WFS1_YE_TO	2k	Test Out, wavefront sensor 1 yaw error signal
H1	ASC	751	WFS1_PE_TO	2k	Test Out, wavefront sensor 1 pitch error signal
H1	ASC	752	WFS2a_YE_TO	2k	Test Out, wavefront sensor 2a yaw error signal
H1	ASC	753	WFS2a_PE_TO	2k	Test Out, wavefront sensor 2a pitch error signal
H1	ASC	754	WFS2b_YE_TO	2k	Test Out, wavefront sensor 2a yaw error signal
H1	ASC	755	WFS2b_PE_TO	2k	Test Out, wavefront sensor 2b pitch error signal
H1	ASC	756	WFS3_YE_TO	2k	Test Out, wavefront sensor 3 yaw error signal
H1	ASC	757	WFS3_PE_TO	2k	Test Out, wavefront sensor 3 pitch error signal
H1	ASC	758	WFS4_YE_TO	2k	Test Out, wavefront sensor 4 yaw error signal
H1	ASC	759	WFS4_PE_TO	2k	Test Out, wavefront sensor 4 pitch error signal
H1	ASC	760	WFS1_YC_TO	2k	Test Out, wavefront sensor 1 yaw control signal
H1	ASC	761	WFS1_PC_TO	2k	Test Out, wavefront sensor 1 pitch control signal
H1	ASC	762	WFS2a_YC_TO	2k	Test Out, wavefront sensor 2a yaw control signal
H1	ASC	763	WFS2a_PC_TO	2k	Test Out, wavefront sensor 2a pitch control signal
H1	ASC	764	WFS2b_YC_TO	2k	Test Out, wavefront sensor 2a yaw control signal

Table 5: Definition of test points.

Sys.	Sub.	ID #	TPName	buffer	Description
H1	ASC	765	WFS2b_PC_TO	2k	Test Out, wavefront sensor 2b pitch control signal
H1	ASC	766	WFS3_YC_TO	2k	Test Out, wavefront sensor 3 yaw control signal
H1	ASC	767	WFS3_PC_TO	2k	Test Out, wavefront sensor 3 pitch control signal
H1	ASC	768	WFS4_YC_TO	2k	Test Out, wavefront sensor 4 yaw control signal
H1	ASC	769	WFS4_PC_TO	2k	Test Out, wavefront sensor 4 pitch control signal
H1	ASC	770	QPDX_1	2k	quadrant position sensor, channel 1, X arm
H1	ASC	771	QPDX_2	2k	quadrant position sensor, channel 2, X arm
H1	ASC	772	QPDX_3	2k	quadrant position sensor, channel 3, X arm
H1	ASC	773	QPDX_4	2k	quadrant position sensor, channel 4, X arm
H1	ASC	774	QPDY_1	2k	quadrant position sensor, channel 1, Y arm
H1	ASC	775	QPDY_2	2k	quadrant position sensor, channel 2, Y arm
H1	ASC	776	QPDY_3	2k	quadrant position sensor, channel 3, Y arm
H1	ASC	777	QPDY_4	2k	quadrant position sensor, channel 4, Y arm
H1	ASC	778	QPDX_YE_TO	2k	Test Out, X-arm QPD yaw error signal
H1	ASC	779	QPDX_PE_TO	2k	Test Out, X-arm QPD pitch error signal
H1	ASC	780	QPDY_YE_TO	2k	Test Out, Y-arm QPD yaw error signal
H1	ASC	781	QPDY_PE_TO	2k	Test Out, Y-arm QPD pitch error signal
H1	ASC	782	QPDX_YC_TO	2k	Test Out, X-arm QPD yaw control signal
H1	ASC	783	QPDX_PC_TO	2k	Test Out, X-arm QPD pitch control signal
H1	ASC	784	QPDY_YC_TO	2k	Test Out, Y-arm QPD yaw control signal
H1	ASC	785	QPDY_PC_TO	2k	Test Out, Y-arm QPD pitch control signal
H1	IOO	1500	WFSMC1_YE_TI	2k	Test In, mode cleaner WFS 1 yaw error signal
H1	IOO	1501	WFSMC1_PE_TI	2k	Test In, mode cleaner WFS 1 pitch error signal
H1	IOO	1502	WFSMC2_YE_TI	2k	Test In, mode cleaner WFS 2 yaw error signal
H1	IOO	1503	WFSMC2_PE_TI	2k	Test In, mode cleaner WFS 2 pitch error signal
H1	IOO	1504	WFSMC1_YC_TI	2k	Test In, mode cleaner WFS 1 yaw control signal
H1	IOO	1505	WFSMC1_PC_TI	2k	Test In, mode cleaner WFS 1 pitch controlr signal
H1	IOO	1506	WFSMC2_YC_TI	2k	Test In, mode cleaner WFS 2 yaw control signal
H1	IOO	1507	WFSMC2_PC_TI	2k	Test In, mode cleaner WFS 2 pitch control signal
H1	IOO	1508	PZT1Y_TI	2k	Test In, PZT 1, yaw angle
H1	IOO	1509	PZT1P_TI	2k	Test In, PZT 1, pitch angle
H1	IOO	1510	PZT2Y_TI	2k	Test In, PZT 2, yaw angle
H1	IOO	1511	PZT2P_TI	2k	Test In, PZT 2, pitch angle
H1	IOO	1600	WFSMC1_1_I	2k	mode cleaner WFS 1, channel 1, I-phase
H1	IOO	1601	WFSMC1_2_I	2k	mode cleaner WFS 1, channel 21, I-phase
H1	IOO	1602	WFSMC1_3_I	2k	mode cleaner WFS 1, channel 3, I-phase
H1	IOO	1603	WFSMC1_4_I	2k	mode cleaner WFS 1, channel 4, I-phase

Table 5: Definition of test points.

Sys.	Sub.	ID #	TPName	buffer	Description
H1	IOO	1604	WFSMC1_1_Q	2k	mode cleaner WFS 1, channel 1, Q-phase
H1	IOO	1605	WFSMC1_2_Q	2k	mode cleaner WFS 1, channel 2, Q-phase
H1	IOO	1606	WFSMC1_3_Q	2k	mode cleaner WFS 1, channel 3, QI-phase
H1	IOO	1607	WFSMC1_4_Q	2k	mode cleaner WFS 1, channel 4, Q-phase
H1	IOO	1608	WFSMC2_1_I	2k	mode cleaner WFS 2, channel 1, I-phase
H1	IOO	1609	WFSMC2_2_I	2k	mode cleaner WFS 2, channel 2, I-phase
H1	IOO	1610	WFSMC2_3_I	2k	mode cleaner WFS 2, channel 3, I-phase
H1	IOO	1611	WFSMC2_4_I	2k	mode cleaner WFS 2, channel 4, I-phase
H1	IOO	1612	WFSMC2_1_Q	2k	mode cleaner WFS 2, channel 1, Q-phase
H1	IOO	1613	WFSMC2_2_Q	2k	mode cleaner WFS 2, channel 2, Q-phase
H1	IOO	1614	WFSMC2_3_Q	2k	mode cleaner WFS 2, channel 3, Q-phase
H1	IOO	1615	WFSMC2_4_Q	2k	mode cleaner WFS 2, channel 4, Q-phase
H1	IOO	1616	WFSMC1_Y_Q	2k	mode cleaner WFS 1, yaw signal, Q-phase
H1	IOO	1617	WFSMC1_P_Q	2k	mode cleaner WFS 1, pitch signal, Q-phase
H1	IOO	1618	WFSMC2_Y_Q	2k	mode cleaner WFS 2, yaw signal, Q-phase
H1	IOO	1619	WFSMC2_P_Q	2k	mode cleaner WFS 2, pitch signal, Q-phase
H1	IOO	1620	WFSMC1_YE_TO	2k	Test Out, mode cleaner WFS 1 yaw error signal
H1	IOO	1621	WFSMC1_PE_TO	2k	Test Out, mode cleaner WFS 1 pitch error signal
H1	IOO	1622	WFSMC2_YE_TO	2k	Test Out, mode cleaner WFS 2 yaw error signal
H1	IOO	1623	WFSMC2_PE_TO	2k	Test Out, mode cleaner WFS 2 pitch error signal
H1	IOO	1624	WFSMC1_YC_TO	2k	Test Out, mode cleaner WFS 1 yaw control signal
H1	IOO	1625	WFSMC1_PC_TO	2k	Test Out, mode cleaner WFS 1 pitch control sig
H1	IOO	1626	WFSMC2_YC_TO	2k	Test Out, mode cleaner WFS 2 yaw control signal
H1	IOO	1627	WFSMC2_PC_TO	2k	Test Out, mode cleaner WFS 2 pitch control sig
H1	GDS	2000	AUDIO1	16k	audio channel 1
H1	GDS	2001	AUDIO2	16k	audio channel 2
H1	GDS	2002	LSC_LF_MOD_SB	16k	modulation input of rf generator, sidebands
H1	GDS	2003	LSC_LF_MOD_NRSB	16k	modulation input of rf generator, non-res. SBs
H1	GDS	2004	LSC_LF_MOD_MC	16k	modulation input of rf generator, MC sidebands
H1	GDS	2005	LSC_CAL_ETMX	16k	calibration signal ETMX
H1	GDS	2006	LSC_CAL_ETMY	16k	calibration signal ETMY
H1	GDS	2007	IOO_MC_I_OFS	16k	modecleaner error signal offset
H1	GDS	2008	IOO_LEN_MC_OFS	16k	modecleaner length offset
H1	GDS	2009	IOO_TEST_IN1	16k	after servo split, MC path
H1	GDS	2010	IOO_TEST_IN2	16k	after servo split, laser path
H1	GDS	2011	IOO_LEN_MMT1_OFS	16k	mode matching mirror 1 offset
H1	GDS	2012	IOO_LEN_MMT2_OFS	16k	mode matching mirror 2 offset
H1	GDS	2013	IOO_LEN_MMT3_OFS	16k	mode matching mirror 3 offset
H1	GDS	2014	PSL_FREQ_AOM_OFS	16k	laser frequnecy offset, AOM
H1	GDS	2015	PSL_PWR_OFS	16k	laser power modulation