The LIGO Timing System

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G030257-00-D

Design/Requirements

- 10μs absolute calibration of incoming GW waves
- 1μs clock accuracy
- Use a GPS master clock in all buildings
- Use IRIG-B slaves in each VME crate (UTC – GPS leap seconds)
- Synchronize the ADC modules using a hardware clock signal
- Use a NTP server for the control room workstations

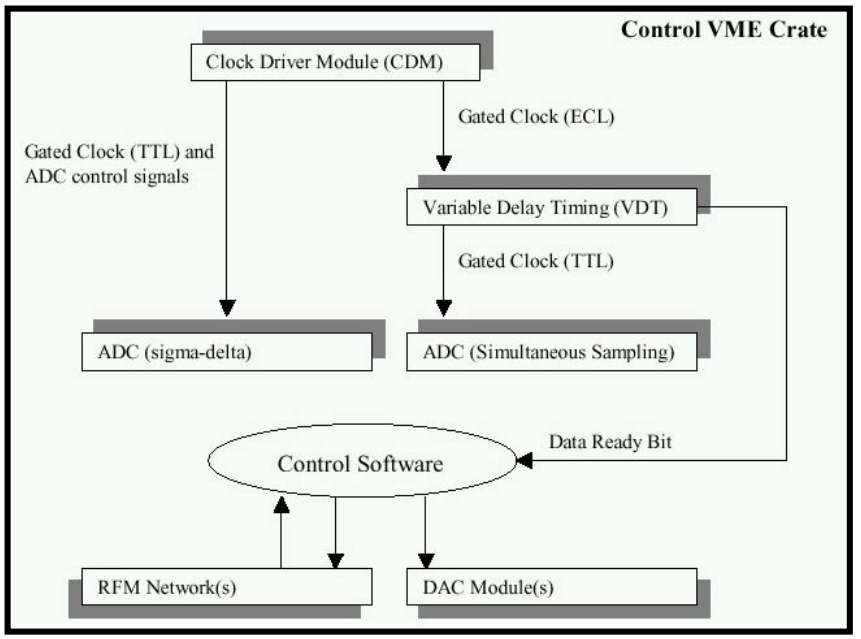
Implementation

- GPS master in DAQ controller for timestamp
  - 1 second mark
- Second GPS master with a 2^{24}Hz quartz oscillator
  - Feeds clock driver module (1pps and 2^{22}Hz)
  - Ramp signal at 1pps, IRIG-B slave signal
  - Trigger signals for ADC modules
- Data collection: reflective memory loop
  - 1/16s buffers, 1/2s ring buffer
  - Collected and time stamped by DAQ controller (1s)
  - 2s ring buffer to frame builder (1/16s buffers)
  - 16s frame files
- Excitations are written to refl. mem. (using GPS time)
- Photon Calibrator

Front-End / T020196
Rolf Bork, Dale Ouimette

- Initialization/Auto-resync
- Diagnostics
  - GPS Ramp => absolute
  - CPU meter overload
    => lost IO cycles
  - Polling ADC/Clock ready bit
    ADC ready at the same time as clock?
    => late ADC samples
  - Resync counter
    ADC ready at end of processing?
    => missed ADC samples
  - Cycle count
    Everyone on the same sample count?
    => inter-crate synchronization

- Processing Time @ 16kHz
  - LSC: 46µs, LVEA LOS: 56µs,
    ETM: 45µs, MC2: 27µs



Timing Diagram