

L-Bus Proposal

CDS Meeting, June 23, 2004 Paul Schwinberg, Daniel Sigg



Goal

- Eliminate the cross-connects used by EPICS controls
 - Simplify the EMI retrofit
- Replace with design that can operate in low noise environment
 - Mass-termination on backplane
 - Single controller with serial interface
 - Modern bus-type design for both analog and digital
- Clean up the power supplies
 - Locally regulated
- Support of legacy boards



Pros

- Drastic reduction of inter-system cabling
- Isolated power supplies
- Reduce susceptibility to EMI problems and noise injection
- Reduce documentation headaches because boards and interfacing go together
- Modifications are easier (new boards don't require re-cabling)
- Going forth and back between two designs is straight forward
- Better testing (boards AND subsystems can be fully tested in the shop without a custom rig)
- Support for loading and storing a digital word
- Sound infrastructure for advanced LIGO?

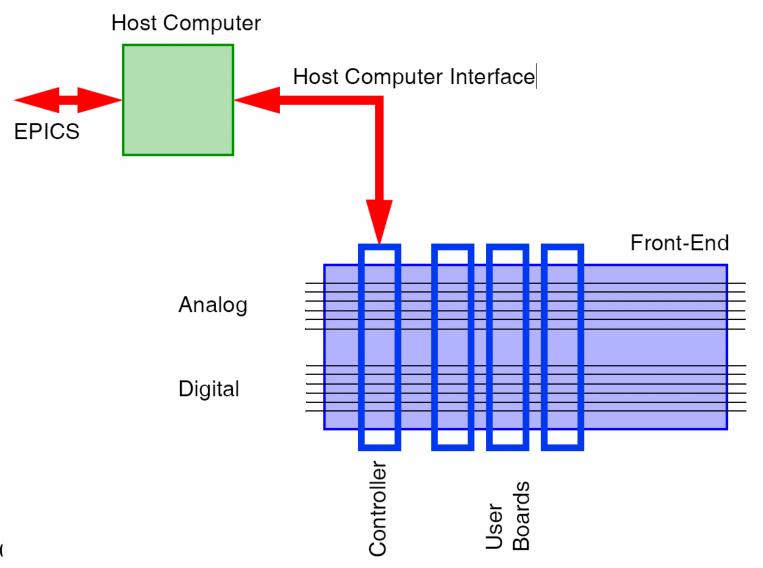


Cons

- Increased complexity (nothing is simpler than a cable!)
- Custom scheme of mass-termination
- Requires a commitment/Are we locked in?
- Requires a lot of individual interfacing for legacy boards



Basic Layout



G040



Analog Backplane

- □ 16 lines of analog readbacks
 - > Each board selects one line
 - ➤ Single ADC on controller board that operates at 2048 Hz (16 lines x 16 addresses x 16 Hz)
 - GPS synchronized
- 4 analog addresses for multiplexing 16 analog readbacks on each board
- 8 analog control lines
 - Used by boards that need to adjust voltages during running
 - Typically DACs are on the user board



Digital Backplane

- Modern memory mapped architecture
- Multiplexed 16 bit address/16 bit data
 - Boards typically use a 8 bit board identification
 - Up to 128 words can be used locally
- Simple bus interface
 - Address strobe/write indicator/data latch
- □ Low speed to minimize EMI problems
- Supports zero activity during science running
- Separate power supply



Power Supplies

- Voltages:
 - > +5V at 1A/board, digital, linear post-regulation
 - > ±5V at 1A/board, analog, linear post-regulation
 - > ±15V at 0.5A/board, analog, linear post-regulation
 - > ±24V at 1A/board, unregulated, use for local post-regulation
- Voltage monitoring
 - > ± 5% tolerance
- On/off switch



Form Factor

- Eurocrate
 - > 6U height, 220 mm depth (60 mm deeper than current boards)
 - Full (21 slots) and half (10 slots) backplanes
 - > EMI compliant enclosure
 - Support of legacy boards through 60 mm interface adapter
- Stand-alone chassis
 - Everything goes...
- □ (Field module)



Software

Dumb controller

- Supports reads, writes and read-modify-writes
- Supports 16 Hz data dump of analog readbacks
- Simple protocol to host computer (command, payload, return)

Host computer provides EPICS and DAQ interface

- Runs EPICS database
- Talks to controller to set data values based on EPICS commands and to update readbacks
- ➤ Implements data dump to DAQ system to avoid EDCU bottleneck and maintain timing information



Plan

- Prototype by end of year (optimistically)
 - ➤ Estimated costs: 10K-15K (buy crate, develop backplane, build power supply, develop controller, develop 1 user board and write software)
 - Support of high density SMD components in EE shop(?): ~15K
 - Support for EPROM/GAL/etc. burner in EE shop(?): ~5K
- Decision of go-ahead before LHO EMI retrofit is set into motion and depending on prototype results