VIRGO Control System Upgrade: Multi-DSP Board

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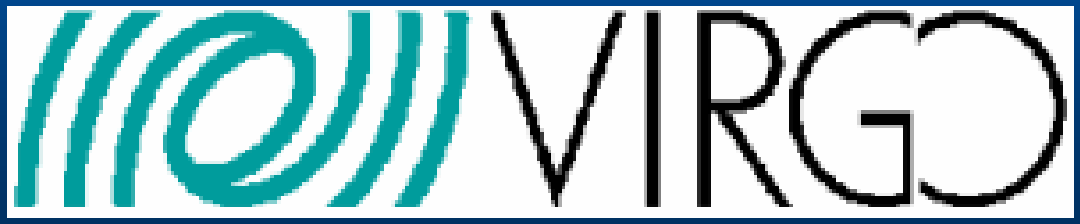
INFN Pisa

LIGO-G070351-00-Z



Introduction

- **Motivations: the control system currently in use is operative since 1998 (project started in 1994) and it is now approaching its limits in terms of performances for available computational power, converters dynamical range and components availability**

- **R&D "VIRGO Control System Upgrade" founded by EGO and focused on the upgrade of the main control loops of Virgo (suspensions, injection, locking and alignment) aiming to faster and higher dynamical range control systems**

  - **Task #1. New Digital Signal Processor (DSP) board (INFN Pisa)**
  - Task #2. New Digital Optical Link (DOL) board (LAPP Annecy).
  - Task #3. New Timing System Interface (LAPP Annecy).
  - Task #4. New analog-to-digital converter (ADC) board. (LAPP Annecy)
  - Task #5. New digital-to-analog converter (DAC) board. (INFN Pisa)

VSR1 DSP Usage (Samp. Freq = 10 kHz)

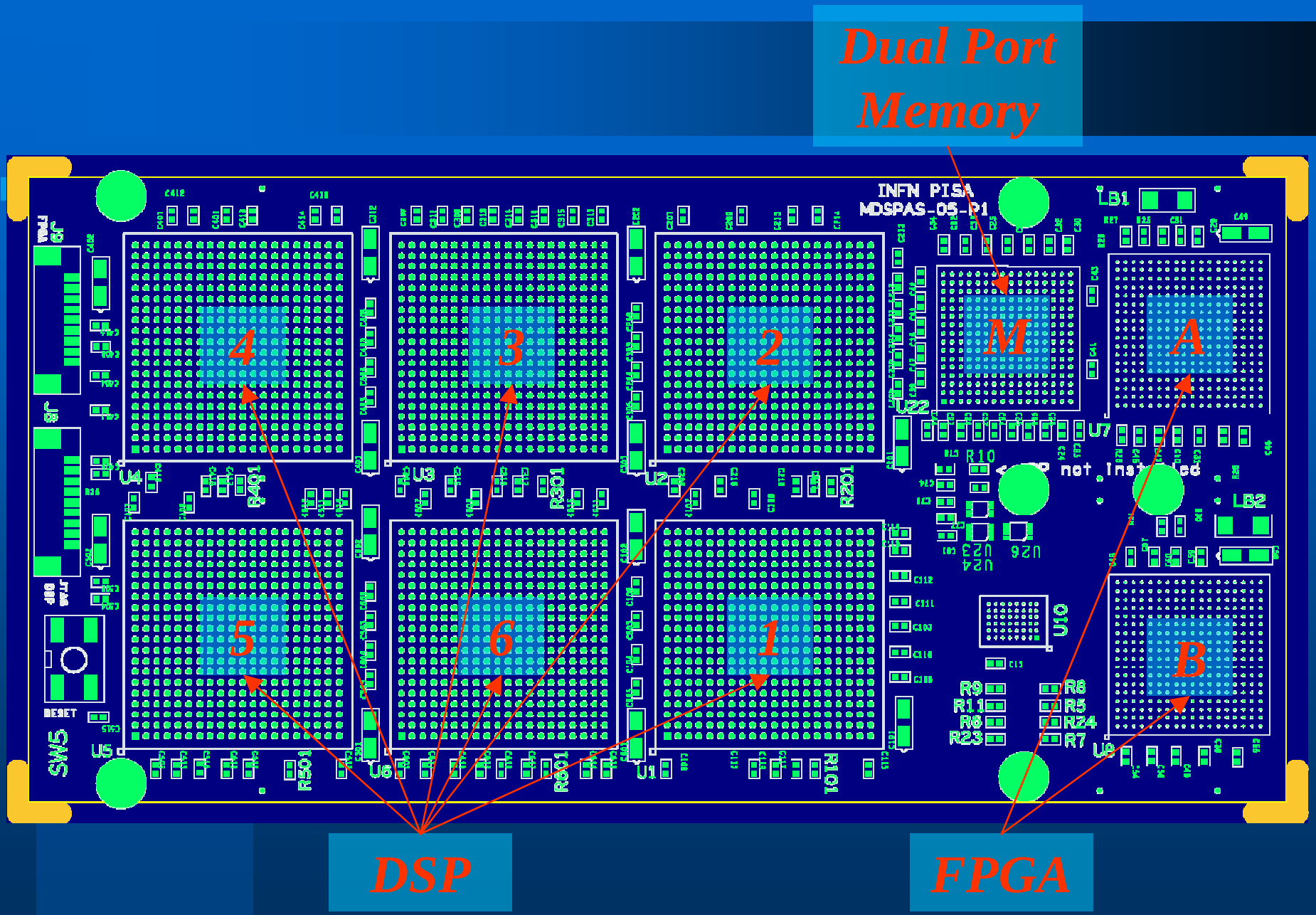
DSP	Program Memory (kBytes)	Data Memory (kBytes)	MFLOPS (Average)	MFLOPS (Sust.)	I/O (Mbit/sec)	% Used
BC	6.6	1.3	7	13	16.0	55%
BS Down	9.3	1.6	10	14	18.9	77%
BS Up	7.6	1.9	11	17	15.7	63%
IB Down	8.8	1.6	10	14	12.8	73%
IB Up	7.0	1.7	9	16	14.4	59%
MC Down	9.3	1.9	12	16	17.0	78%
MC Up	6.9	1.9	10	18	13.4	57%
NE Down	9.5	1.8	11	14	19.5	79%
NE Up	7.6	1.9	11	17	16.0	64%
NI Up	7.6	2.0	11	17	15.7	64%
NI Down	8.7	1.7	11	15	17.6	73%
OB Down	5.7	1.1	8	16	17.0	47%
OB Up	6.8	1.8	9	17	13.4	57%
PR Up	7.4	1.9	10	17	15.4	62%
PR Down	8.3	1.7	11	15	15.4	70%
WE Up	8.8	2.1	12	16	21.8	73%
WE Down	9.4	1.8	11	15	18.9	78%
WI Down	8.8	1.7	11	15	17.6	73%
WI Up	7.7	2.0	11	17	15.7	64%

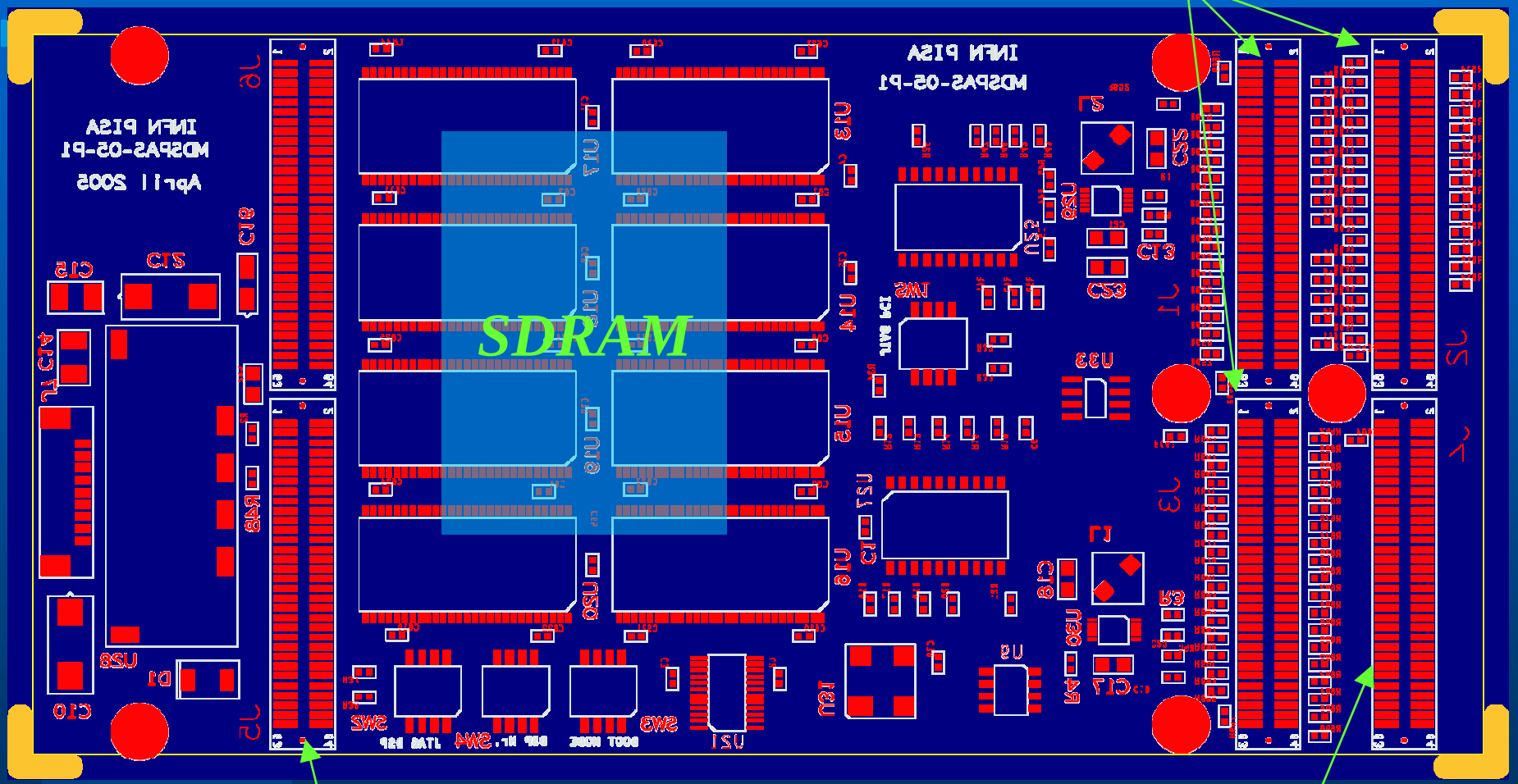
New DSP Board Specs

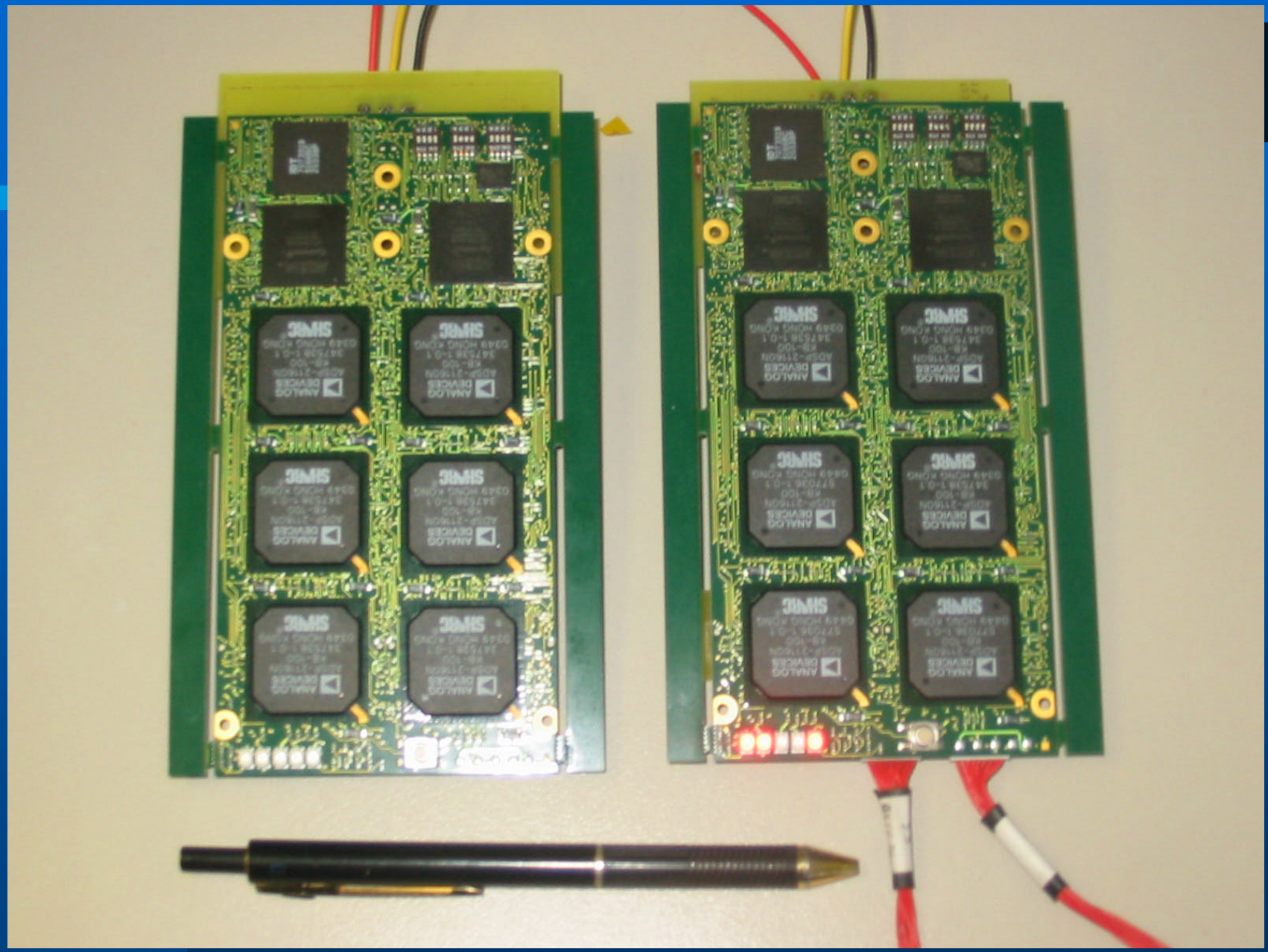
- 6 x 100 MHz ADSP211160N SHARC DSP (3.6 GigaFLOPS in single PMC Mezzanine)
- 1800 MB/s of low latency inter processor communication bandwidth
- 512 MB SDRAM, 4Mbit FLASH EPROM
- 64-bit 66 MHz PCI bus
- 256 kWord real Dual Port memory (PCI – DSP Local Bus)
- DSP LB to VSB bridge for I/O devices access
- 200 MB/s auxiliary I/O bandwidth
- IEEE 1149.1 JTAG Standard Test Access Port
- 2 x Altera EP1C4 Cyclone FPGA.

Overview

- **The new multi-DSP board is a major improvement for available computational power, condensing in a 149 x 74 mm board, dissipating about 4 Watt, the computational power of 3 PC of last generation**
- **Additional computational power provided by multi-DSP boards will contribute to improving performances anywhere digital processing is required. MIMO and adaptive controllers could be easily implemented, with major advantages from the so called “control noise” point of view.**
- **Multi-DSP computing units, will allow operation at high sampling rate and high resolution thus allowing extending applications range.**


Dual Port Memory
INFN PISA
MDSPAS-05-P1
4
3
2
M
A
5
6
1
B
DSP
FPGA

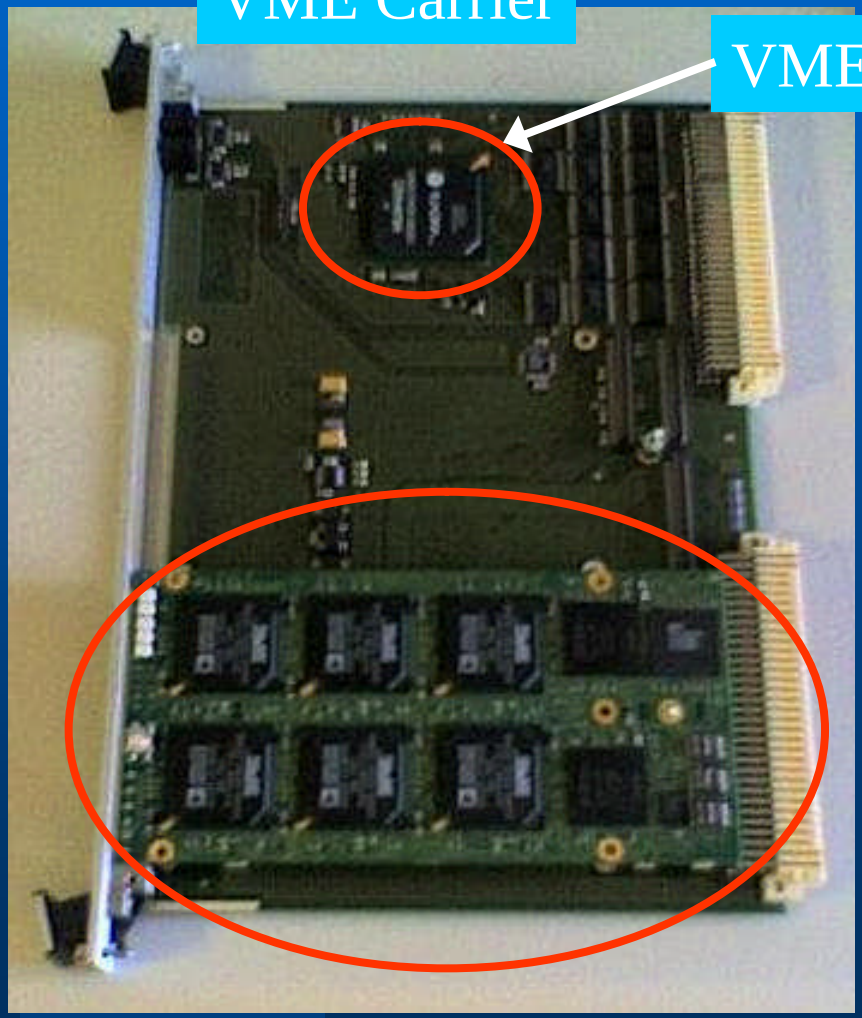

PCI 64 – 66 MHz
SDRAM
I/O → TimDOL
VSBbus



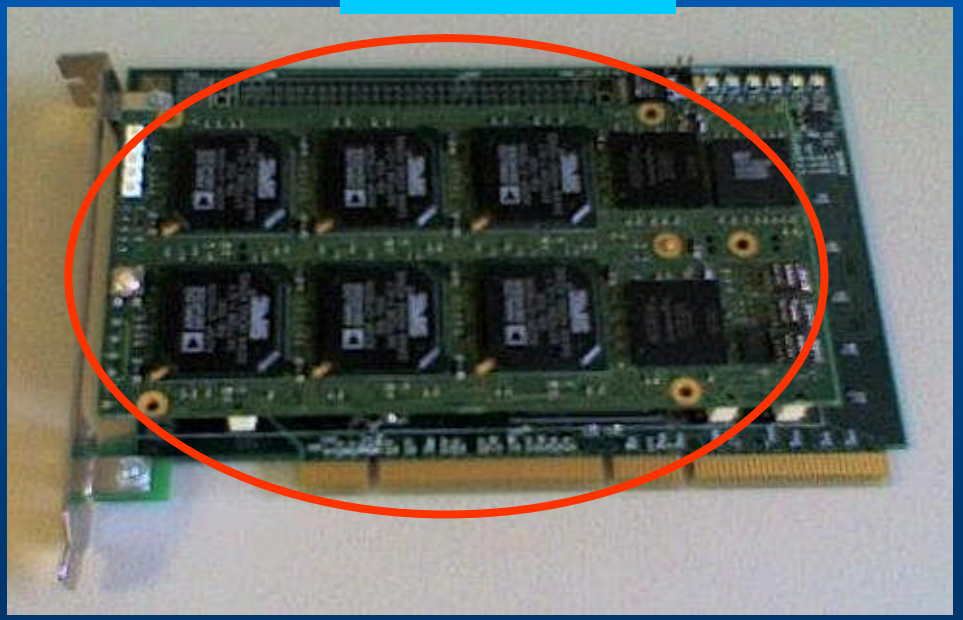
Hardware Environment

VME Carrier

VME-PCI Bridge



PCI Carrier



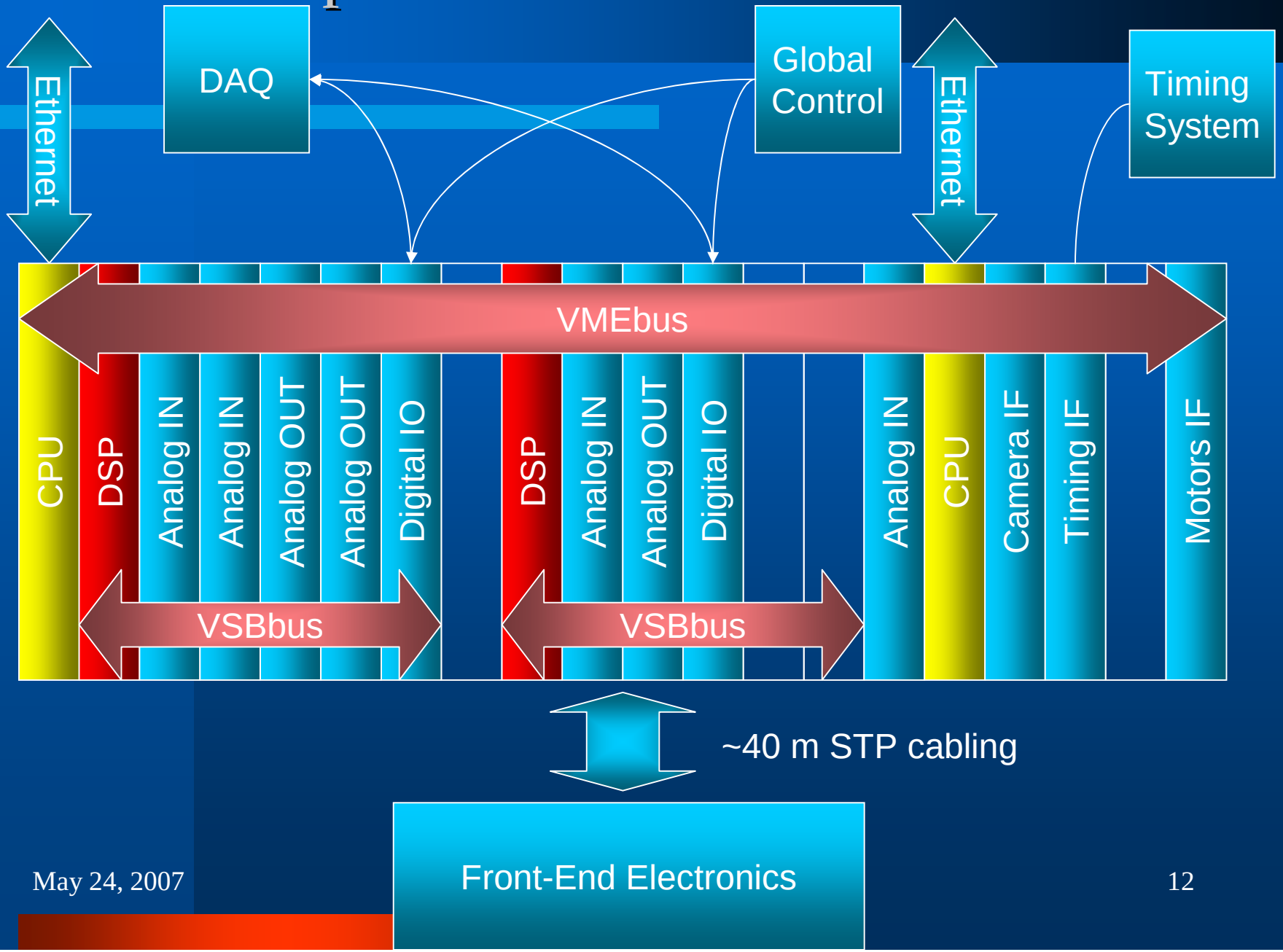
Platforms

- **VME**
  - **Motorola PPC – (LynxOS) – VME PMC Carrier**
  - **Intel x86 – (Linux) – VME PMC Carrier**
  - **Intel x86 – (Linux) – OnBoard PMC site**
- **PCI**
  - **Intel x86 – (Linux) – PCI PMC Carrier**

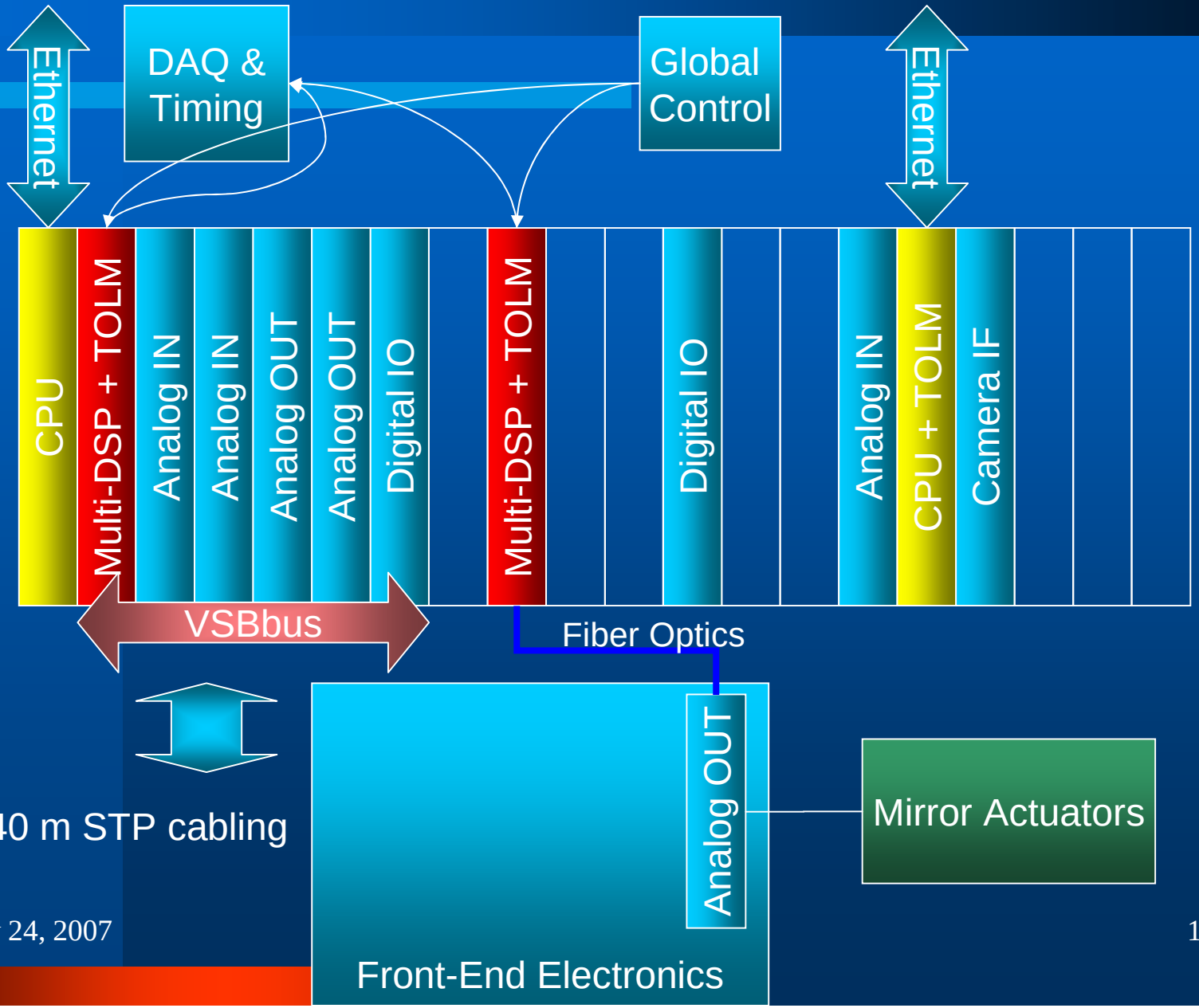
In VIRGO

- **Reference Solution**
  - **VME CPU (LynxOS or Linux)**
  - **Custom VME PMC (2 Sites) Carrier**
    - **Why “Custom”?**
      - **DSP → Link Port → “New” DOL (TOLM)**
      - **DSP → VSB → Analog IO**
      - **DSP → VSB → “Old” DOL**

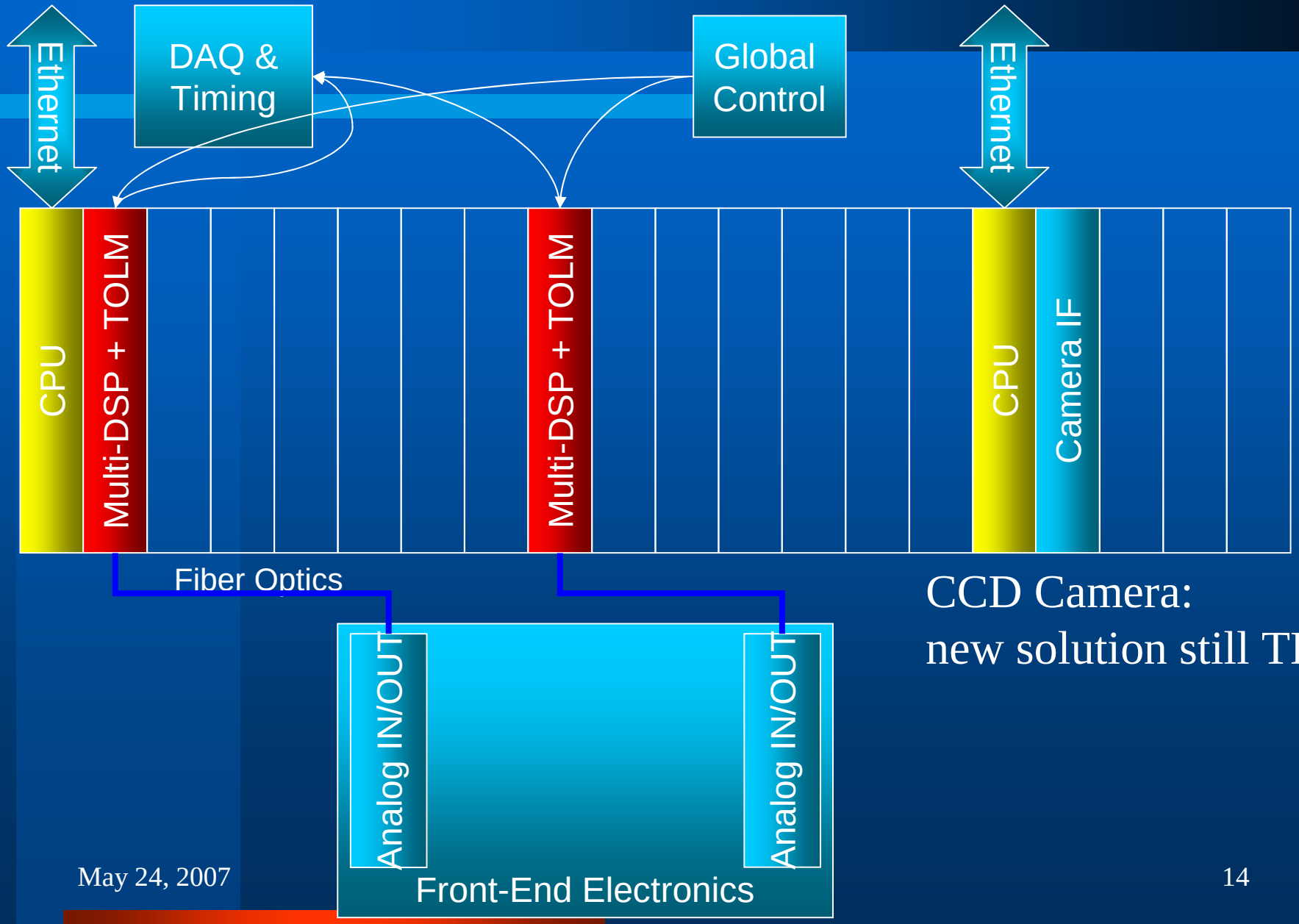
VSR1 Suspension Control Unit



VIRGO+ Suspension Control Unit



Advanced VIRGO



CCD Camera:
new solution still TBD

Software

- **Damping Compiler**
  - **Source code developed for DSP in use now will compile for the new platform**
- **New Suspension Control Software**
- **Analog Devices VisualDSP++**

Main Steps Towards VIRGO+

- **May 2005**
  - **MDSPAS-05-P1 First prototype (1 device)**
- **May 2006**
  - **MDSPAS-06-P2 Second prototype (4 devices)**
- **December 2006**
  - **MDSPAS-07-A Order placed for first release (50 devices)**
- **May-June 2007**
  - **Place order for carrier board manufacturing**
- **September 2007**
  - **Test New DSP with Old Suspension Control Unit**
  - **Test TOLM – New DSP – DAQ Integration Test**
- **Missing**
  - **Installation plan (installation now foreseen Q1-Q2 2008)**

Related Documents

- **Design**
  - **VIR_SPE_PIS_4900_120,** *New DSP Final Design Document*
- **Budget & Planning**
  - **VIR_SPE_PIS_4900_118,** *New DSP Board 2005 Budget*
  - **VIR_SPE_PIS_4900_128,** *New DSP Board 2006 Budget*
  - **VIR_SPE_PIS_4900_135,** *New DSP Board 2007 Budget*
- **Review**
  - **VIRGO Control System Upgrade, Pisa Activities Report, September 30th, 2004**
  - **VIRGO Control System Upgrade, Pisa Activities Report, April 16th, 2005**
  - **VIRGO Control System Upgrade, Pisa Activities Final Report, June, 2006**
- **Software**
  - **https://workarea.ego-gw.it/ego2/ego/itf/software/auth-only/projects/superattenuator-control-software**

How use 3 GFLOPS?

- **Digital Feedback Design in VIRGO**
  - **Classical Design Methods**
    - **Discrete-time controllers derived from continuous-time controllers (indirect design techniques)**
      - **Design a continuous-time controller and then obtain the corresponding discrete-time controller using a transformation from G(s) to G(z).**

Feedback Design Methods

- **Classical Design Methods (SISO)**
  - **Root locus method**
  - **Nyquist techniques (design based on frequency response)**
  - **PID Controller design methods**
    - **Transient response method**
    - **Stability limit method**
- **State Space Design Methods (SISO – MIMO)**
  - **Pole Placement**
  - **Optimal Control - LQG Methods**
  - **H-Infinity**
  - **Youla parameterization**
  - **μ-synthesis**
  - **...**
- **Adaptive Control**
  - **Model Reference adaptive control**
  - **Self-tuning regulators**
  - **…**

Additional computational power will allow implementing MIMO and adaptive controllers.