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Converter Design Update

Advanced LIGO CDS Meeting, Aug 1, 2006

Daniel Sigg, Paul Schwinberg, Josh Myers

G060375-00-D

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Features of Present System

- Collocation of analog and digital
- Poor noise performance
- Inadequate throughput
- Limited timing support
- Convoluted data paths
- High costs

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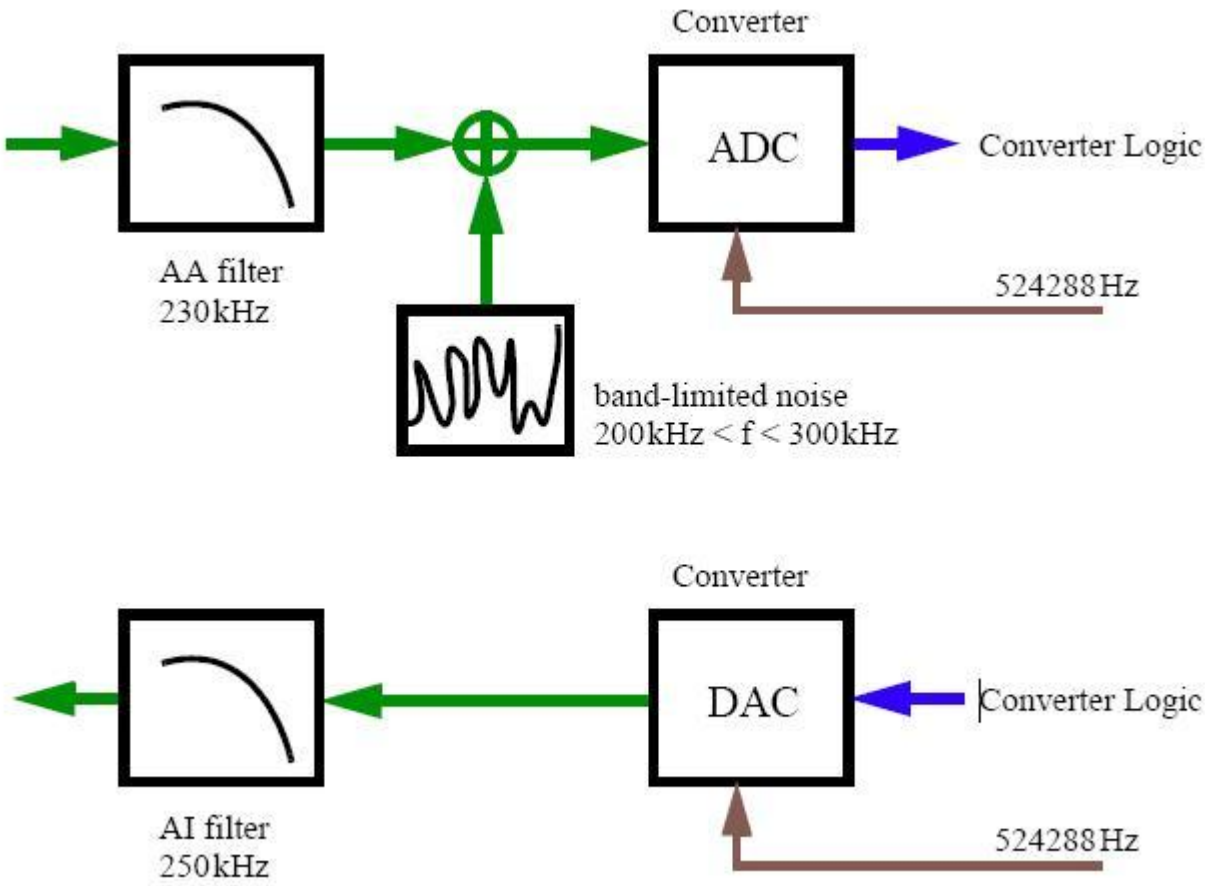
Requirements

- Timing
  - Absolute timing precision relative to UTC: 1μs
  - Guaranteed (no counting of cycles forever)
  - Latency between converter and processor: < 5μs
- Noise
  - Converter range: ±10V SE or ±20V DE
  - Converter noise: 100–300nV/√Hz (SE, best effort)
  - No electrical connection between converters and processors (fiber)
- Others
  - No restriction on converter location
  - Detection of transmission errors
  - Support for diagnostics

Analog Front-End



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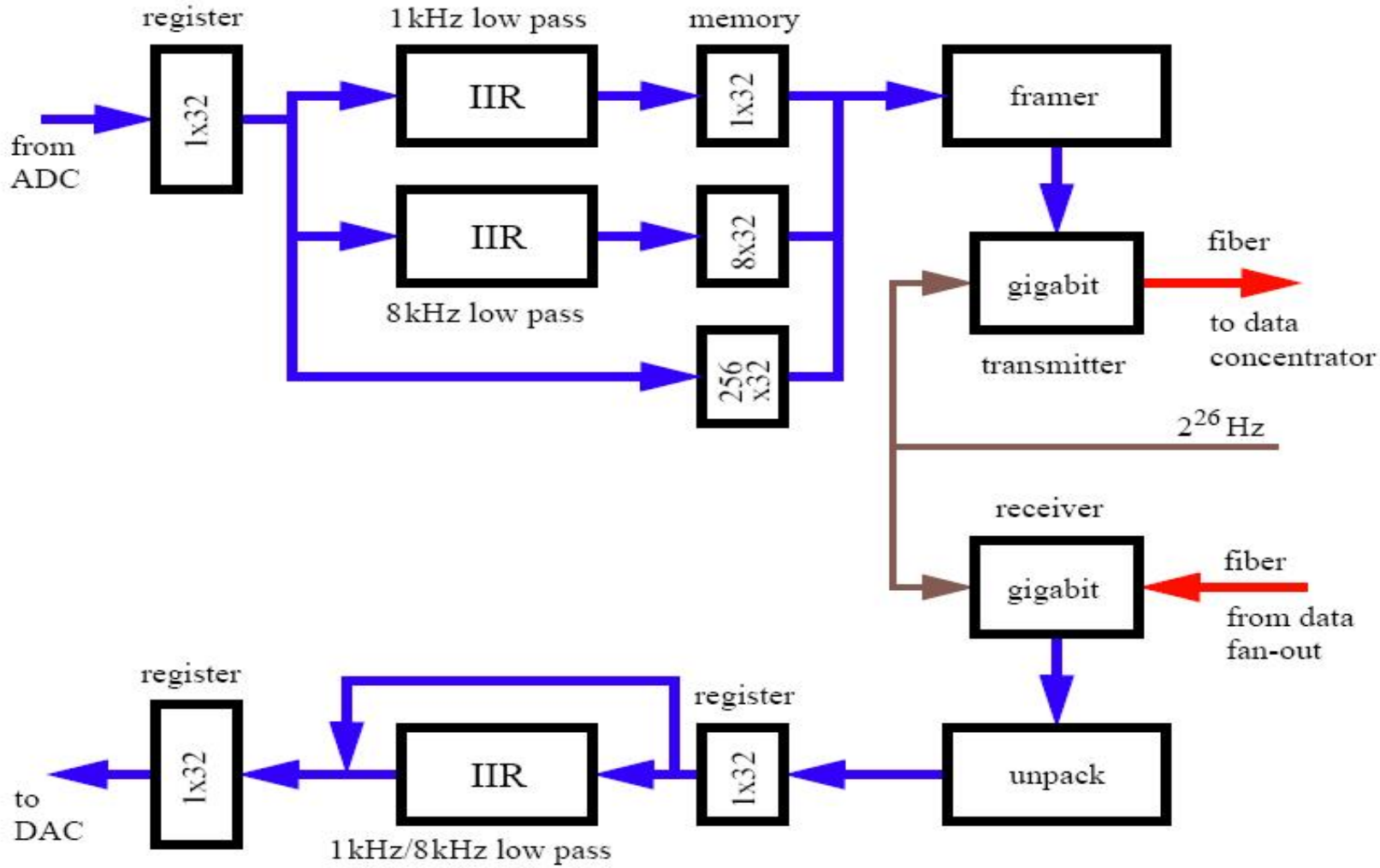
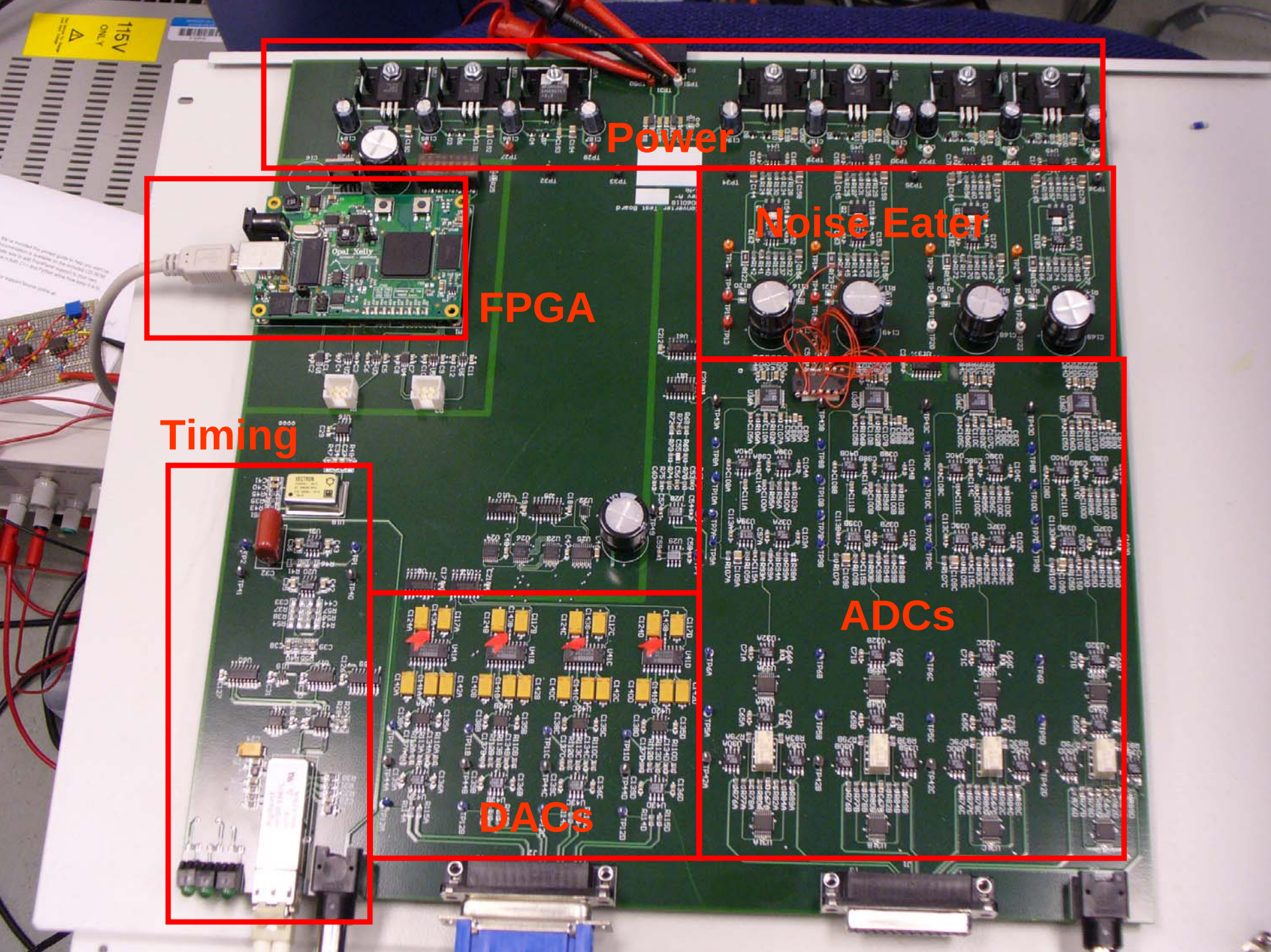
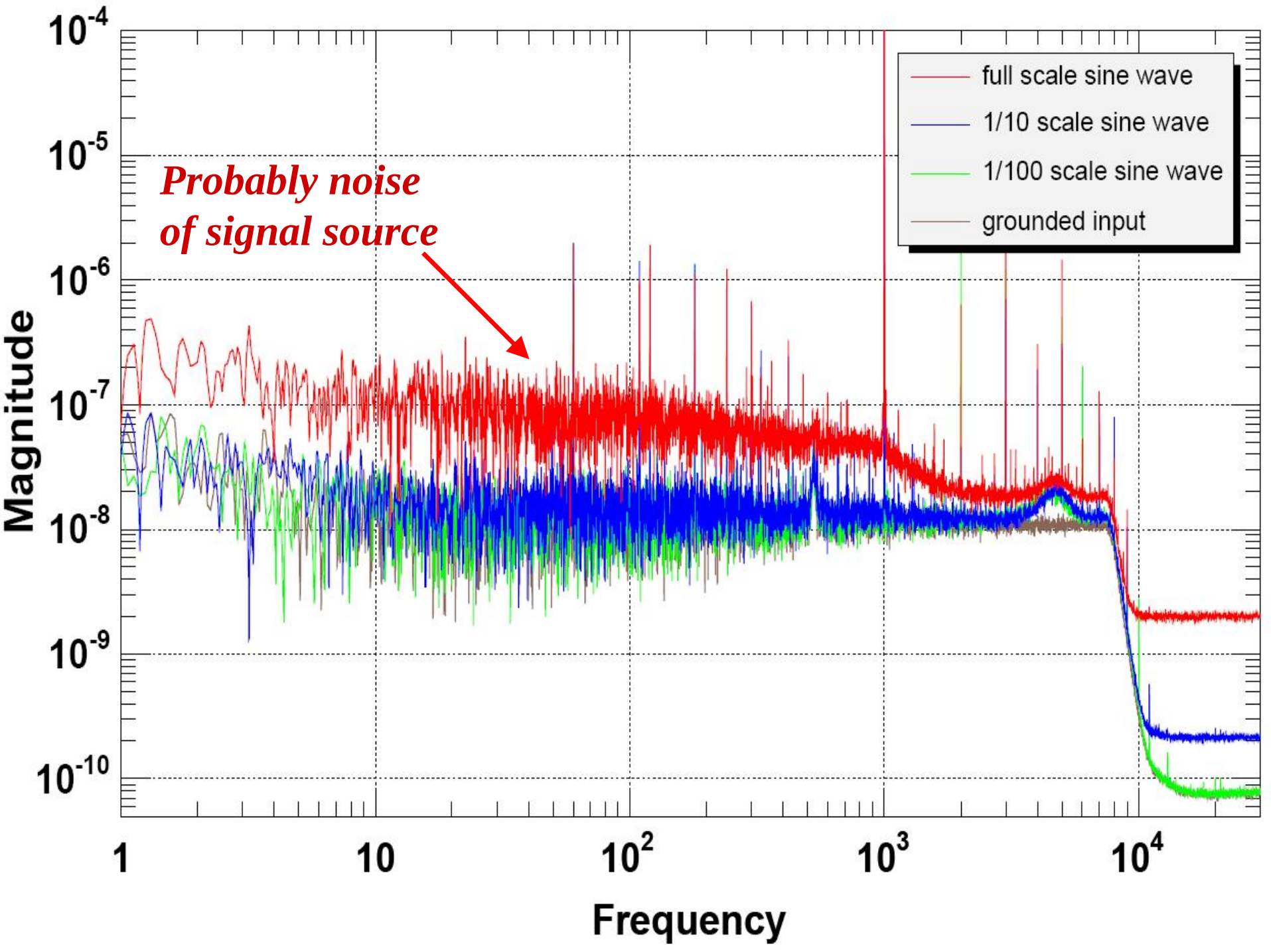
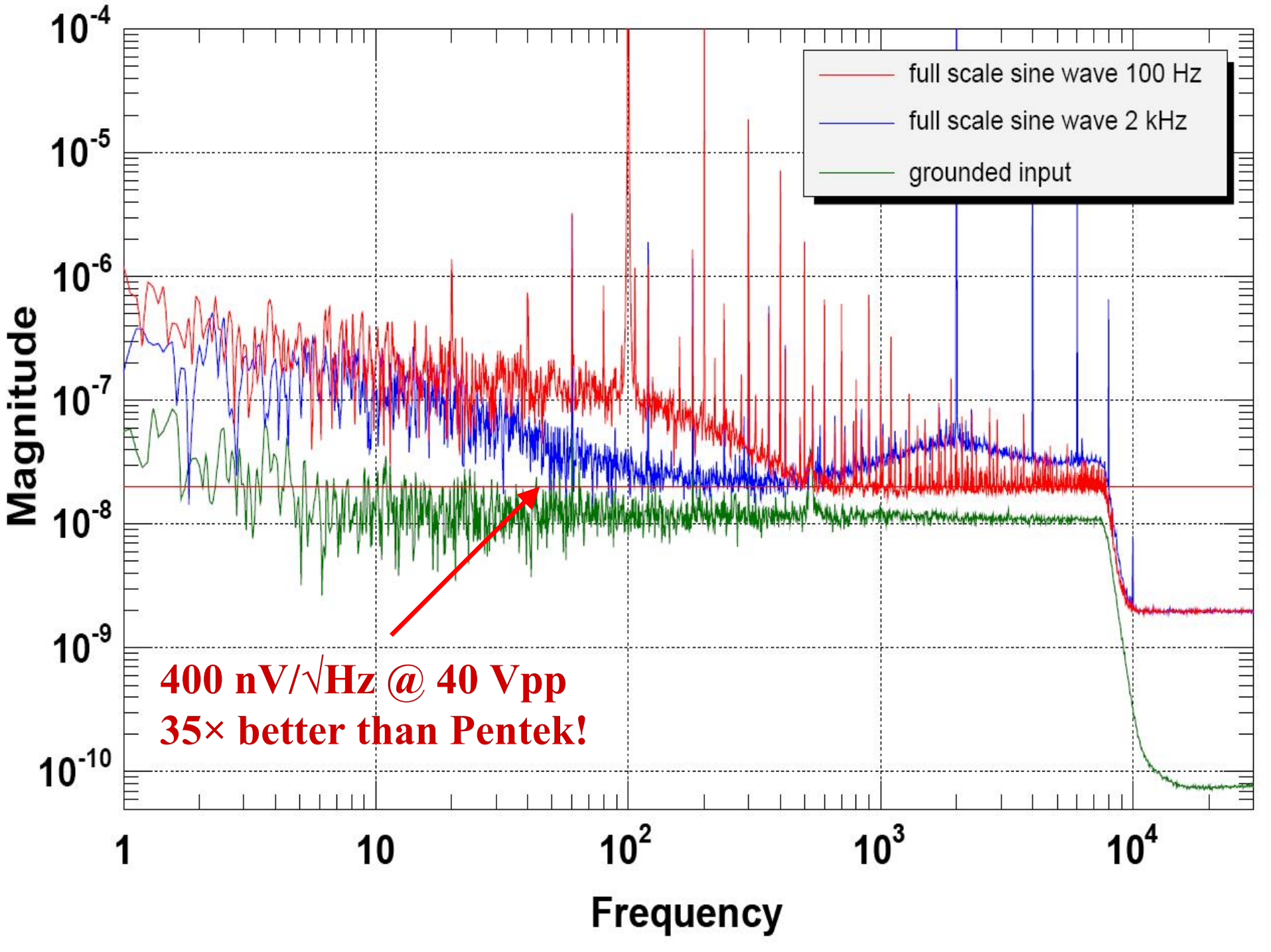
Digital Front-End




Power
FPGA
Noise Eater
Timing
ADCs
DACs


Probably noise
of signal source
full scale sine wave
1/10 scale sine wave
1/100 scale sine wave
grounded input
Magnitude
Frequency
10^-4
10^-5
10^-6
10^-7
10^-8
10^-9
10^-10
1
10
10^2
10^3
10^4


full scale sine wave 100 Hz
full scale sine wave 2 kHz
grounded input
Magnitude
Frequency
10^-4
10^-5
10^-6
10^-7
10^-8
10^-9
10^-10
1
10
10^2
10^3
10^4
400 nV/√Hz @ 40 Vpp
35× better than Pentek!

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Plans

- Finish evaluation of converter test board
  - Use new Audio Precision analyzer (maybe add AES/EBU interface)
  - Wrap up in Fall 2006
- Get an FPGA test board with gigabit fiber interfaces
  - Uplink development till end of 2006
- Develop a 1U ADC and/or DAC chassis
  - ~8 channels per chassis with timing and uplink
  - Prototype developed by mid next year
- Integrated chassis/crate
  - Requires location plan
- Fast Servo Loops?
- Slow Controls?

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Other Documents

- T050042: Proposal for a new Converter Design
- T050060: Implementing an IIR Filter in Hardware
- D060118: Converter Test Board
- T060082: Converter Backplane
- Wiki: UplinkDesign: Gigabit Ethernet Uplink Ideas
- Rachel Reddick's SURF report (soon)