Split Whitening Board Driver Test Procedure
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1. Overview

The following checkout procedure pertains to the 8-Channel Split Whitening Chassis variant of the aLIGO ISC Whitening Chassis D1002559 using D1300520 front board. The documents associated with this design have links to schematic and panel files for all the associated components.

This board functions as an interconnect point to allow splitting the normal bank of eight analog inputs into two banks of four. Channels 0 to 3 still function in the same manner as other ISC whitening chassis, but the connector associated with channels 4 to 7 serves as the readout and control interface for the aLIGO OMC DCPDs.

Testing this board is trivial, as much of its functionality is passive in nature much like a connection point. Provided the connection paths are properly soldered, the board will serve its intended function. There are several regulated voltages used in conjunction with the DCPDs, these parameters will be recorded along with the DCPD Transimpedance test switch functionality.

2. Procedure and Data

As indicated in the table below, record the observations and voltages. When needed for current readings, power the board by applying +/- 15VDC (+/- 0.1VDC), to test points TP6 and TP7 respectively. For all other measurements, connect to mating whitening PCBs in chassis for power.

Parameter	**Requirement**	**Observed**
Board Serial Number	N/A	
+15 VDC Current	40mA, +/-5mA	
-15 VDC Current	25mA, +/-5mA	
J4 Pin 8, wrt GND (Bias 1)	+11.9VDC, +/-20mVDC	
J4 Pin 4, wrt GND (Bias 2)	+11.9VDC, +/-20mVDC	
J4 Pin 21, wrt GND (Z Switch Head 1)	+5VDC then 0VDC, +/-20mVDC Z Switch HI/LO	
J4 Pin 17, wrt GND (Z Switch Head 2)	+5VDC then 0VDC, +/-20mVDC Z Switch HI/LO	
J4 Pin 2, wrt GND	+15 VDC, +/-100mVDC	
J4 Pin 3, wrt GND	-15 VDC, +/-100mVDC	
J4 Pin 6, wrt GND	+15 VDC, +/-100mVDC	
J4 Pin 7, wrt GND	-15 VDC, +/-100mVDC	
DCPD 1&2 Power LEDs on front panel	All Lit	