Serial Number: S1000573 Date: 10/28/13

Tech: Alexa

LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

-LIGO-

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**Test Procedure for RF Oscillator Source.
Advanced LIGO**

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1 Introduction

The following Test Procedure describes the test of proper operation of the Frequency Locking Slave which locks the frequency of an external oscillator to the 1PPS synchronous timing signal.

2 Test Equipment

- Bench supplies for +12V and ±24V
- Stanford Research SR785 analyzer
- Voltmeter
- Oscilloscope
- RF Power meter
- Wenzel Phase noise measurement unit
- Wiki Board Schematics
  D080702-A Assembly
  D080705-C Oscillator board
  D080665-B 1 PPS locking board
  D070071-C Timing slave
  D080709-A Push wheel board
  D080708-B Power board

3 Tests

In the Test Procedure, ground will be denoted with GND. Measured voltages on the Power Board or Test Daughterboard should be referenced to GND.

1) Verify the proper current draw. Using a bench DC power supply apply +12V to the *Chassis*. Measure the current draw of the board. Check the voltage on TP1 of the power board. Check if the power LED (DS3) is ON after you apply the voltage.

+12V at < 700 mA	Measured: mA	Pass	Fail
TP1 at +12V ± 5%	Measured: V	Pass	Fail
Power LED is on		Yes	No

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2) Check that the JTAG connector works properly. Connect the JTAG Interface to the JTAG connector of the *Slave*. Reset and then program the PROM on the *Slave* with the *FGPA_SLAVE_1PPS* program. Cycle the power. In the Altium Designer program, open the digital I/O unit called U_HZ. In the upper left corner of the window, the JTAG variable should be 0 if the program has loaded properly.

JTAG connector works properly	Yes	No

For the following tests the FGPA_SLAVE_1PPS program should be loaded onto the Slave board, and the Slave should be connected to a FanOut (or Master) board with 2xLC optical fiber. The optical fiber should be connected to the SYNCIN connector (J1) of the Slave through an SFP Transceiver module with optical 2xLC connector. This transceiver module is removable and should be placed in the SFP connector of the board. The test point TP2 (CTRL) is located on the Slave board underneath. It is accessible from the side.

3) Verify the proper operation of HF PLL. Using a Voltmeter measure the voltage on the Control Mon output TP2 (CTRL). With no SYNCIN signal, the control voltage should be at the positive rail, which is ~9.5V, indicating that the loop is unconnected. The 1PPSIN LED (DS1) should be off. Now connect the optical fiber with the SYNCOUT signal from the *FanOut* (or *Master*) to the SYNCIN connector (J1). First, the 1PPSIN LED (DS1) should be ON for 250 ms and OFF for the next 250 ms (thereafter, '2 *Hz blink*'), indicating that the board receives the SYNCIN signal, but it is not locked to the *FanOut* (or *Master*) yet. After locking, the LED will be ON for one second and OFF for the next second (thereafter, '½ *Hz blink*'). For this part of the Test a ½ *Hz blink* should be observed. If HF PLL is locked, the control voltage will no longer be railed and should be roughly 5V. Record the locked control voltage. Also check if the power draw of the *Slave* has changed significantly due to the connection of the optical fiber (a significant change shows improper operation - some components are probably shorted).

TP2 (open) at >9V	Measured: V	Pass	Fail
TP2 (connected) at 5V ± 3V	Measured: V	Pass	Fail
1 PPSIN LED works properly (exhibits ½ *Hz blink*)		Yes	No

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4) Write down the value of the VCXO Control ADC and compare with the analog readback. In Altium Designer, open the U_Test digital I/O of the *FGPA_SLAVE_1PPS* program. Compare the value of the variable VCXO_CONTROL[15..0] (shown with decimal numbers) with the Control Mon output TP2 (CTRL) on the *Slave*. The value of VCXO_CONTROL[15..0] can be converted to Volts with the following formula:

V_VCXO [V] = VCXO_CONTROL[15..0] / 65536.

If the ADC works properly, V_VCXO and TP2 should be roughly equal. Check it for the cases of connected and disconnected optical fiber separately.

V_ VCXO (open)	Measured: V	Pass	Fail
V_VCXO (connected)	Measured: V	Pass	Fail
ADC works properly		Yes	No

5) The Push Wheel switches are needed to set the frequency, so make sure they are installed and connected, removing the FPGA power while connecting them. After connecting the switches reapply power to the FPGA so there is power for the internal pull ups. While cycling each switch from 0 to 9 read the corresponding number in the 'U_HZ' FPAG test instrument.

S1	If failure, describe:	Pass	Fail
S2	If failure, describe:	Pass	Fail
S3	If failure, describe:	Pass	Fail
S4	If failure, describe:	Pass	Fail
S5	If failure, describe:	Pass	Fail
S6	If failure, describe:	Pass	Fail
S7	If failure, describe:	Pass	Fail
S8	If failure, describe:	Pass	Fail
S9	If failure, describe:	Pass	Fail

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This is the part of the test procedure for the RF Source Oscillator Board. Connect the oscillator board to the flat ribbon cable and the 2-pin LEMO cable, but leave it outside the metal pipe. This way one has access to the test points.

6) Verify proper current draw. Using a bench DC power supply apply ±24Volts to the chassis. One needs to wait a little while, since the OCXO will initially draw more current until it reaches its operating temperature.

+24V at < 400 mA	Measured: mA	Pass	Fail
-24V at < 100 mA	Measured: mA	Pass	Fail

7) On the oscillator board check the voltages.

TP2 (+10V)	+10V ± 5%	Measured: V	Pass	Fail
TP3 (–15V)	–15V ± 5%	Measured: V	Pass	Fail
TP4 (+15V)	+15V ± 5%	Measured: V	Pass	Fail

8) If TP2, 3 and 4 are correct then pin 9 on P1 should be logic high, ~3 Volts. This can be confirmed by making sure that the LED to the right on the rear panel is on.

Power LED on rear panel is ON	Pass	Fail

9) The noise on TP 2, 3 and 4 should be measured with a SR 785 using an rms power spectrum.

TP2 <0.2μV/√Hz @ 140Hz	Measured: μV/√Hz	Pass	Fail
TP3 <2μV/√Hz @ 140Hz	Measured: μV/√Hz	Pass	Fail
TP4 <2μV/√Hz @ 140Hz	Measured: μV/√Hz	Pass	Fail

10) The noise on TP1 should be measured with a SR 785 using an rms power spectrum. The tune inputs on J1 should be shorted together or terminated with a low impedance load.

TP1 <0.5μV/√Hz @ 140Hz	Measured: μV/√Hz	Pass	Fail

The Oscillator Board can be assembled into the magnetic shield now.

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This is the part of the test procedure for the fully assembled RF Oscillator Source.

11) Verify the proper voltages. Using bench DC power supplies apply +12V and ±24V to the chassis. If all of the voltages are correct then DS2 on the power board should light. Note the test point voltages.

TP1 (+12V)	+12V ± 10%	Measured:	V	Pass	Fail
TP5 (+24V)	+24V ± 10%	Measured:	V	Pass	Fail
TP8 (–24V)	–24V ± 10%	Measured:	V	Pass	Fail
TP3 (+18V)	+18V ± 5%	Measured:	V	Pass	Fail
TP5 (–18V)	–18V ± 5%	Measured:	V	Pass	Fail
On the 1PPS daughter board:					
TP4 (P10V)	+10V ± 5%	Measured:	V	Pass	Fail
TP5 (VCC)	+5V ± 5%	Measured:	V	Pass	Fail

For the remainder of the test the OCXO needs to be locked to the timing system. Make sure that the 2-pin LEMO cable is connected and that the push wheel switches show the exact frequency of the installed oscillator. Then, wait for the locking which is indicated by a blinking green light next to the front panel BNC.

13) **Measure the frequency range of the OCXO.** On the daughterboard TP7 indicates the control voltage of the OCXO. The RF signal form the OCXO is available at TP6. In Altium Designer open the U_JAM crosspoint switch instrument of the *FGPA_SLAVE_1PPS*. First, select the 'HI' path by connecting the output to the 'HI' input. OCXO_CONTROL[15..0] should read *65535*. Measure the voltage on TP7 and record the measured frequency. Now select the 'LO' path and repeat the above; and again for the 'MID' path. The OCXO passes the test, if its nominal frequency is within the center 50% of the range.

JAM is ON; HI is ON				
TP7 at >9V	Measured: 9.85	V	Pass	Fail
OCXO frequency	Measured: 24.079591	MHz		
JAM is ON; LO is ON				
TP7 at <1V	Measured: 0.051	V	Pass	Fail
OCXO frequency	Measured: 24.077154	MHz		
JAM is ON; MID is ON				
TP7 at 5V ±0.2V	Measured: 5.026	V	Pass	Fail
OCXO frequency	Measured: 24.079091	MHz		
Range OK			Pass	Fail

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14) Measure the control voltage of the OCXO. On the daughterboard TP7 indicates the control voltage of the OCXO. It should be close to 5V under nominal operating conditions at the nominal frequency settings. But first make sure that the push wheel switches are set to the nominal frequency of the OCXO.

Push wheel switches	Value: 24.078360 MHz		
TP7 at 5V ± 3V	Measured: 2.45 V	Pass	Fail
DS3 LED works properly (exhibits ½ Hz *blink*)		Yes	No
DS2 LED works properly (off)		Yes	No

15) Write down the value of the OCXO Control ADC and compare with the analog readback. In Altium Designer, open the U_HZ digital I/O of the *FGPA_SLAVE_1PPS* program. Compare the value of the variable OCXO_CONTROL[15..0] (shown with decimal numbers) with the Control Mon output TP7 (CTRL) on the Daughter board. The value of OCXO_CONTROL[15..0] can be converted to Volts with the following formula:

$$V\_OCXO\ [V] = OCXO\_CONTROL[15..0]\ /\ 65536.$$

If the ADC works properly, V_OCXO and TP7 should be roughly equal.

V_ OCXO	Measured: V	Pass	Fail
ADC works properly		Yes	No

16) Verify the TTL signal on the front panel BNC output. Connect a voltmeter to the front panel BNC and write down the voltages. This is a TTL signal which is high, when the OCXO is locked, and low when not. Now change the nominal frequency by 100Hz. The OCXO will lose lock which is indicated by the red LED turning on. The BNC output will go low as well. After a while lock will be reacquired and the values return to nominal.

TTL when locked	Measured: V	Pass	Fail
TTL when unlocked	Measured: V	Pass	Fail
DS3 LED works properly (steady on or off when unlocked)		Yes	No
DS2 LED works properly (on when unlocked)		Yes	No

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17) **Measure the output power of the RF Oscillator Source** with 1 PPS locking using the RF power meter. Connect the power meter to the front panel N connector and note down the RF level in dBm.

Level at 13 dBm ± 1.5 dBm	Measured: 12.0	dBm	Pass	Fail

18) **Measure the phase noise of the RF Oscillator Source** with 1 PPS locking using the Wenzel single channel phase noise measurement technique (3.5.3), Figure 3.5.2-1, which can be found at:

http://www.wenzel.com/pdffiles1/BP1000Manual/BP_1000_v101_2_.pdf .

A reasonable FFT analyzer is the SR785, which can be set to measure power units if you start in Display Setup. A Reference Source must be provided which can be just a Wenzel crystal oscillator of frequency close enough to lock, properly powered and connected to the Wenzel phase noise measurement system. Make measurements with a span of 100 kHz, 12.5 kHz, 1.6 kHz and 200 Hz and with 800 FFT lines. Save the traces as ASCII files and stitch them together into a single file covering both the low and high frequency range as a continuous function. Plot the noise spectrum with the proper calibration factor, so that the units on the y-axis are dBc/Hz. A test is considered passed, if the measured noise level is no more than 10dB worse than the Wenzel specification for the oscillator. Save the plot as a PDF file and the data as an ASCII file. Use the filename 'serial #'-noise.pdf and .txt.

~ −100dBc/Hz @ 10Hz	Measured: ~ −118	dBc/Hz	Pass	Fail
~ −130dBc/Hz @ 100Hz	Measured: ~ −133	dBc/Hz	Pass	Fail
~ −155dBc/Hz @ 1kHz	Measured: ~ −146	dBc/Hz	Pass	Fail
~ −165dBc/Hz @ 10kHz	Measured: ~ −162	dBc/Hz	Pass	Fail

Step 1: Slope $= \frac{68\,mV}{0.02\pi\,rad} = 1.0823\ V/rad$

200 Hz → 21
1.6k Hz → 22
12.5k Hz → 23
100k Hz → 24

f (Hz)	PSO (dBV(rms)/$\sqrt{Hz}$)	L_{corr} (dBc/Hz)
10	−55	−118
100	−70	−133
1K	−83	−146
10K	−99	−162