**LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY**

**-LIGO-**

**CALIFORNIA INSTITUTE OF TECHNOLOGY**

**MASSACHUSETTS INSTITUTE OF TECHNOLOGY**

|  |  |  |
| --- | --- | --- |
| Document Type  Test Procedure | DCC Number  **T1400045**-v5 | March 14, 2014 |
| **TCS ISS and Interface Box Test Procedure** | | |
| B. Abbott | | |

Distribution of this draft:

This is an internal working note of the LIGO Laboratory

**California Institute of Technology Massachusetts Institute of Technology**

**LIGO Project – MS 18-33 LIGO Project – MS 20B-145**

**Pasadena, CA 91125 Cambridge, MA 01239**

Phone (626) 395-2129 Phone (617) 253-4824

Fax (626) 304-9834 Fax (617) 253-7014

E-mail: info@ligo.caltech.edu E-mail: info@ligo.mit.edu

<http://www.ligo.caltech.edu/>

Performed by:\_\_\_\_\_\_\_\_\_\_\_\_

Date:\_\_\_\_\_\_\_\_\_\_\_\_\_

Board Serial Number: \_\_\_\_\_\_\_\_\_\_\_\_\_

1. **Overview**

The Thermal Compensation System (TCS) Intensity Stabilization Servo (ISS) and Interface Box serves many functions. The ISS board (D1300015) stabilizes the intensity of the TCS CO2 laser by modulating an AOM, while also bringing in the two Photodiode signals (inside and outside the loop). The Interface board (D1300650) Collects, and signal conditions signals from 2 Thermal Quadrant PDs, a Thermal Power Sensor, and a Laser Thermopile. It also gets a drive signal from the DAC, and drives (and monitors) the signal to the Laser PZT. This document will describe how to test each box, to ensure proper functionality.

1. **Test Equipment**

**2.1** Power Supply capable of +/- 18V

**2.2** Power Supply capable of +100V

**2.3** Digital Multimeter (DMM)

**2.4** SR785 network analyzer, or equivalent

**2.5** Voltage Calibrator, or adjustable power supply

**2.6** Signal Generator

**2.7** Oscilloscope

1. **Preliminaries**

**3.1** Perform visual inspection on board to check for missing components or solder deficiencies

**3.2** Before connecting the power to the chassis, set power supplies to +/- 18 Volts and 100V, respectively, then turn them off. Connect the power supplies to the chassis under test at the back panel 3-pin power connector labeled “Power Input” and the BNC labeled “100V In” paying attention to the values and polarities on the panel.

1. **DC Tests**
   1. Turn on the +/- 18V power supplies to the system under test and then turn on the Chassis Power switch. Record the total current.

|  |  |  |  |
| --- | --- | --- | --- |
| **Measure** | **Expected Current** | **Observed Current** | **FP Leds On?** |
| +18V Supply | 270mA +/- 20mA |  |  |
| -18V Supply | 270mA +/- 20mA |  |  |

* 1. Using a digital multimeter to verify that +/- 8.5V is outputted to the “Power to TTL” Output connector.

|  |  |  |
| --- | --- | --- |
| **OUTPUT** | **Expect**  **Value** | **Voltage**  **Correct?** |
| “Power to TTL”  (J3-1 (+) / J3-6 (GND)) | +8.5V +/- .2V |  |
| “Power to TTL”  (J3-2 (-) / J3-7 (GND)) | -8.5V+/- .2V |  |

1. **Dynamic Tests**
   1. **ISI Interface Tests :**

# PD Channels: Set the network analyzer source to 1mV p-p with respect to GND, swept from 1Hz to 10KHz, and input at the appropriate QPD input connector, as dictated below. The output should be read differentially (A-B) at the back panel connector “To Anti-Alias Chassis” (J5)

|  |  |  |  |
| --- | --- | --- | --- |
| **Input 1mV P-P** | **Expected Output = 80dB** +/-1dB **@DC with a pole at 10.6Hz** +/-2Hz | **Observed Gain @ 1Hz (dB)** | **Observed 3dB Pole Frequency (Hz)** |
| **“From QPD-A” pins 1(+) and 3(GND)** | **“To Anti-Alias Chassis”**  **Pins 1(+) and 20 (-)** |  |  |
| **“From QPD-A” pins 14(+) and 3(GND)** | **“To Anti-Alias Chassis”**  **Pins 2(+) and 21 (-)** |  |  |
| **“From QPD-A” pins 2(+) and 3(GND)** | **“To Anti-Alias Chassis”**  **Pins 3(+) and 22 (-)** |  |  |
| **“From QPD-A” pins 15(+) and 3(GND)** | **“To Anti-Alias Chassis”**  **Pins 4(+) and 23 (-)** |  |  |
| **“From QPD-B” pins 1(+) and 3(GND)** | **“To Anti-Alias Chassis”**  **Pins 5(+) and 24 (-)** |  |  |
| **“From QPD-B” pins 14(+) and 3(GND)** | **“To Anti-Alias Chassis”**  **Pins 6(+) and 25 (-)** |  |  |
| **“From QPD-B” pins 2(+) and 3(GND)** | **“To Anti-Alias Chassis”**  **Pins 7(+) and 26 (-)** |  |  |
| **“From QPD-B” pins 15(+) and 3(GND)** | **“To Anti-Alias Chassis”**  **Pins 8(+) and 27 (-)** |  |  |

# Thermal Sensor Tests: The source should be set to the stated amplitude with respect to GND, and swept from 1Hz to 100KHz at the input of the appropriate connector, as dictated below. The output should be read differentially (A-B) at the back panel connector “To Anti-Alias Chassis” (J5)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Input 10mV P-P**  **“From Thermal Power Sensor”** | **Expected Output = 60dB +/-1dB @DC with a pole at 10.6Hz +/-2Hz, zero at about 4.8KHz, and 100KHz gain of 6dB** | **Observed Gain @ 1Hz** | **Observed 3dB Pole Frequency** | **Gain@ 100KHz** |
| **Pin8 (+) and Pin3 (GND)** | **“To Anti-Alias Chassis”**  **Pins 9 (+) and 28 (-)** |  |  |  |
| **Input 100mV P-P** | **Expected Output = a Flat 40dB +/-1dB to 55KHz** | **Observed Gain@ 1Hz** | **Observed Gain@ 55KHz** | **(Starts to droop after 55KHz)** |
| **“From Thermopile” SMA** | **“To Anti-Alias Chassis”**  **Pins 10 (+) and 29 (-)** |  |  |  |

* 1. **Intensity Servo Tests**

**5.2.1 Unconditioned or buffered Photodiode Signals:** The raw signals coming from the PD Heads are not amplified or filtered in the ISS chassis. To make sure that we have continuity for the three untouched, and one buffered (Inner DC) signals, run a quick transfer function from 100Hz to 100KHz, with a source level of **1V**. Compare the results with the expected, below.

|  |  |  |
| --- | --- | --- |
| **INPUT**  **PD Connector** | **Expected Output= a Flat 0dB +/-0.1dB** | **Observed Output** |
| **“From In-Loop PD”**  **Pin1(+) and Pin6(-)** | **“To Anti-Alias Chassis”**  **Pins 11 (+) and 30 (-)** |  |
| **“From In-Loop PD”**  **Pin2(+) and Pin7(-)** | **“To Anti-Alias Chassis”**  **Pins 12 (+) and 31 (-)** |  |
| **“From Out-of-Loop PD”**  **Pin1(+) and Pin6(-)** | **“To Anti-Alias Chassis”**  **Pins 13 (+) and 32 (-)** |  |
| **“From Out-of -Loop PD”**  **Pin2(+) and Pin7(-)** | **“To Anti-Alias Chassis”**  **Pins 14 (+) and 33 (-)** |  |

**5.2.2 Loop Switch and DC Summing Tests:**

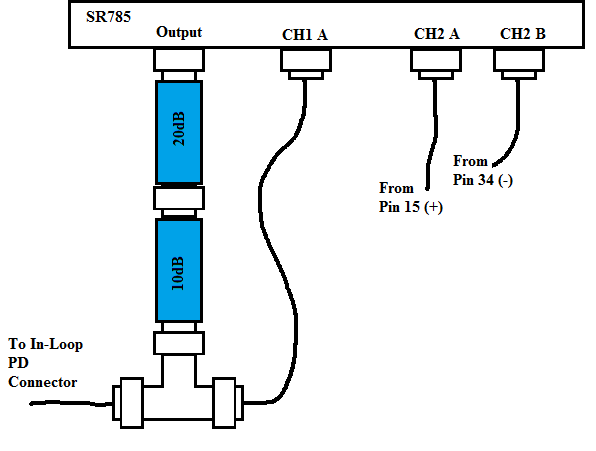
Input a 20Hz 10mVp-p sine wave into Pins 2(+) and 7(-) on the “From In-Loop PD” connector, and read out on an oscilloscope on the “Out to AOM” front panel BNC connector. To read this signal out correctly, it needs to be terminated in 50Ohms. The easy way to do this is to put a BNC “Tee” on the “Out to AOM” connector, then put a 50 Ohm terminator on one side of the Tee, and connect your oscilloscope to the other side. At first, you should see nothing coming out. Then put 15V (Easily found on TP1 of the Back Power Board) onto the “From AI Chassis” connector on pin 3(+) and GND From TP9 or TP10. This should throw the Loop Switch relay, and you should now see a half-wave rectified signal. At the same time, the “Loop closed” LED should light, and the Loop Switch Readback should go to 15V as seen on the “To Anti-Alias” connector, Pin17 (+) and Pin36 (GND). Then, using a voltage calibrator, or equivalent, put a biasing DC voltage on the “From AI Chassis” connector to get the full sine wave signal.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **INPUT**  **PD Connector** | **Voltage on**  **AI connector,**  **Pin 3 to GND** | **Voltage on**  **AI pins**  **1(+) & 6 (-)** | **Expected**  **Output** | **Observed Output**  **Correct?** |
| **“From In-Loop PD”**  **Pin2(+) and Pin7(-)**  **20Hz, 10mVp-p** | **0V** | **0V** | **0V p-p** |  |
| **“From In-Loop PD”**  **Pin2(+) and Pin7(-)**  **20Hz, 10mVp-p** | **15V** | **0V** | **0-680mV Half-wave rectified Sine (+/-20mV)** |  |
| **“From Out-of-Loop PD”**  **Pin2(+) and Pin7(-)**  **20Hz, 10mVp-p** | **15V** | **7V** | **0V-1.38 V Sine Wave (+/- 20mV)** |  |

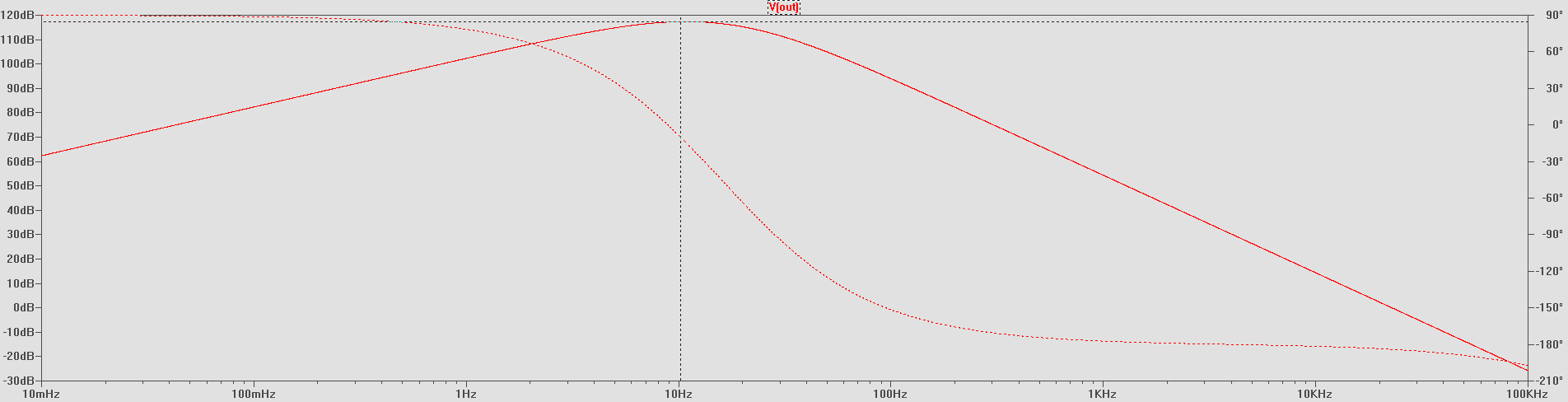
**5.2.3 Servo Shape, and Whitening Tests**

With the voltage to throw the Loop Switch relay still present (From AI Chassis, Pin 3), check the transfer functions of the three available outputs of the ISS Servo by putting a **0.5mV** 1Hz-10KHz signal through 30dB of attenuation (see diagram, below) into the “In-Loop PD” connector, pins 2(+) and 7(-), and read the outputs at the “Expected output” pins dictated in the three following tables. Following each table is the predicted response of the signal paths. Enter any gain information into the table, and indicate if the output waveform looks like the predicted waveform.

**SR785 Setup: (Be sure to tie both black leads of**

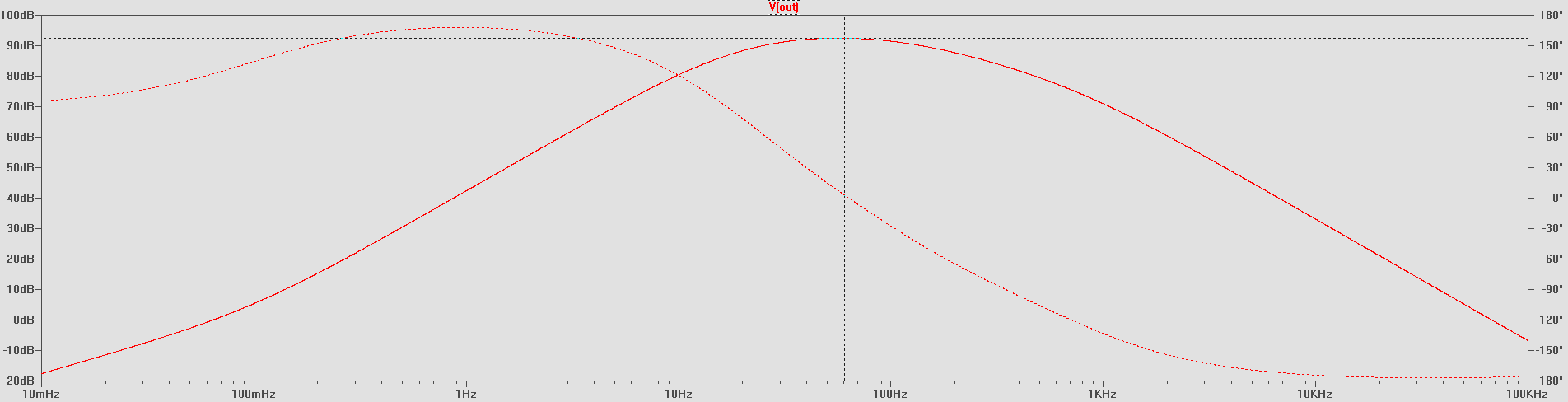
 **The test leads to GND on the Board)**

|  |  |  |  |
| --- | --- | --- | --- |
| **Input**  **0.5mV, 1Hz – 10KHz** | **Expected Output**  **(Whiten 1)** | **Gain @ 10Hz?** | **Observed Output**  **Correct?** |
| **“From In-Loop PD”**  **Pin2(+) and Pin7(-)** | **“To Anti-Alias Chassis”**  **Pins 15 (+) and 34 (-)**  **Zero @ DC, 2 Poles @ 20Hz, and a Pole @ 1KHz. Gain @ 10Hz = 117.4dB +/- 1dB.** |  |  |

**Calculated Plot:**

**Remove the attenuators, for the rest of the measurements:**

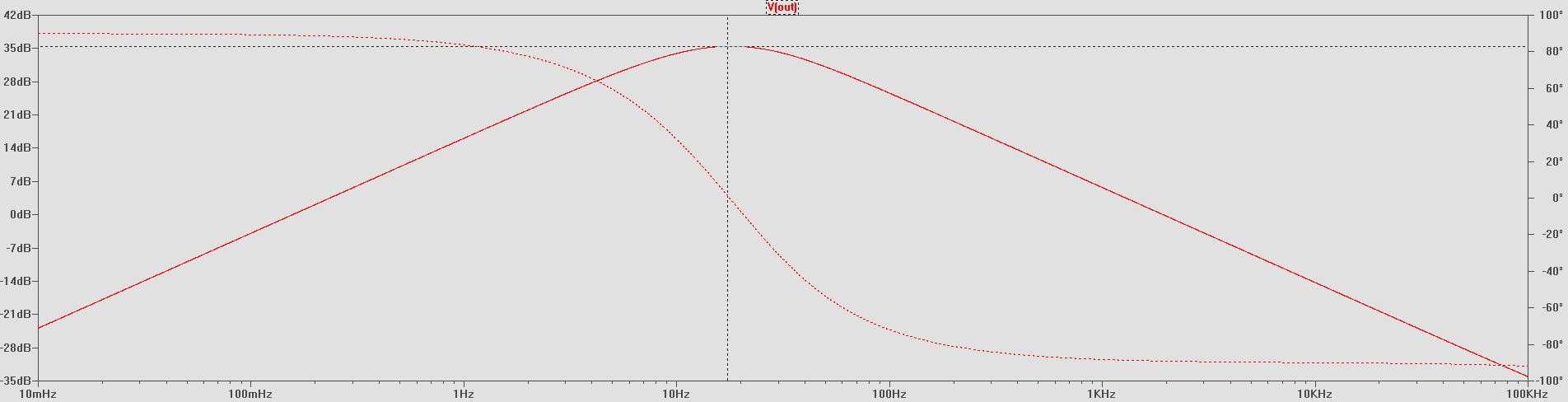
|  |  |  |  |
| --- | --- | --- | --- |
| **Input (no attenuators)**  **0.5mV, 1Hz – 10KHz** | **Expected Output**  **(Whiten 2)** | **Gain @ 60Hz?** | **Observed Output**  **Correct?** |
| **“From In-Loop PD”**  **Pin2(+) and Pin7(-)**  **Plus +7V on “To AI Chassis” connector, pins 1(+) and 6 (-)** | **“To Anti-Alias Chassis”**  **Pins 16 (+) and 35 (-)**  **2 Zeroes @ DC, 2 Poles @ 20Hz, 1 pole at 106Hz and 800 Hz.**  **Gain @ 60Hz = 92.5dB +/- 1dB.** |  |  |



**Calculated Plot:**

**Change Chan2 input from A-B to A, Make sure the analyzer is AC coupled, and put 7V into “From AI Chassis” pins 1& 6, and keep the 50Ohm terminator on, like in 5.2.2, above.**

|  |  |  |  |
| --- | --- | --- | --- |
| **Input (no attenuators)**  **10mV, 1Hz – 10KHz** | **Expected Output**  **(Out to AOM)** | **Gain @ 20Hz?** | **Observed Output**  **Correct?** |
| **“From In-Loop PD”**  **Pin2(+) and Pin7(-)** | **“OUT to AOM” Front Panel BNC**  **Zero @ DC, 2 Poles @ 20Hz.**  **Gain @ 20Hz = 36.5dB +/- 1dB.** |  |  |

**Calculated Plot:**

# PZT High Voltage Power Supply: (Warning, High Voltage!!) For sections 5.1.3, 5.1.4, and 5.1.5, you will be dealing with high Voltage (100V). Take appropriate precautions to protect yourself from shock. Make sure that the chassis cover is securely attached, so nothing can touch the internal high voltage circuitry. Be mindful of exposed connectors and pins. Connect, then turn on the 100V power supply, and record its current and indicator LED below.

|  |  |  |  |
| --- | --- | --- | --- |
| **Measure** | **Expected Current** | **Observed Current** | **100V LED Lit?** |
| +100V Supply | 15mA +/- 5mA |  |  |

# PZT Drive Monitor Tests: With the High Voltage supply still on, the source should be set to 100mV p-p, swept from 1Hz to 10KHz, and input at the appropriate input connector, as dictated below. The monitor output should be read differentially (A-B) at the back panel connector “To Anti-Alias Chassis” (J5)

|  |  |  |  |
| --- | --- | --- | --- |
| **Input 10mV P-P**  **“From AI Chassis”** | **Expected Output = DC Gain=0dB +/-0.5dB with a Pole at 33Hz +/- 5Hz** | **Observed Gain @ 1Hz** | **Pole Frequency** |
| **Pin2 (+) and Pin7 (GND)** | **“To Anti-Alias Chassis”**  **Pins 18 (+) and 37 (-)** |  |  |

# High Voltage PZT Drive Test: Use a Voltage Calibrator or adjustable Power Supply, put 1V, 5V, and 10V across Pins 2 and 7 of the “From AI Chassis” connector, and read the output on the “To PZT” SMA connector with a handheld DMM rated for more than 100V.

|  |  |  |
| --- | --- | --- |
| **Input**  **“From AI Chassis”** | **Expected Output**  **“To PZT” SMA** | **Observed Output** |
| **Pin2 (+) and Pin7 (GND) 1V** | **10V +/- 0.2V** |  |
| **Pin2 (+) and Pin7 (GND) 5V** | **50V +/- 1.0V** |  |
| **Pin2 (+) and Pin7 (GND) 10V** | **100V +/- 2V** |  |

**Turn Off the 100V power supply, and disconnect it.**

* + 1. Servo Noise Test:With Chan2 input from still set to A, and 15V into “From AI Chassis” pin 3, ground all of the inputs to the servo loop: “From In-Loop PD”, pins 2&7, and “From AI Chassis” pins 1&6. Measure the noise coming out of the “To AOM” BNC Connector with a span from 1 Hz to 801Hz, allowing 50 averages. Record the noise levels, and chassis test results in the table below.

|  |  |  |  |
| --- | --- | --- | --- |
| **Measurement** | **Expected Output** | **Observed Output** | **Pass? (Yes/No)** |
| **Noise level at 10Hz** | **<525 nV/** |  |  |
| **Noise level at 20Hz** | **<525 nV/** |  |  |
| **Peak noise from 5Hz to 801Hz (Excluding 60 Hz and harmonics)** | **<575 nV/** |  |  |