PSoC® Creator™
Project Datasheet for Pulser

Creation Time: 02/25/2015 17:16:04
User: C22093\abbott
Project: Pulser
Tool: PSoC Creator 3.1 Component Pack 1

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1 Overview

The Cypress PSoC 3 is a family of 8-bit devices with the following characteristics:

- An 8-bit single cycle pipelined 8051 processor, running up to 67 MHz, with a nested vectored interrupt controller (NVIC) and a high-performance DMA controller. The single cycle 8051 CPU runs ten times faster than a standard 8051 processor.
- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals, such as USB, CAN and I2C
- Analog subsystem that includes configurable switched (SC) and continuous time (CT) blocks, up to 20-bit Delta Sigma converters (ADC), SAR ADCs, 8-bit DACs that can be configured for 12-bit operation, op amps, comparators, PGAs, and more
- Several types of memory elements, including SRAM, flash, and EEPROM
- Programming and debug system through JTAG, serial wire debug (SWD), and single wire viewer (SWV)
- Flexible routing to all pins

Figure 1 shows the major components of a typical CY8C38 family member PSoC 3 device. For details on all the systems listed above, please refer to the PSoC 3 Technical Reference Manual .

Figure 1. CY8C38 Device Family Block Diagram

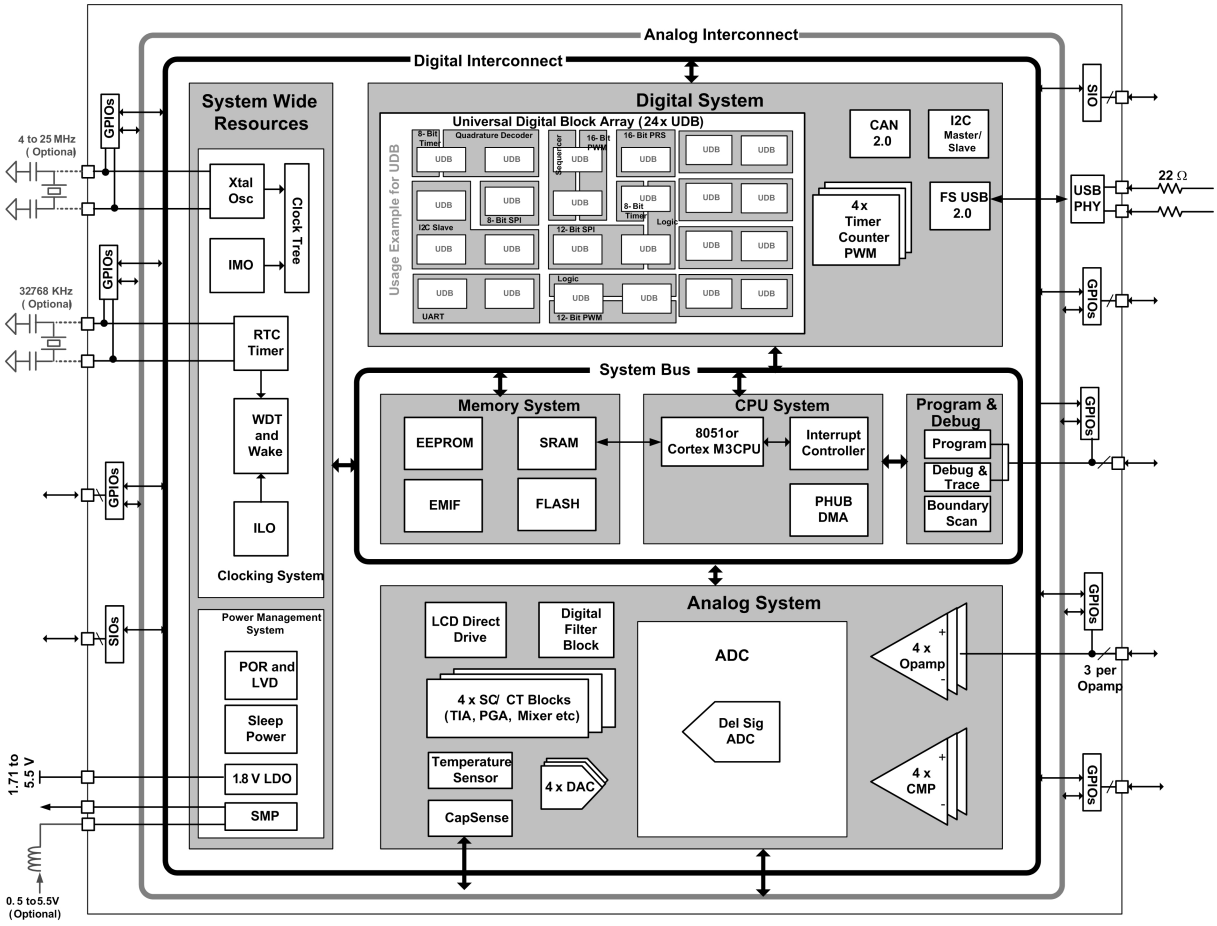


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CY8C3866AXI-040
Package Name	100-TQFP
Architecture	PSoC 3
Family	CY8C38
CPU speed (MHz)	67
Flash size (kBytes)	64
SRAM size (kBytes)	8
EEPROM size (Bytes)	2048
Trace Buffer (kBytes)	4
Vdd range (V)	1.7 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celcius)	-40 to 85
JTAG ID	0x1E028069

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by Bus Clock, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

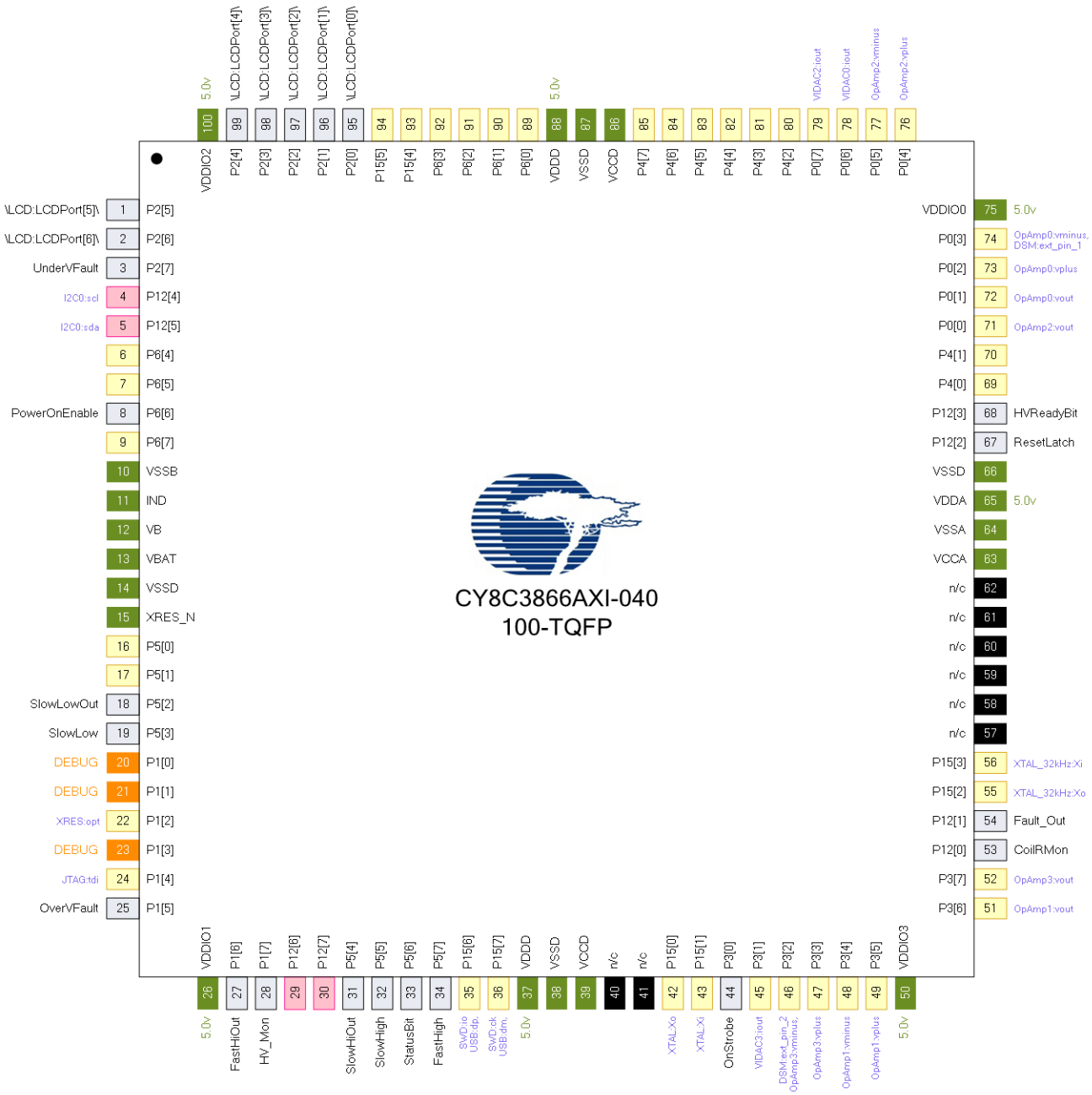
Table 2. Device Resources

Name	In Use	Free	Total Resources Available	% in Use
Digital clock dividers	2	6	8	25.0%
Analog clock dividers	1	3	4	25.0%
Pins	26	46	72	36.1%
UDB Macrocells	86	106	192	44.8%
UDB Unique Pterms	159	225	384	41.4%
UDB Datapath Cells	2	22	24	8.3%
UDB Status Cells	3	21	24	12.5%
UDB Control Cells	2	22	24	8.3%
DMA Channels	0	24	24	0.0%
Interrupts	1	31	32	3.1%
DSM Fixed Blocks	1	0	1	100.0%
VIDAC Fixed Blocks	1	3	4	25.0%
SC Fixed Blocks	0	4	4	0.0%
Comparator Fixed Blocks	1	3	4	25.0%
Opamp Fixed Blocks	0	4	4	0.0%
CapSense Buffers	0	2	2	0.0%
CAN Fixed Blocks	0	1	1	0.0%
Decimator Fixed Blocks	1	0	1	100.0%
I2C Fixed Blocks	0	1	1	0.0%
Timer Fixed Blocks	0	4	4	0.0%
DFB Fixed Blocks	0	1	1	0.0%
USB Fixed Blocks	0	1	1	0.0%
LCD Fixed Blocks	0	1	1	0.0%
EMIF Fixed Blocks	0	1	1	0.0%
LPF Fixed Blocks	0	2	2	0.0%

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode	Reset State
1	P2[5]	\LCD:LCDPort[5]\	Software Output	Strong drive	HiZ Analog Unb
2	P2[6]	\LCD:LCDPort[6]\	Software Output	Strong drive	HiZ Analog Unb
3	P2[7]	UnderVFault	Dgtl In	Res pull up	HiZ Analog Unb
4	P12[4]	SIO [unused]			HiZ Analog Unb
5	P12[5]	SIO [unused]			HiZ Analog Unb
6	P6[4]	GPIO [unused]			HiZ Analog Unb
7	P6[5]	GPIO [unused]			HiZ Analog Unb
8	P6[6]	PowerOnEnable	Dgtl In	Res pull down	HiZ Analog Unb
9	P6[7]	GPIO [unused]			HiZ Analog Unb
10	VSSB	VSSB	Dedicated		
11	IND	IND	Dedicated		
12	VB	VB	Dedicated		
13	VBAT	VBAT	Dedicated		
14	VSSD	VSSD	Power		
15	XRES_N	XRES_N	Dedicated		
16	P5[0]	GPIO [unused]			HiZ Analog Unb
17	P5[1]	GPIO [unused]			HiZ Analog Unb
18	P5[2]	SlowLowOut	Dgtl Out	Strong drive	HiZ Analog Unb
19	P5[3]	SlowLow	Dgtl In	Res pull up	HiZ Analog Unb
20	P1[0]	Debug:SWD_IO	Reserved		
21	P1[1]	Debug:SWD_CK	Reserved		
22	P1[2]	GPIO [unused]			HiZ Analog Unb
23	P1[3]	Debug:SWV	Reserved		
24	P1[4]	GPIO [unused]			HiZ Analog Unb
25	P1[5]	OverVFault	Dgtl In	Res pull up	HiZ Analog Unb
26	VDDIO1	VDDIO1	Power		
27	P1[6]	FastHiOut	Dgtl Out	Strong drive	HiZ Analog Unb
28	P1[7]	HV_Mon	Analog	HiZ analog	HiZ Analog Unb
29	P12[6]	SIO [unused]			HiZ Analog Unb
30	P12[7]	SIO [unused]			HiZ Analog Unb
31	P5[4]	SlowHiOut	Dgtl Out	Strong drive	HiZ Analog Unb
32	P5[5]	SlowHigh	Dgtl In	Res pull up	HiZ Analog Unb
33	P5[6]	StatusBit	Dgtl Out	Strong drive	HiZ Analog Unb
34	P5[7]	FastHigh	Dgtl In	Res pull up	HiZ Analog Unb
35	P15[6]	USB IO [unused]			HiZ Analog Unb
36	P15[7]	USB IO [unused]			HiZ Analog Unb
37	VDDD	VDDD	Power		
38	VSSD	VSSD	Power		
39	VCCD	VCCD	Power		
42	P15[0]	GPIO [unused]			HiZ Analog Unb
43	P15[1]	GPIO [unused]			HiZ Analog Unb
44	P3[0]	OnStrobe	Dgtl In	HiZ digital	HiZ Analog Unb
45	P3[1]	GPIO [unused]			HiZ Analog Unb

Pin	Port	Name	Type	Drive Mode	Reset State
46	P3[2]	GPIO [unused]			HiZ Analog Unb
47	P3[3]	GPIO [unused]			HiZ Analog Unb
48	P3[4]	GPIO [unused]			HiZ Analog Unb
49	P3[5]	GPIO [unused]			HiZ Analog Unb
50	VDDIO3	VDDIO3	Power		
51	P3[6]	GPIO [unused]			HiZ Analog Unb
52	P3[7]	GPIO [unused]			HiZ Analog Unb
53	P12[0]	CoilRMon	Dgtl In	HiZ digital	HiZ Analog Unb
54	P12[1]	Fault_Out	Dgtl Out	Strong drive	HiZ Analog Unb
55	P15[2]	GPIO [unused]			HiZ Analog Unb
56	P15[3]	GPIO [unused]			HiZ Analog Unb
63	VCCA	VCCA	Power		
64	VSSA	VSSA	Power		
65	VDDA	VDDA	Power		
66	VSSD	VSSD	Power		
67	P12[2]	ResetLatch	Dgtl Out	Strong drive	HiZ Analog Unb
68	P12[3]	HVReadyBit	Dgtl Out	Strong drive	HiZ Analog Unb
69	P4[0]	GPIO [unused]			HiZ Analog Unb
70	P4[1]	GPIO [unused]			HiZ Analog Unb
71	P0[0]	GPIO [unused]			HiZ Analog Unb
72	P0[1]	GPIO [unused]			HiZ Analog Unb
73	P0[2]	GPIO [unused]			HiZ Analog Unb
74	P0[3]	GPIO [unused]			HiZ Analog Unb
75	VDDIO0	VDDIO0	Power		
76	P0[4]	GPIO [unused]			HiZ Analog Unb
77	P0[5]	GPIO [unused]			HiZ Analog Unb
78	P0[6]	GPIO [unused]			HiZ Analog Unb
79	P0[7]	GPIO [unused]			HiZ Analog Unb
80	P4[2]	GPIO [unused]			HiZ Analog Unb
81	P4[3]	GPIO [unused]			HiZ Analog Unb
82	P4[4]	GPIO [unused]			HiZ Analog Unb
83	P4[5]	GPIO [unused]			HiZ Analog Unb
84	P4[6]	GPIO [unused]			HiZ Analog Unb
85	P4[7]	GPIO [unused]			HiZ Analog Unb
86	VCCD	VCCD	Power		
87	VSSD	VSSD	Power		
88	VDDD	VDDD	Power		
89	P6[0]	GPIO [unused]			HiZ Analog Unb
90	P6[1]	GPIO [unused]			HiZ Analog Unb
91	P6[2]	GPIO [unused]			HiZ Analog Unb
92	P6[3]	GPIO [unused]			HiZ Analog Unb
93	P15[4]	GPIO [unused]			HiZ Analog Unb
94	P15[5]	GPIO [unused]			HiZ Analog Unb
95	P2[0]	\LCD:LCDPort[0]\	Software Output	Strong drive	HiZ Analog Unb
96	P2[1]	\LCD:LCDPort[1]\	Software Output	Strong drive	HiZ Analog Unb
97	P2[2]	\LCD:LCDPort[2]\	Software Output	Strong drive	HiZ Analog Unb
98	P2[3]	\LCD:LCDPort[3]\	Software Output	Strong drive	HiZ Analog Unb
99	P2[4]	\LCD:LCDPort[4]\	Software Output	Strong drive	HiZ Analog Unb
100	VDDIO2	VDDIO2	Power		

Abbreviations used in Table 3 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl In = Digital Input
- Res pull up = Resistive pull up
- Res pull down = Resistive pull down
- Dgtl Out = Digital Output
- HiZ analog = High impedance analog
- HiZ digital = High impedance digital

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode	Reset State
P0[0]	71	GPIO [unused]			HiZ Analog Unb
P0[1]	72	GPIO [unused]			HiZ Analog Unb
P0[2]	73	GPIO [unused]			HiZ Analog Unb
P0[3]	74	GPIO [unused]			HiZ Analog Unb
P0[4]	76	GPIO [unused]			HiZ Analog Unb
P0[5]	77	GPIO [unused]			HiZ Analog Unb
P0[6]	78	GPIO [unused]			HiZ Analog Unb
P0[7]	79	GPIO [unused]			HiZ Analog Unb
P1[0]	20	Debug:SWD_IO	Reserved		
P1[1]	21	Debug:SWD_CK	Reserved		
P1[2]	22	GPIO [unused]			HiZ Analog Unb
P1[3]	23	Debug:SWV	Reserved		
P1[4]	24	GPIO [unused]			HiZ Analog Unb
P1[5]	25	OverVFault	Dgtl In	Res pull up	HiZ Analog Unb
P1[6]	27	FastHiOut	Dgtl Out	Strong drive	HiZ Analog Unb
P1[7]	28	HV_Mon	Analog	HiZ analog	HiZ Analog Unb
P12[0]	53	CoilRMon	Dgtl In	HiZ digital	HiZ Analog Unb
P12[1]	54	Fault_Out	Dgtl Out	Strong drive	HiZ Analog Unb
P12[2]	67	ResetLatch	Dgtl Out	Strong drive	HiZ Analog Unb
P12[3]	68	HVReadyBit	Dgtl Out	Strong drive	HiZ Analog Unb
P12[4]	4	SIO [unused]			HiZ Analog Unb
P12[5]	5	SIO [unused]			HiZ Analog Unb
P12[6]	29	SIO [unused]			HiZ Analog Unb
P12[7]	30	SIO [unused]			HiZ Analog Unb
P15[0]	42	GPIO [unused]			HiZ Analog Unb
P15[1]	43	GPIO [unused]			HiZ Analog Unb
P15[2]	55	GPIO [unused]			HiZ Analog Unb
P15[3]	56	GPIO [unused]			HiZ Analog Unb
P15[4]	93	GPIO [unused]			HiZ Analog Unb
P15[5]	94	GPIO [unused]			HiZ Analog Unb
P15[6]	35	USB IO [unused]			HiZ Analog Unb
P15[7]	36	USB IO [unused]			HiZ Analog Unb
P2[0]	95	\LCD:LCDPort[0]\	Software Output	Strong drive	HiZ Analog Unb
P2[1]	96	\LCD:LCDPort[1]\	Software Output	Strong drive	HiZ Analog Unb
P2[2]	97	\LCD:LCDPort[2]\	Software Output	Strong drive	HiZ Analog Unb
P2[3]	98	\LCD:LCDPort[3]\	Software Output	Strong drive	HiZ Analog Unb
P2[4]	99	\LCD:LCDPort[4]\	Software Output	Strong drive	HiZ Analog Unb
P2[5]	1	\LCD:LCDPort[5]\	Software Output	Strong drive	HiZ Analog Unb
P2[6]	2	\LCD:LCDPort[6]\	Software Output	Strong drive	HiZ Analog Unb

Port	Pin	Name	Type	Drive Mode	Reset State
P2[7]	3	UnderVFault	Dgtl In	Res pull up	HiZ Analog Unb
P3[0]	44	OnStrobe	Dgtl In	HiZ digital	HiZ Analog Unb
P3[1]	45	GPIO [unused]			HiZ Analog Unb
P3[2]	46	GPIO [unused]			HiZ Analog Unb
P3[3]	47	GPIO [unused]			HiZ Analog Unb
P3[4]	48	GPIO [unused]			HiZ Analog Unb
P3[5]	49	GPIO [unused]			HiZ Analog Unb
P3[6]	51	GPIO [unused]			HiZ Analog Unb
P3[7]	52	GPIO [unused]			HiZ Analog Unb
P4[0]	69	GPIO [unused]			HiZ Analog Unb
P4[1]	70	GPIO [unused]			HiZ Analog Unb
P4[2]	80	GPIO [unused]			HiZ Analog Unb
P4[3]	81	GPIO [unused]			HiZ Analog Unb
P4[4]	82	GPIO [unused]			HiZ Analog Unb
P4[5]	83	GPIO [unused]			HiZ Analog Unb
P4[6]	84	GPIO [unused]			HiZ Analog Unb
P4[7]	85	GPIO [unused]			HiZ Analog Unb
P5[0]	16	GPIO [unused]			HiZ Analog Unb
P5[1]	17	GPIO [unused]			HiZ Analog Unb
P5[2]	18	SlowLowOut	Dgtl Out	Strong drive	HiZ Analog Unb
P5[3]	19	SlowLow	Dgtl In	Res pull up	HiZ Analog Unb
P5[4]	31	SlowHiOut	Dgtl Out	Strong drive	HiZ Analog Unb
P5[5]	32	SlowHigh	Dgtl In	Res pull up	HiZ Analog Unb
P5[6]	33	StatusBit	Dgtl Out	Strong drive	HiZ Analog Unb
P5[7]	34	FastHigh	Dgtl In	Res pull up	HiZ Analog Unb
P6[0]	89	GPIO [unused]			HiZ Analog Unb
P6[1]	90	GPIO [unused]			HiZ Analog Unb
P6[2]	91	GPIO [unused]			HiZ Analog Unb
P6[3]	92	GPIO [unused]			HiZ Analog Unb
P6[4]	6	GPIO [unused]			HiZ Analog Unb
P6[5]	7	GPIO [unused]			HiZ Analog Unb
P6[6]	8	PowerOnEnable	Dgtl In	Res pull down	HiZ Analog Unb
P6[7]	9	GPIO [unused]			HiZ Analog Unb

Abbreviations used in Table 4 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl In = Digital Input
- Res pull up = Resistive pull up
- Dgtl Out = Digital Output
- HiZ analog = High impedance analog
- HiZ digital = High impedance digital
- Res pull down = Resistive pull down

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type	Reset State
\LCD:LCDPort[0]\	P2[0]	Software Output	HiZ Analog Unb
\LCD:LCDPort[1]\	P2[1]	Software Output	HiZ Analog Unb
\LCD:LCDPort[2]\	P2[2]	Software Output	HiZ Analog Unb
\LCD:LCDPort[3]\	P2[3]	Software Output	HiZ Analog Unb
\LCD:LCDPort[4]\	P2[4]	Software Output	HiZ Analog Unb
\LCD:LCDPort[5]\	P2[5]	Software Output	HiZ Analog Unb
\LCD:LCDPort[6]\	P2[6]	Software Output	HiZ Analog Unb
CoilRMon	P12[0]	Dgtl In	HiZ Analog Unb
Debug:SWD_CK	P1[1]	Reserved	
Debug:SWD_IO	P1[0]	Reserved	
Debug:SWV	P1[3]	Reserved	
FastHigh	P5[7]	Dgtl In	HiZ Analog Unb
FastHiOut	P1[6]	Dgtl Out	HiZ Analog Unb
Fault_Out	P12[1]	Dgtl Out	HiZ Analog Unb
HV_Mon	P1[7]	Analog	HiZ Analog Unb
HVReadyBit	P12[3]	Dgtl Out	HiZ Analog Unb
OnStrobe	P3[0]	Dgtl In	HiZ Analog Unb
OverVFault	P1[5]	Dgtl In	HiZ Analog Unb
PowerOnEnable	P6[6]	Dgtl In	HiZ Analog Unb
ResetLatch	P12[2]	Dgtl Out	HiZ Analog Unb
SlowHigh	P5[5]	Dgtl In	HiZ Analog Unb
SlowHiOut	P5[4]	Dgtl Out	HiZ Analog Unb
SlowLow	P5[3]	Dgtl In	HiZ Analog Unb
SlowLowOut	P5[2]	Dgtl Out	HiZ Analog Unb
StatusBit	P5[6]	Dgtl Out	HiZ Analog Unb
UnderVFault	P2[7]	Dgtl In	HiZ Analog Unb

Abbreviations used in Table 5 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl In = Digital Input
- Dgtl Out = Digital Output

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Enable Error Correcting Code (ECC)	False
Store Configuration Data in ECC Memory	True
Instruction Cache Enabled	True
Enable Fast IMO During Startup	True
Clear SRAM During Startup	True
Unused Bonded IO	Allow but warn

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	SWD+SWV (serial wire debug and viewer)
Enable Device Protection	False
Use Optional XRES	False

3.3 System Operating Conditions

Table 8. System Operating Conditions

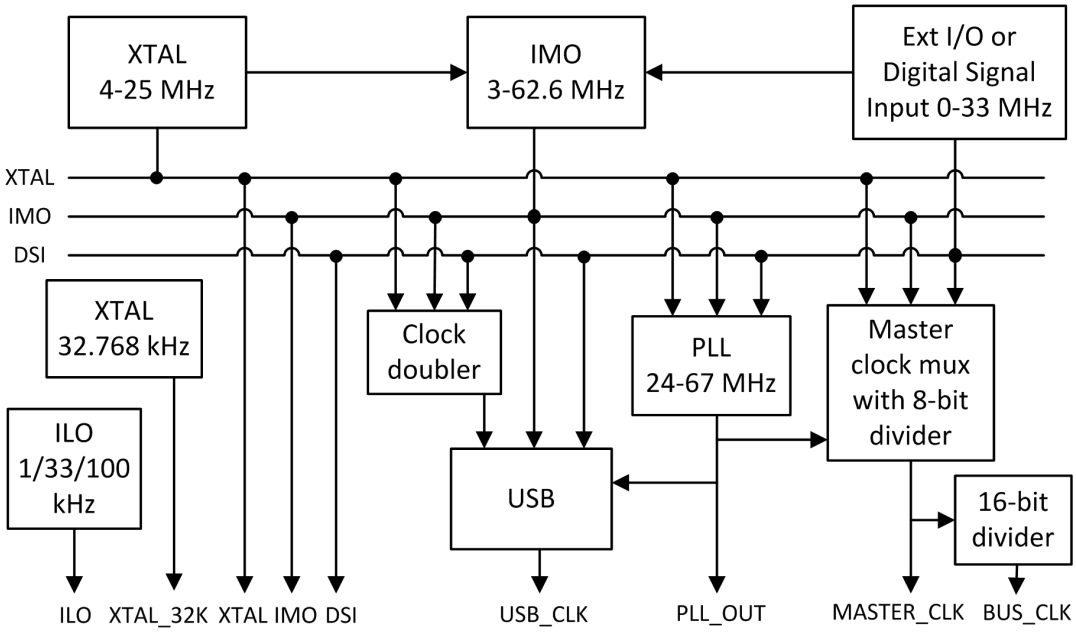
Name	Value
VDDA (V)	5.0
Variable VDDA	False
VDDD (V)	5.0
VDDIO0 (V)	5.0
VDDIO1 (V)	5.0
VDDIO2 (V)	5.0
VDDIO3 (V)	5.0
Temperature Range	-40C - 85/125C

4 Clocks

The clock system includes these clock resources:

- Four internal clock sources increase system integration:
  - 3 to 62.6 MHz Internal Main Oscillator (IMO) ±1% at 3 MHz
  - 1 kHz, 33 kHz, and 100 kHz Internal Low Speed Oscillator (ILO) outputs
  - 12 to 67 MHz clock doubler output, sourced from IMO, MHz External Crystal Oscillator (MHzECO), and Digital System Interconnect (DSI)
  - 24 to 67 MHz fractional Phase-Locked Loop (PLL) sourced from IMO, MHzECO, and DSI
- Clock generated using a DSI signal from an external I/O pin or other logic
- Two external clock sources provide high precision clocks:
  - 4 to 25 MHz External Crystal Oscillator (MHzECO)
  - 32.768 kHz External Crystal Oscillator (kHzECO) for Real Time Clock (RTC)
- Dedicated 16-bit divider for bus clock
- Eight individually sourced 16-bit clock dividers for the digital system peripherals
- Four individually sourced 16-bit clock dividers with skew for the analog system peripherals
- IMO has a USB mode that synchronizes to USB host traffic, requiring no external crystal for USB. (USB equipped parts only)

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq (MHz)	Nominal Freq (MHz)	Accuracy (%)	Start at Reset	Enabled
PLL_OUT	DIGITAL	IMO	24	24	±1	True	True
BUS_CLK	DIGITAL	MASTER_CLK	0	24	±1	True	True
MASTER_CLK	DIGITAL	PLL_OUT	0	24	±1	True	True
IMO	DIGITAL		3	3	±1	True	True
ILO	DIGITAL		0	0.001	-50,+100	True	True
USB_CLK	DIGITAL	IMO	48	0	±0	False	False
Digital Signal	DIGITAL		0	0	±0	False	False
XTAL 32kHz	DIGITAL		0.0328	0	±0	False	False
XTAL	DIGITAL		24	0	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

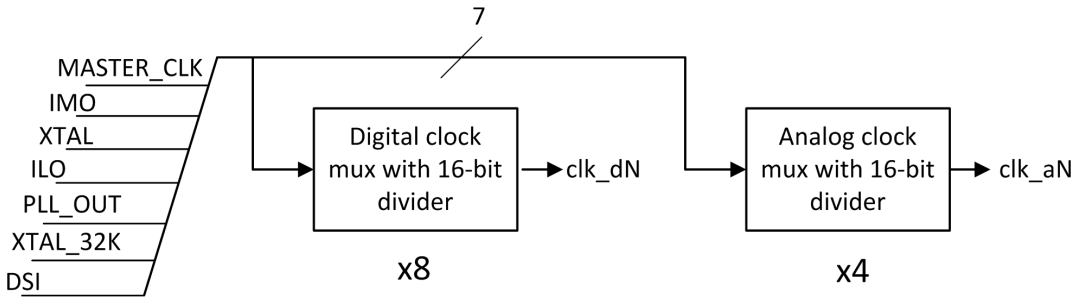


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq (MHz)	Nominal Freq (MHz)	Accuracy (%)	Start at Reset	Enabled
ADC_DelSig_-1_Ext_CP_Clk	DIGITAL	MASTER_CLK	0	24	±1	True	True
Clock_1	DIGITAL	MASTER_CLK	1	1	±1	False	True
ADC_DelSig_-1_theACLK	ANALOG	MASTER_CLK	0.64	0.6316	±1	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 3 Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - o CyPLL API routines
  - o CyIMO API routines
  - o CyILO API routines

- CyMaster API routines
- CyXTAL API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

Name	Priority	Vector
ADC_DelSig_1_IRQ	7	29

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 3 Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

5.2 DMAs

This design contains no DMA components.

6 Flash Memory

PSoC 3 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 12 lists the Flash protection settings for your design.

Table 12. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0xFFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- F - Factory Upgrade
- R - Field Upgrade
- W - Full Protection

For more information on Flash memory and protection, please refer to:

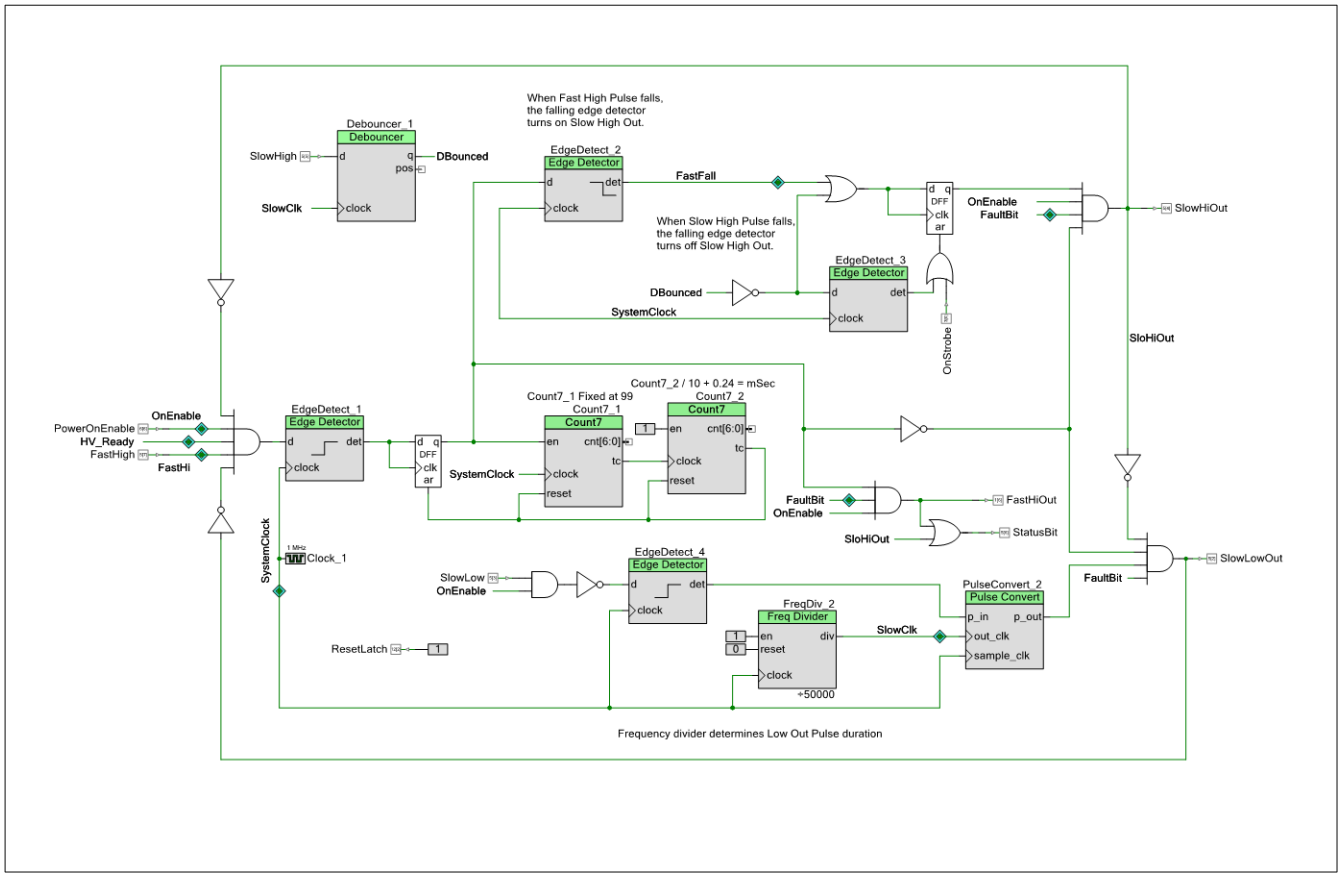
- Flash Protection chapter in the PSoC 3 Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CyWrite API routines
  - CyFlash API routines

7 Design Contents

This design's schematic content consists of the following 2 schematic sheets:

7.1 Schematic Sheet: Page 1

Figure 5. Schematic Sheet: Page 1

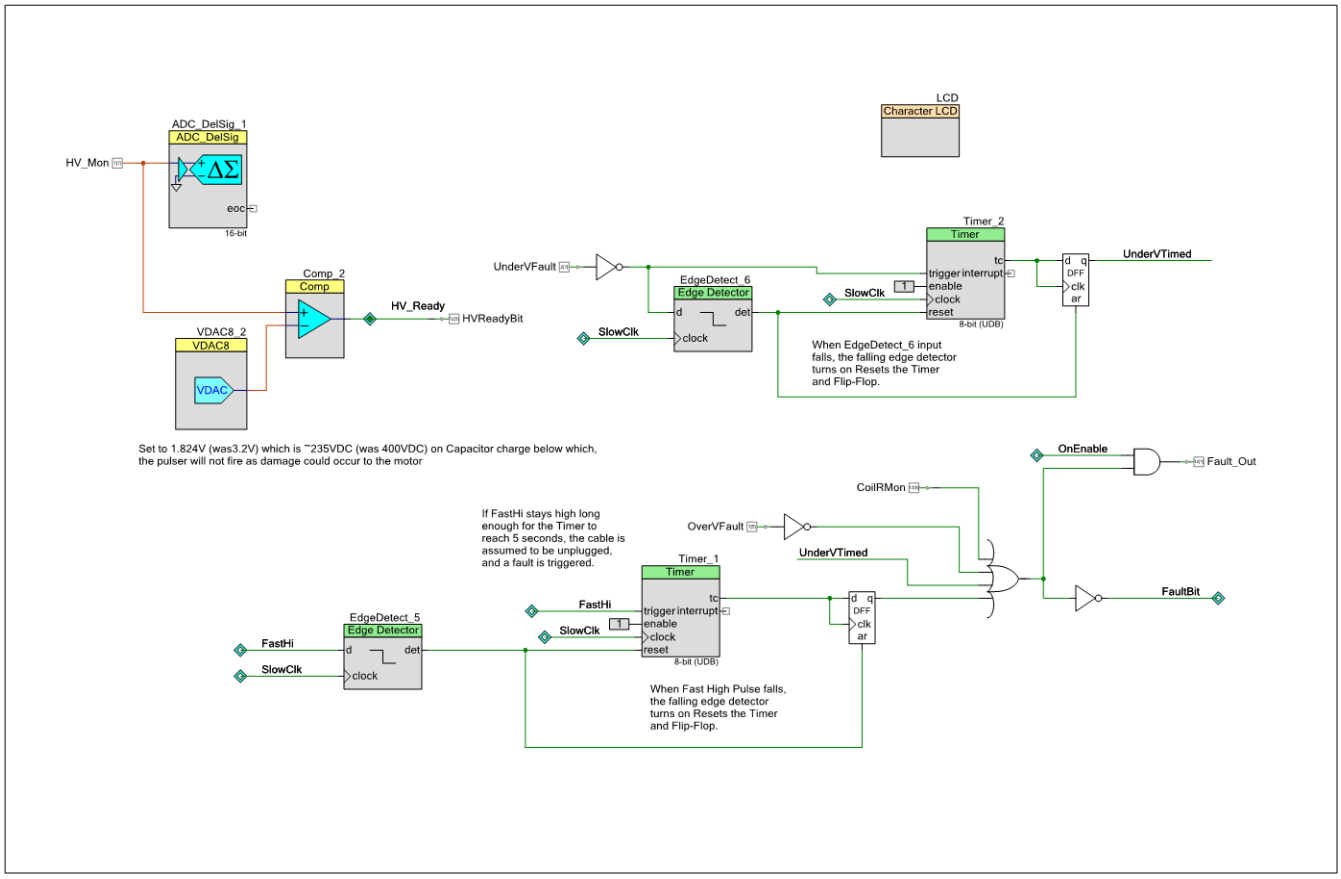


This schematic sheet contains the following component instances:

- Instance Count7_1 (type: Count7_v1_0)
- Instance Count7_2 (type: Count7_v1_0)
- Instance Debouncer_1 (type: Debouncer_v1_0)
- Instance EdgeDetect_1 (type: EdgeDetect_v1_0)
- Instance EdgeDetect_2 (type: EdgeDetect_v1_0)
- Instance EdgeDetect_3 (type: EdgeDetect_v1_0)
- Instance EdgeDetect_4 (type: EdgeDetect_v1_0)
- Instance FreqDiv_2 (type: FreqDiv_v1_0)
- Instance PulseConvert_2 (type: PulseConvert_v1_0)

7.2 Schematic Sheet: Page 2

Figure 6. Schematic Sheet: Page 2



This schematic sheet contains the following component instances:

- Instance ADC_DelSig_1 (type: ADC_DelSig_v3_10)
- Instance Comp_2 (type: Comp_v2_0)
- Instance EdgeDetect_5 (type: EdgeDetect_v1_0)
- Instance EdgeDetect_6 (type: EdgeDetect_v1_0)
- Instance LCD (type: CharLCD_v2_0)
- Instance Timer_1 (type: Timer_v2_60)
- Instance Timer_2 (type: Timer_v2_60)
- Instance VDAC8_2 (type: VDAC8_v1_90)

8 Components

8.1 Component type: ADC_DelSig [v3.10]

8.1.1 Instance ADC_DelSig_1

Description: Delta-Sigma ADC
Instance type: ADC_DelSig [v3.10]
Datasheet: online component datasheet for ADC_DelSig

Table 13. Component Parameters for ADC_DelSig_1

Parameter Name	Value	Description
ADC_Alignment	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Alignment_Config2	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Alignment_Config3	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Alignment_Config4	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Charge_Pump_Clock	true	Low power charge pump clock selection
ADC_Clock	Internal	Parameter for selecting the ADC clock type.
ADC_Input_Mode	Single	Differential or Single ended input mode
ADC_Input_Range	Vssa to Vdda	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config2	0.0 to Vref	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config3	0.0 to Vref	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config4	0.0 to Vref	Choose input operating mode that best supports the range of the signals being measured.
ADC_Power	Medium Power	Sets power level of ADC.
ADC_Reference	Internal Vdda/4	Selects voltage reference source and configuration.
ADC_Reference_Config2	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Reference_Config3	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Reference_Config4	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Resolution	16	ADC Resolution in bits
ADC_Resolution_Config2	16	ADC Resolution in bits
ADC_Resolution_Config3	16	ADC Resolution in bits
ADC_Resolution_Config4	16	ADC Resolution in bits

Parameter Name	Value	Description
Clock_Frequency	64000	Determines the ADC clock frequency.
Comment_Config1	Default Config	Parameter which holds the user comment for the config1.
Comment_Config2	Second Config	Parameter which holds the user comment for the config2.
Comment_Config3	Third Config	Parameter which holds the user comment for the config3.
Comment_Config4	Fourth Config	Parameter which holds the user comment for the config4.
Config1_Name	CFG1	This parameter is used to create constants in the header file for config 1.
Config2_Name	CFG2	This parameter is used to create constants in the header file for config 2.
Config3_Name	CFG3	This parameter is used to create constants in the header file for config 3.
Config4_Name	CFG4	This parameter is used to create constants in the header file for config 4.
Configs	4	Number of active configurations
Conversion_Mode	2 - Continuous	ADC conversion mode
Conversion_Mode_Config2	2 - Continuous	ADC conversion mode
Conversion_Mode_Config3	2 - Continuous	ADC conversion mode
Conversion_Mode_Config4	2 - Continuous	ADC conversion mode
Enable_Vref_Vss	false	Determines whether or not to connect ADC's reference Vssa to AGL[6].
EnableModulatorInput	false	When this parameter is enabled, the modulator input terminal will be enabled on the symbol.
Input_Buffer_Gain	1	Gain of input amplifier
Input_Buffer_Gain_Config2	1	Gain of input amplifier
Input_Buffer_Gain_Config3	1	Gain of input amplifier
Input_Buffer_Gain_Config4	1	Gain of input amplifier
Input_Buffer_Mode	Rail to Rail	Buffer Mode type selection
Input_Buffer_Mode_Config2	Rail to Rail	Buffer Mode type selection
Input_Buffer_Mode_Config3	Rail to Rail	Buffer Mode type selection
Input_Buffer_Mode_Config4	Rail to Rail	Buffer Mode type selection
Ref_Voltage	1.25	Set reference voltage
Ref_Voltage_Config2	1.024	Set reference voltage
Ref_Voltage_Config3	1.024	Set reference voltage
Ref_Voltage_Config4	1.024	Set reference voltage
rm_int	false	Removes internal interrupt (IRQ)
Sample_Rate	10000	Sample Rate in Hz
Sample_Rate_Config2	10000	Sample Rate in Hz
Sample_Rate_Config3	10000	Sample Rate in Hz
Sample_Rate_Config4	10000	Sample Rate in Hz
Start_of_Conversion	Software	Continuous conversions or hardware controlled

8.2 Component type: CharLCD [v2.0]

8.2.1 Instance LCD

Description: Character LCD Component
Instance type: CharLCD [v2.0]
Datasheet: online component datasheet for CharLCD

Table 14. Component Parameters for LCD

Parameter Name	Value	Description
ConversionRoutines	true	Defines if the conversion routines will be included in the project.
CustomCharacterSet	None	Defines the type of custom character set (User defined, Vertical or Horizontal bargraph). Based on the selection a look-up table with proper characters representation will be generated in the source code.

8.3 Component type: Comp [v2.0]

8.3.1 Instance Comp_2

Description: Analog voltage comparator.
Instance type: Comp [v2.0]
Datasheet: online component datasheet for Comp

Table 15. Component Parameters for Comp_2

Parameter Name	Value	Description
Hysteresis	Disable	Enable to add output hysteresis.
Pd_Override	Disable	Power down override to allow comparator to continue operating during sleep.
Polarity	Non Inverting	Allows output to be inverted.
Speed	Slow	Set comparator response speed.
Sync	Bypass	Allows synchronization with clock.

8.4 Component type: Count7 [v1.0]

8.4.1 Instance Count7_1

Description: 7-bit Down Counter (Count7)
Instance type: Count7 [v1.0]
Datasheet: online component datasheet for Count7

Table 16. Component Parameters for Count7_1

Parameter Name	Value	Description
EnableSignal	Enabled	Enables the connection of a routed hardware enable signal.
LoadSignal	Disabled	Enables the connection of a routed hardware load signal.
Period	99	Sets the period register value.

Parameter Name	Value	Description
ResetSignal	Enabled	Enables the connection of a routed asynchronous reset signal.

8.4.2 Instance Count7_2

Description: 7-bit Down Counter (Count7)
Instance type: Count7 [v1.0]
Datasheet: online component datasheet for Count7

Table 17. Component Parameters for Count7_2

Parameter Name	Value	Description
EnableSignal	Enabled	Enables the connection of a routed hardware enable signal.
LoadSignal	Disabled	Enables the connection of a routed hardware load signal.
Period	52	Sets the period register value.
ResetSignal	Enabled	Enables the connection of a routed asynchronous reset signal.

8.5 Component type: Debouncer [v1.0]

8.5.1 Instance Debouncer_1

Description: Debounces the input digital signal from most types of switches
Instance type: Debouncer [v1.0]
Datasheet: online component datasheet for Debouncer

Table 18. Component Parameters for Debouncer_1

Parameter Name	Value	Description
EitherEdgeDetect	false	Specifies whether the positive or negative edge detection is enabled for the component.
NegEdgeDetect	false	Specifies whether the negative edge detection is enabled for the component.
PosEdgeDetect	true	Specifies whether the positive edge detection is enabled for the component.
SignalWidth	1	Determines the bus width of input and output terminals.

8.6 Component type: EdgeDetect [v1.0]

8.6.1 Instance EdgeDetect_1

Description: Edge Detector
Instance type: EdgeDetect [v1.0]
Datasheet: online component datasheet for EdgeDetect

Table 19. Component Parameters for EdgeDetect_1

Parameter Name	Value	Description
EdgeType	Rising Edge	The edge type that this component will detect.

8.6.2 Instance EdgeDetect_2

Description: Edge Detector
Instance type: EdgeDetect [v1.0]
Datasheet: online component datasheet for EdgeDetect

Table 20. Component Parameters for EdgeDetect_2

Parameter Name	Value	Description
EdgeType	Falling Edge	The edge type that this component will detect.

8.6.3 Instance EdgeDetect_3

Description: Edge Detector
Instance type: EdgeDetect [v1.0]
Datasheet: online component datasheet for EdgeDetect

Table 21. Component Parameters for EdgeDetect_3

Parameter Name	Value	Description
EdgeType	Falling Edge	The edge type that this component will detect.

8.6.4 Instance EdgeDetect_4

Description: Edge Detector
Instance type: EdgeDetect [v1.0]
Datasheet: online component datasheet for EdgeDetect

Table 22. Component Parameters for EdgeDetect_4

Parameter Name	Value	Description
EdgeType	Rising Edge	The edge type that this component will detect.

8.6.5 Instance EdgeDetect_5

Description: Edge Detector
Instance type: EdgeDetect [v1.0]
Datasheet: online component datasheet for EdgeDetect

Table 23. Component Parameters for EdgeDetect_5

Parameter Name	Value	Description
EdgeType	Falling Edge	The edge type that this component will detect.

8.6.6 Instance EdgeDetect_6

Description: Edge Detector
Instance type: EdgeDetect [v1.0]
Datasheet: online component datasheet for EdgeDetect

Table 24. Component Parameters for EdgeDetect_6

Parameter Name	Value	Description
EdgeType	Falling Edge	The edge type that this component will detect.

8.7 Component type: FreqDiv [v1.0]

8.7.1 Instance FreqDiv_2

Description: Frequency Divider
Instance type: FreqDiv [v1.0]
Datasheet: online component datasheet for FreqDiv

Table 25. Component Parameters for FreqDiv_2

Parameter Name	Value	Description
Divider	50000	The divider used to generate the div output from the clock input.
HighPulseTime	0	Number of clock cycles each clock period that the div output is high. 0 indicates 50% duty cycle.

8.8 Component type: PulseConvert [v1.0]

8.8.1 Instance PulseConvert_2

Description: Pulse Converter
Instance type: PulseConvert [v1.0]
Datasheet: online component datasheet for PulseConvert

8.9 Component type: Timer [v2.60]

8.9.1 Instance Timer_1

Description: 8, 16, 24 or 32-bit Timer
Instance type: Timer [v2.60]
Datasheet: online component datasheet for Timer

Table 26. Component Parameters for Timer_1

Parameter Name	Value	Description
CaptureAlternatingFall	false	Enables data capture on either edge but not until a valid falling edge is detected first.
CaptureAlternatingRise	false	Enables data capture on either edge but not until a valid rising edge is detected first.

Parameter Name	Value	Description
CaptureCount	2	The CaptureCount parameter works as a divider on the hardware input "capture". A CaptureCount value of 2 would result in an actual capture taking place every other time the input "capture" is changed.
CaptureCounterEnabled	false	Enables the capture counter to count capture events (up to 127) before a capture is triggered.
CaptureMode	None	This parameter defines the capture input signal requirements to trigger a valid capture event
EnableMode	Hardware Only	This parameter specifies the methods in enabling the component. Hardware mode makes the enable input pin visible. Software mode may reduce the resource usage if not enabled.
FixedFunction	false	Configures the component to use fixed function HW block instead of the UDB implementation.
InterruptOnCapture	false	Parameter to check whether interrupt on a capture event is enabled or disabled.
InterruptOnFIFOFull	false	Parameter to check whether interrupt on a FIFO Full event is enabled disabled.
InterruptOnTC	false	Parameter to check whether interrupt on a TC is enabled or disabled.
NumberOfCaptures	1	Number of captures allowed until the counter is cleared or disabled.
Period	99	Defines the timer period (This is also the reload value when terminal count is reached)
Resolution	8	Defines the resolution of the hardware. This parameter affects how many bits are used in the Period counter and defines the maximum resolution of the internal component signals.
RunMode	One Shot	Defines the hardware to run continuously, run until a terminal count is reached or run until an interrupt event is triggered.
TriggerMode	Rising Edge	Defines the required trigger input signal to cause a valid trigger enable of the timer

8.9.2 Instance Timer_2

Description: 8, 16, 24 or 32-bit Timer
Instance type: Timer [v2.60]
Datasheet: online component datasheet for Timer

Table 27. Component Parameters for Timer_2

Parameter Name	Value	Description
CaptureAlternatingFall	false	Enables data capture on either edge but not until a valid falling edge is detected first.
CaptureAlternatingRise	false	Enables data capture on either edge but not until a valid rising edge is detected first.
CaptureCount	2	The CaptureCount parameter works as a divider on the hardware input "capture". A CaptureCount value of 2 would result in an actual capture taking place every other time the input "capture" is changed.
CaptureCounterEnabled	false	Enables the capture counter to count capture events (up to 127) before a capture is triggered.
CaptureMode	None	This parameter defines the capture input signal requirements to trigger a valid capture event
EnableMode	Hardware Only	This parameter specifies the methods in enabling the component. Hardware mode makes the enable input pin visible. Software mode may reduce the resource usage if not enabled.
FixedFunction	false	Configures the component to use fixed function HW block instead of the UDB implementation.
InterruptOnCapture	false	Parameter to check whether interrupt on a capture event is enabled or disabled.
InterruptOnFIFOFull	false	Parameter to check whether interrupt on a FIFO Full event is enabled disabled.
InterruptOnTC	false	Parameter to check whether interrupt on a TC is enabled or disabled.
NumberOfCaptures	1	Number of captures allowed until the counter is cleared or disabled.
Period	39	Defines the timer period (This is also the reload value when terminal count is reached)

Parameter Name	Value	Description
Resolution	8	Defines the resolution of the hardware. This parameter affects how many bits are used in the Period counter and defines the maximum resolution of the internal component signals.
RunMode	One Shot	Defines the hardware to run continuously, run until a terminal count is reached or run until an interrupt event is triggered.
TriggerMode	Rising Edge	Defines the required trigger input signal to cause a valid trigger enable of the timer

8.10 Component type: VDAC8 [v1.90]

8.10.1 Instance VDAC8_2

Description: 8-Bit Voltage DAC
Instance type: VDAC8 [v1.90]
Datasheet: online component datasheet for VDAC8

Table 28. Component Parameters for VDAC8_2

Parameter Name	Value	Description
Data_Source	CPU or DMA (Data Bus)	Selects the method in which the data is written to the vDAC.
Initial_Value	114	Configures the initial vDAC output voltage. The output uses the following relation: Initial output voltage = value*(FullRange/255). This calculated output voltage value is invalid if DAC Bus is used.
Strobe_Mode	Register Write	Selects how the data is strobed into the DAC. For a register write, the data is strobed into the DAC on each CPU or DMA write. If operating in External mode, an external data strobe signal is required.
VDAC_Range	0 - 4.080V (16mV/bit)	Specifies the full voltage scale range of the vDAC
VDAC_Speed	Low Speed	Specifies the vDAC settling speed. Note that the 'Slow Speed' selection consumes less power.
Voltage	1824	This parameter sets the voltage value.

9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 3 register map is covered in the PSoC 3 Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 3 Technical Reference Manual
  - Low Power Modes chapter in the PSoC 3 Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines
- Cache Management
  - Cache Controller chapter in the PSoC 3 Technical Reference Manual
  - Cache chapter in the System Reference Guide