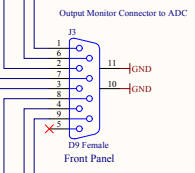


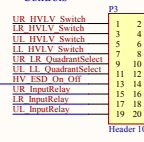
PS Page 13
PowerSupplies.SchDoc

Part1
Panel Mount SHV Cable Assembly (SHV Jack to BNC)
Manufacturer Part Number: SHVJBS-RG58-BNCM-1-4
Quantity: 10
Manufacturer: Field Components



Binary IO to rear board via ribbon

Controls



All inputs are tied on this board to either 20k pull up resistors, or relay coils resulting in the default condition being a logic high in the absence of a logic input from an external control source.

HV.LV.Switch - If actively pulled low will result in the LV path being open, and the HV path being closed.

QuadrantSelect - If actively pulled low will select the PI_out1 connection corresponding to either LL or LR.

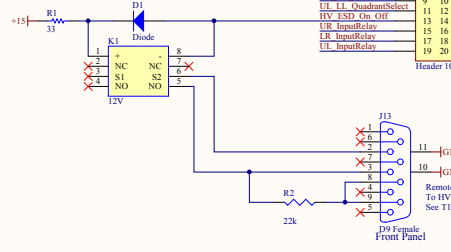
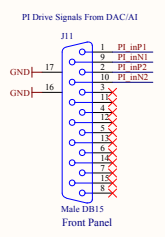
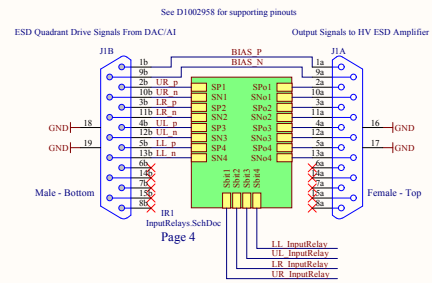
HV ESD On/Off - This is a toggle function. If this input is actively pulled low for > .5seconds, the state will toggle between on and off.

Input Relay - If actively pulled low will connect DAC input to HV ESD amplifier

Pole Zero Bypass - If actively pulled low, the pole-zero are engaged

Version History:

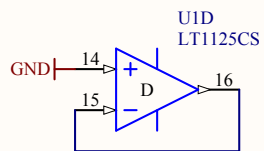
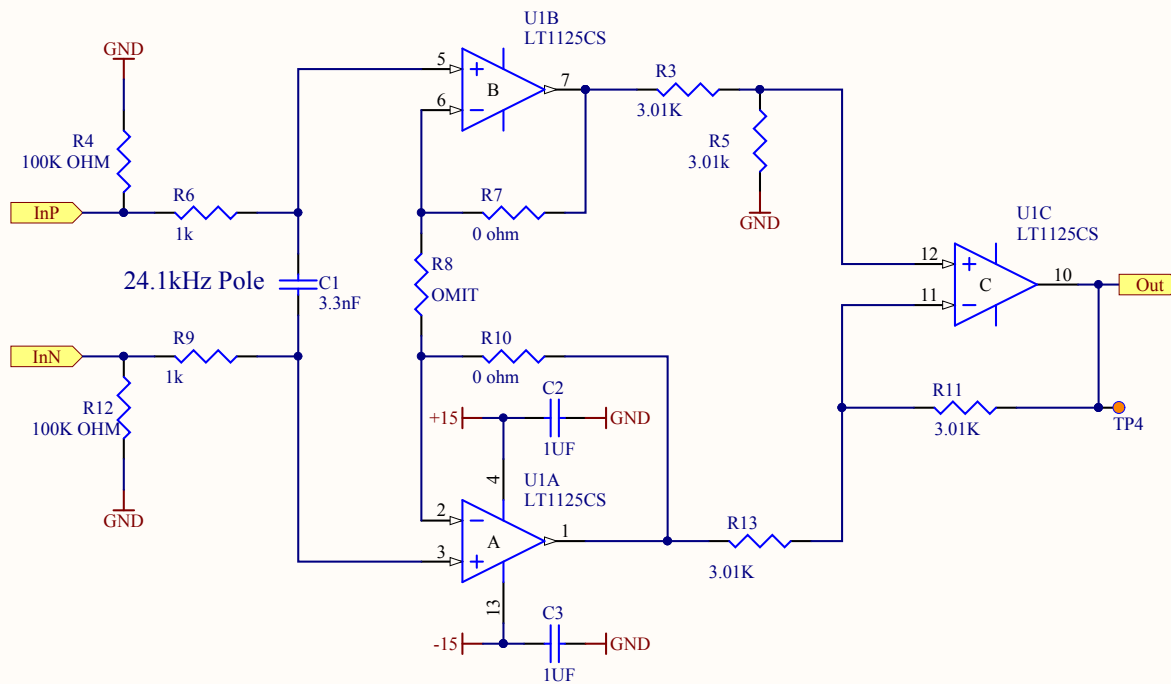
- v1 - Initial release, two PCBs created S1500066 and S1500067
- v2 - New PCB release. Changes are:
 1. Rearranged the bits serving the input relays for better mapping
 2. Changed opamps in High Pass Filter from OP27 to AD829 for higher slew rate. Added 68pF compensation capacitors for AD829
 3. Changed the Quadrant Selector relay, K8, to be able to terminate unused channels in short to avoid inconsistent loading of unused PI input to quadrant drive
 4. Added page numbering to top sheet for ease of browsing
- v3 - Component value changes per ECR E1500341
 1. Changed C32 in monitoring amplifier from 1uF to 0.047uF to increase the dynamic range of the normal quadrant paths such that inspiral waveforms may be adequately injected at higher frequencies
 2. Changed C36 in the summing node from 1uF to 0.047uF to increase the dynamic range of the normal quadrant paths such that inspiral waveforms may be adequately injected at higher frequencies
 3. Corrected typo on DAC noise spectrum from 800uV to 800mV



+380mA, -190mA Measured Quiescent +/- 18V Current Draw

Title	Top Level ETM Low Voltage ESD Driver	LRGO Laboratory California Institute of Technology Massachusetts Institute of Technology	LIGO
Size	C	DCC Number: D1500016	SCH / PCB Revision: V3
Date	11/18/2015	Engineer: R.Abbott	Time: 3:30:10 PM
Page	1	of 12	

Overall Gain = 1 from InP-InN to Out
 Ex. 10V battery across input = 10V from Out to GND



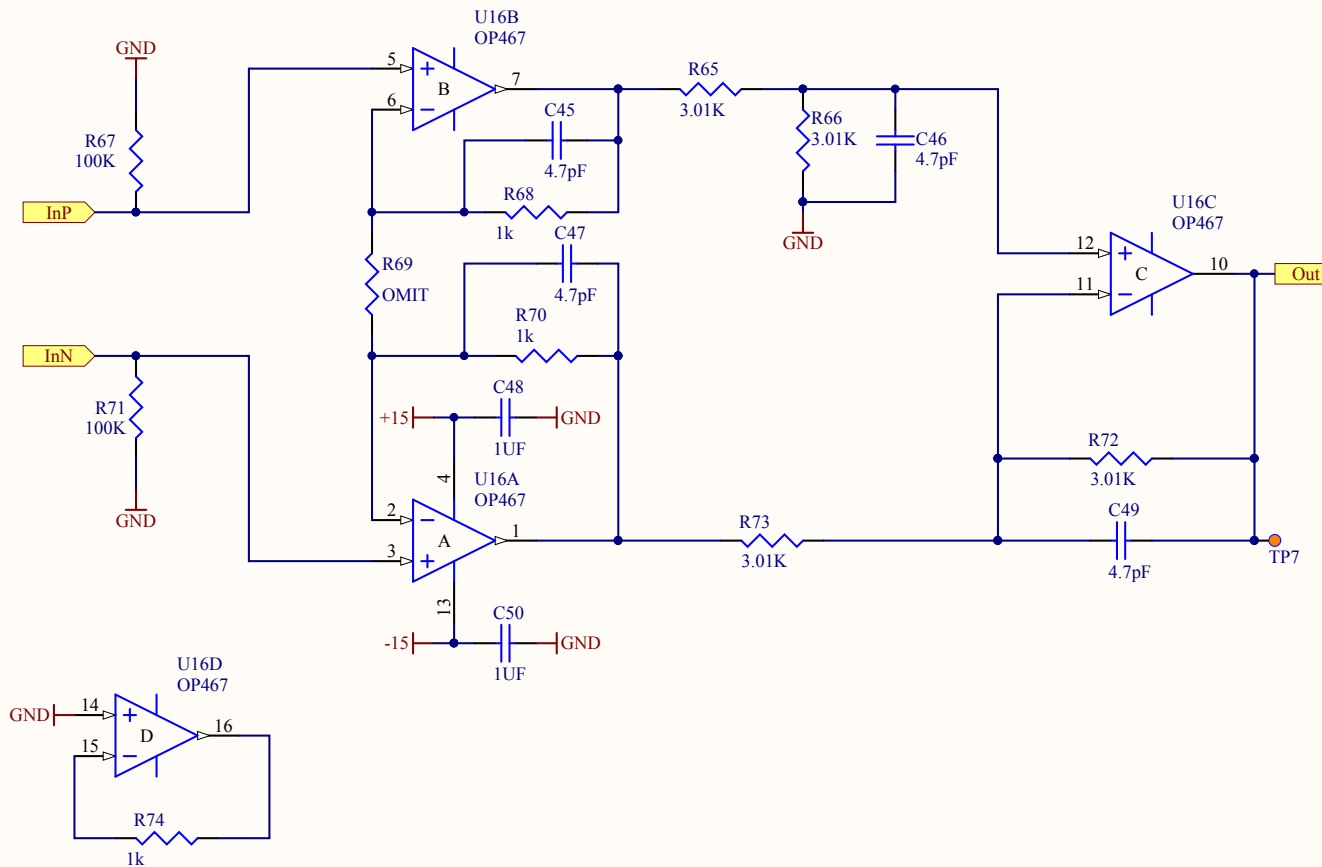
The 24.1kHz RC filter is there to cut high frequency noise to prevent slew rate limiting. Overall gain is 1 such that 10 volts peak from DAC yields 10v wrt ground at output

Checked All

Last Edited: 9/16/2015

Title Differential Receiver		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology		LIGO
Size: A	DCC Number: D1500016	Revision: V3	Engineer: R. Abbott	
File: C:\Rich's Files\Mycadfiles\Suspensions\ETM LVLN Driver\DifferentialReceiver.SchDoc			Date: 11/18/2015	Time: 3:30:10 PM
				Sheet 2 of 15

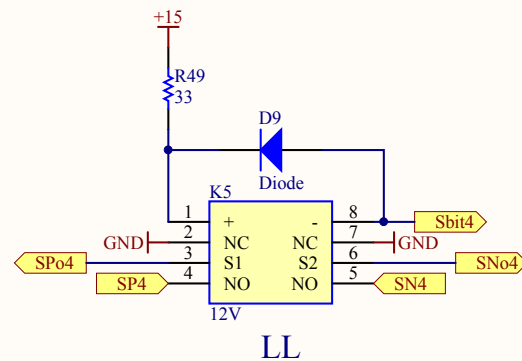
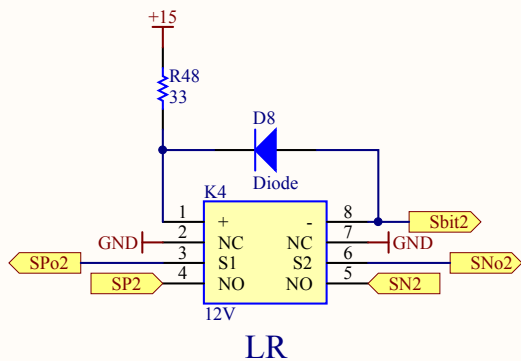
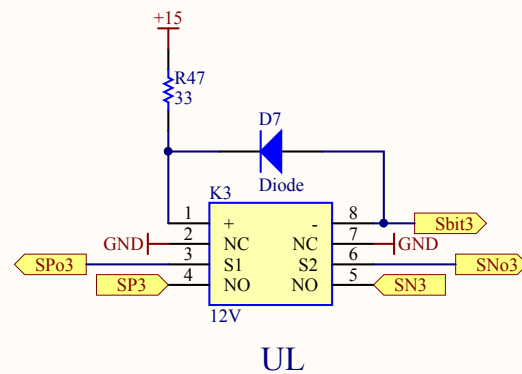
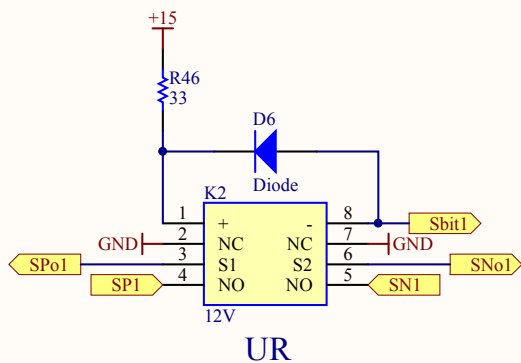
Overall Gain = 1 from InP-InN to Out
 Ex. 10V battery across input = 10V from Out to GND



Checked All

Last Edited: 9/16/2015

Title		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology		LIGO
Fast Differential Receiver				
Size: A	DCC Number: D1500016	Revision: V3	Engineer: R. Abbott	Date: 11/18/2015
				Time: 3:30:10 PM
File: C:\Rich's Files\Mycadfiles\Suspensions\ETM LVLN Driver\FastDiffRec.SchDoc				Sheet 3 of 15

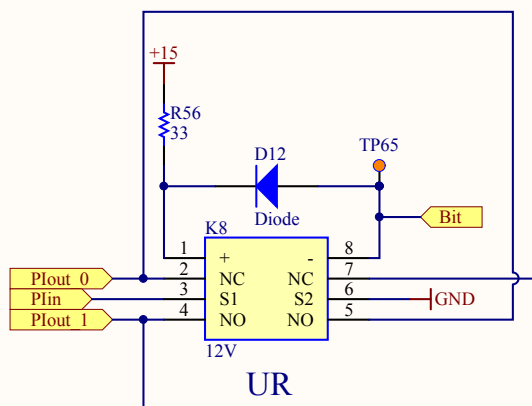


These relays are used to disconnect the applied differential DAC signals from the high voltage ESD amplifier after transition to low voltage control.

Checked All

Last Edited: 9/16/2015

Title Input Relays		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology		LIGO
Size: A	DCC Number: D1500016	Revision: V3	Engineer: R. Abbott	
Date: 11/18/2015			Time: 3:30:10 PM	
Sheet 4 of 15				



Only a total of 2 ADC channels were available within the existing SUS topology for the PI input. This switch allows the user to select which two quadrants of a test mass will receive the PI correction signals.

The grounded pin on S2 terminates the unused leg of the PI output path to mimic the voltage source that would have been connected. Failure to do this would result in a change in the transfer function of the passive summing network.

Bit control input pulling low will select the PInout_1 path and vice versa

Last Edited: 9/16/2015

Title
Quadrant Selector

LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology

LIGO

Size: A

DCC Number: D1500016

Revision: V3

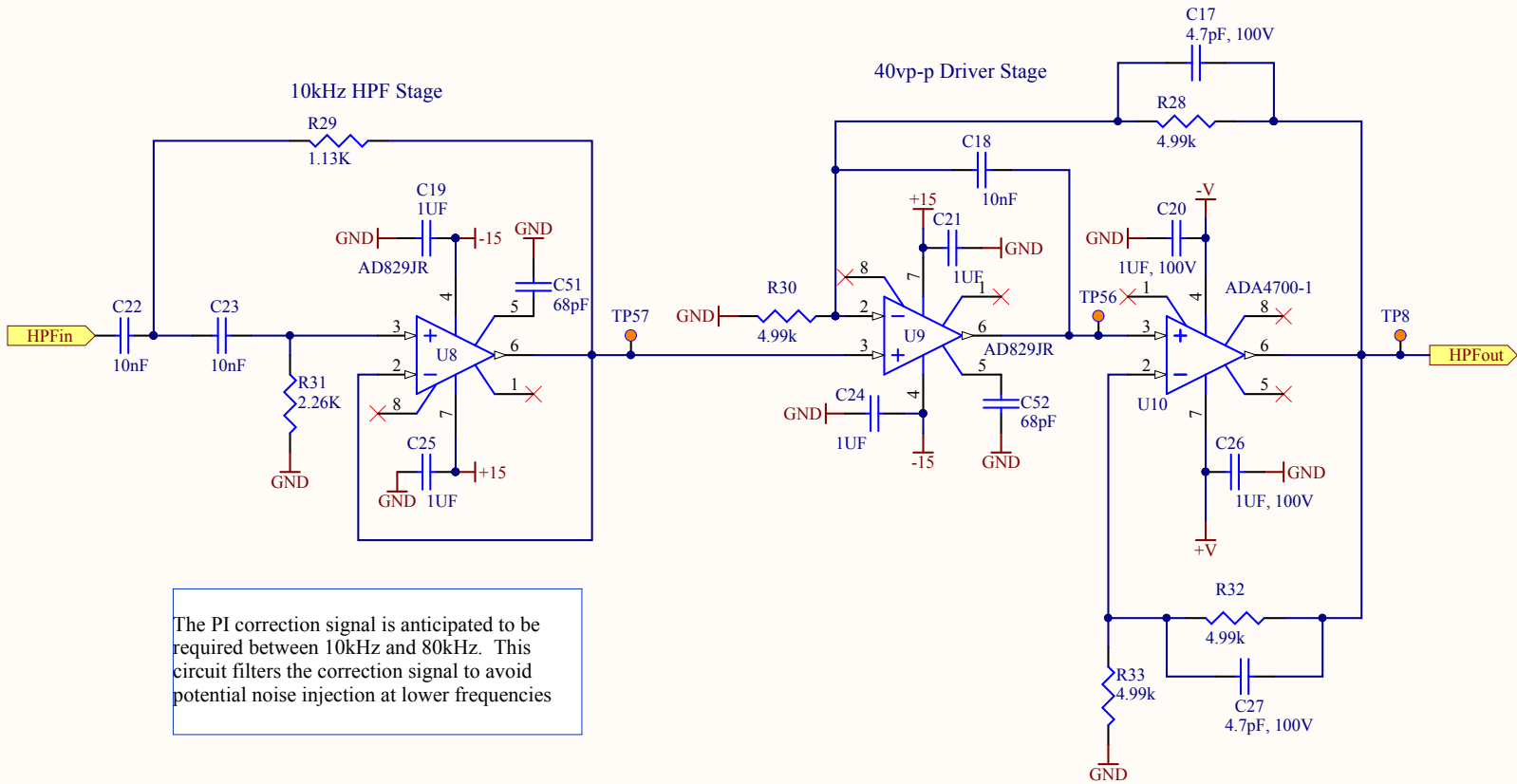
Engineer: R. Abbott

Date: 11/18/2015

Time: 3:30:10 PM

File: C:\Rich's Files\Mycadfiles\Suspensions\ETM LVLN Driver\QuadrantSelector.SchDoc

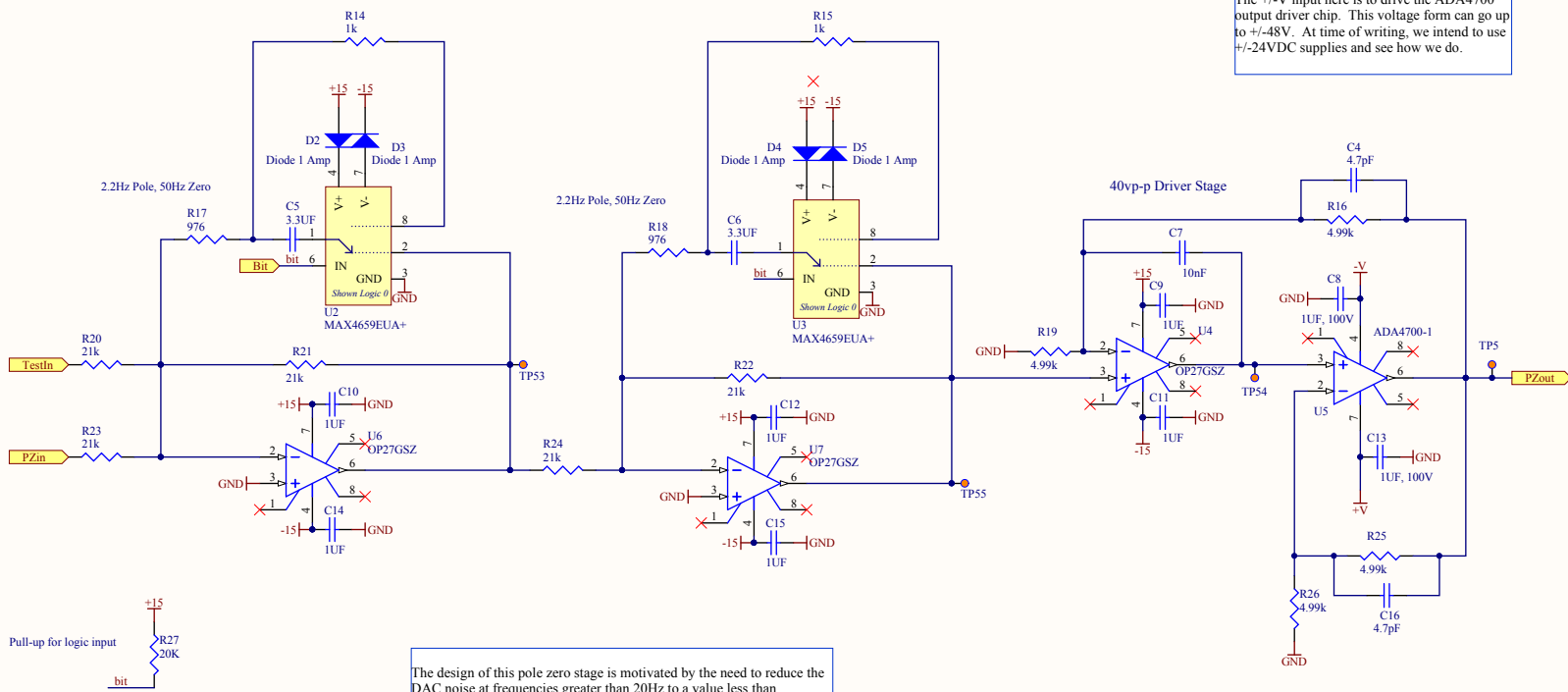
Sheet 5 of 15



The +/-V input here is to drive the ADA4700 output driver chip. This voltage form can go up to +/-48V. At time of writing, we intend to use +/-24VDC supplies and see how we do.

The PI correction signal is anticipated to be required between 10kHz and 80kHz. This circuit filters the correction signal to avoid potential noise injection at lower frequencies

Title		Last Edited: 9/16/2015	
10kHz Sallen Key HPF		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology	
Size: A	DCC Number: D1500016	Revision: V3	Engineer: R. Abbott
File: C:\Rich's Files\Mycadfiles\Suspensions\ETM LVLN Driver\HPF.SchDoc		Date: 11/18/2015	Time: 3:30:10 PM
		Sheet 6 of 15	



The +/-V input here is to drive the ADA4700 output driver chip. This voltage form can go up to +/-48V. At time of writing, we intend to use +/-24VDC supplies and see how we do.

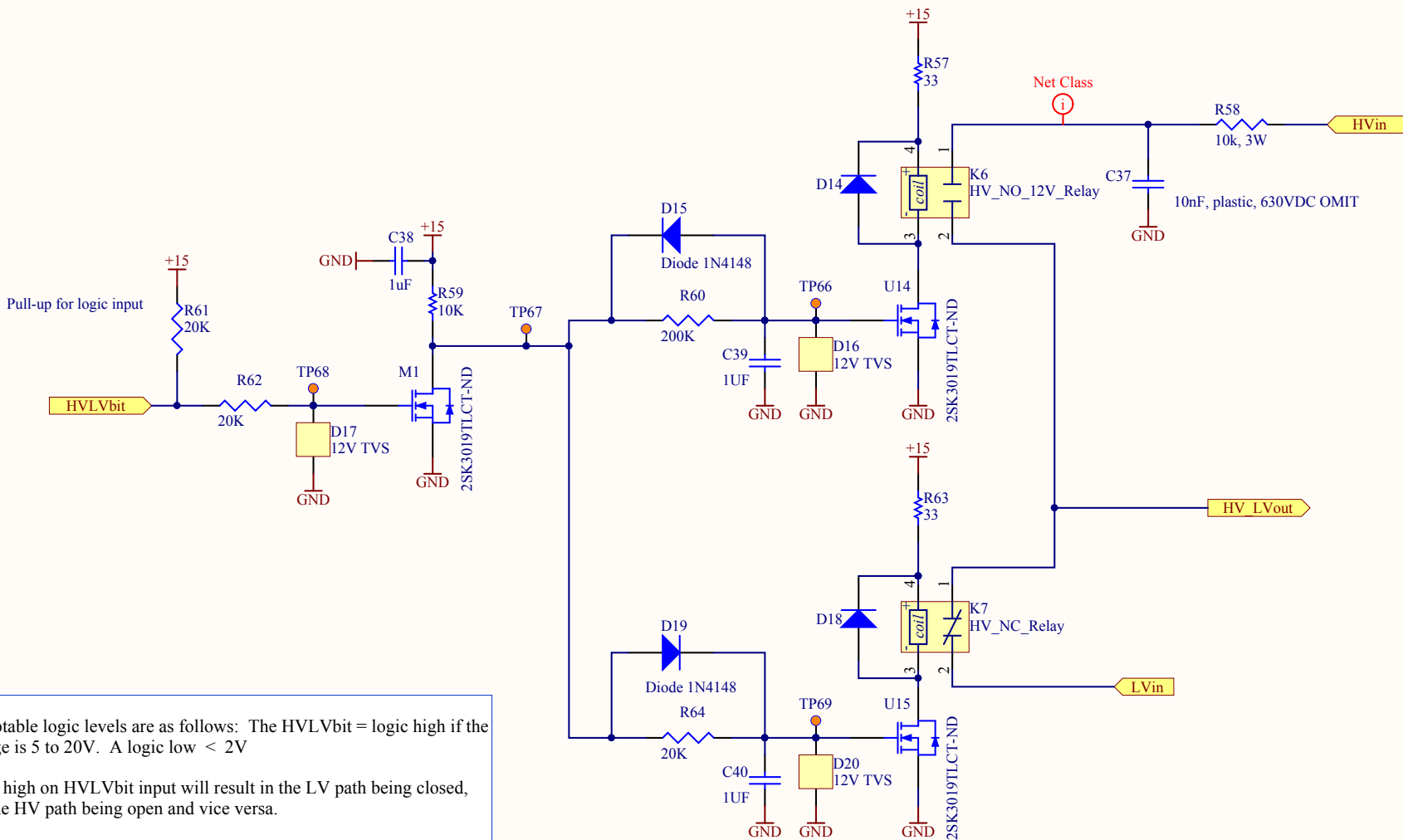
The design of this pole zero stage is motivated by the need to reduce the DAC noise at frequencies greater than 20Hz to a value less than 40nV/rHz. The DAC noise is estimated (per G1401399-v2) to be 800nV/rHz at 20 Hz. The choice of pole and zero frequency above results in a predicted circuit output noise of 28nV/rHz at 20Hz in the presence of the anticipated DAC noise. The zero preserves some drive dynamic range at intermediate frequencies.

The ADA4700-1 stage provides the capability to increase the dynamic range to 40vp-p

Checked All

Last Edited: 9/16/2015

Title Pole-Zero and Driver		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology		LIGO	
Size: B	DCC Number: D1500016	Revision: V3	Engineer: R. Abbott	Date: 11/18/2015	Time: 3:30:10 PM
				Sheet 7 of 15	



Acceptable logic levels are as follows: The HVLVbit = logic high if the voltage is 5 to 20V. A logic low < 2V

Logic high on HVLVbit input will result in the LV path being closed, and the HV path being open and vice versa.

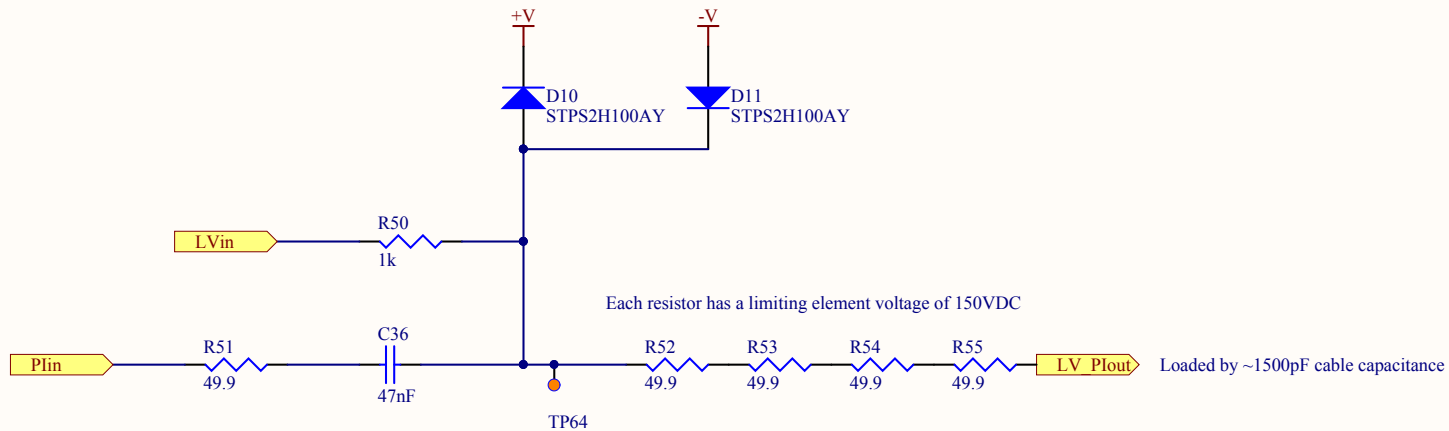
Due to the action of the RC filters on the FET gates, a delay (30mSec minimum) is introduced ensuring the HV path will never be closed while the LV path is closed. Failure to do this would connect the HV circuit to the LV which would be bad.

The uncommanded state results in the HV being OFF and the LV being ON

The 10nF HV capacitor on the output can be optionally utilized to lower the source impedance in the event that is useful.

Title		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology	
High & Low Voltage Transition Relays		LIGO	
Size: A	DCC Number: D1500016	Revision: V3	Date: 11/18/2015
File: C:\Rich's Files\Mycadfiles\Suspensions\ETM LVLN Driver\HV Relays.SchDoc		Engineer: R. Abbott	Time: 3:30:10 PM
			Sheet 8 of 15

Last Edited: 9/16/2015



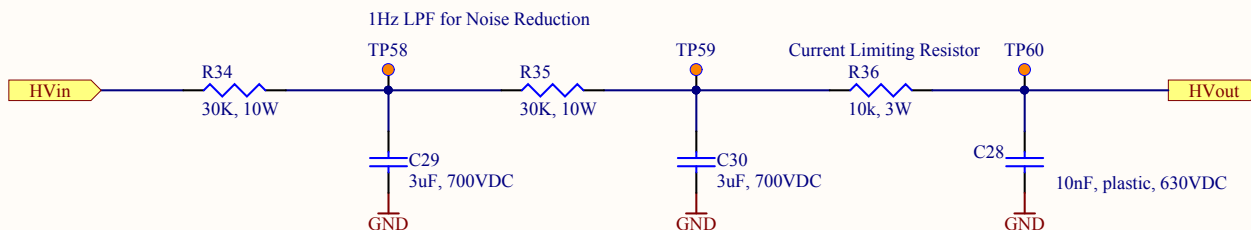
This summing node combines the low frequency DC coupled signals present in the normal feedback path to each quadrant with the parametric instability correction signal. The summing was done passively to allow greater dynamic range than that afforded by an active summing stage. The STPS2H100AY diodes and output 200 ohm resistor string dissipate the potential stored charge present on the output cable leading to the vacuum system and limit the instantaneous current to be less than 2 amperes assuming worst case cable charge of 400VDC and 1500pF cable capacity.

Checked All

Last Edited: 9/16/2015

Title		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology		LIGO
Output Summing Node				
Size: A	DCC Number: D1500016	Revision: V3	Engineer: R. Abbott	Date: 11/18/2015
				Time: 3:30:11 PM
File: C:\Rich's Files\Mycadfiles\Suspensions\ETM LVLN Driver\OutputSum.SchDoc				Sheet 9 of 15

This filter can store charge. Assume the capacitors are charged until positively discharged and measured.



From T1400406 by Rai Weiss, this filter lowers the voltage noise on the bias path. This path has no requirement for fast frequency response beyond the ability to set the bias voltage on a human timescale.

An additional 10k series resistor is conservatively included as a hedge against an in-vacuum discharge event. The 10nF HV capacitor on the output can be optionally utilized to lower the source impedance to the bias electrode in the event that is useful.

Last Edited: 9/16/2015

Title
High Voltage Bias Filter

LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology

LIGO

Size: A

DCC Number: D1500016

Revision: V3

Engineer: R. Abbott

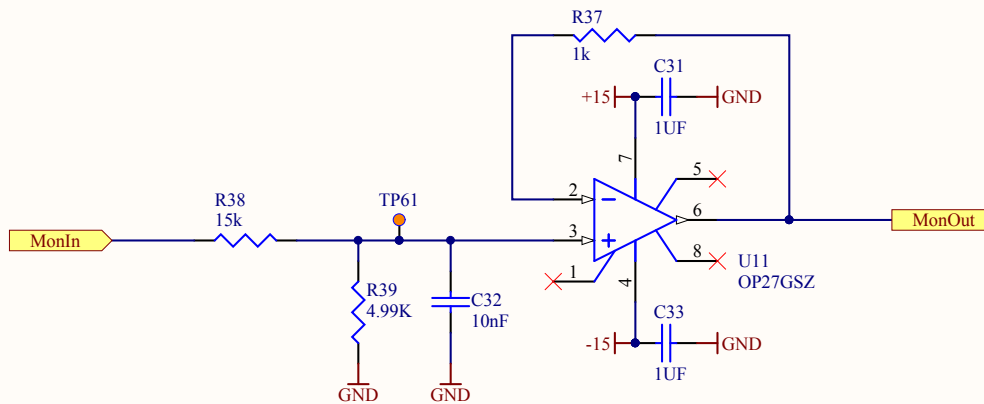
Date: 11/18/2015

Time: 3:30:11 PM


File: C:\Rich's Files\Mycadfiles\Suspensions\ETM LVLN Driver\HV Filter.SchDoc

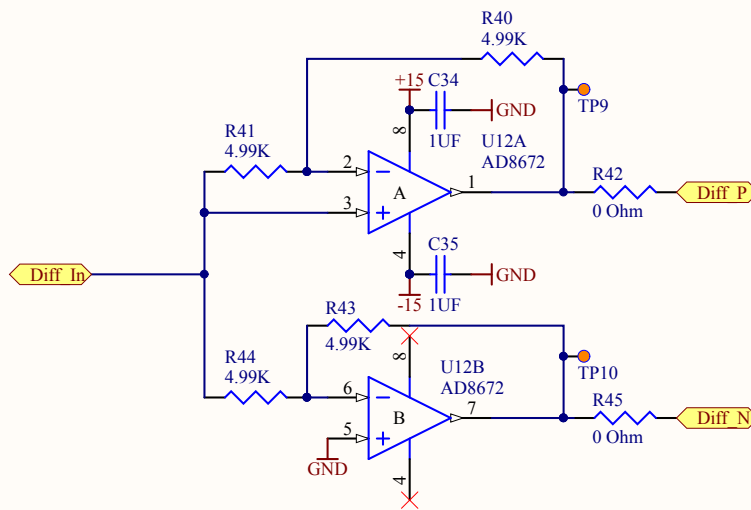
Sheet 10 of 15

The large dynamic range of the output drivers (40vp-p) requires this monitor to attenuate the input signal. A pole at 1kHz is included for further attenuation of the PI band.



Last Edited: 11/18/2015

Title		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology		
Monitoring Amplifier				
Size: A	DCC Number: D1500016	Revision: V3	Engineer: R. Abbott	Date: 11/18/2015
				Time: 3:30:11 PM
File: C:\Rich's Files\Mycadfiles\Suspensions\ETM LVLN Driver\MonAmp.SchDoc				Sheet 11 of 15



Typical LIGO differential driver circuit for the monitor signals.

Last Edited: 9/16/2015

Title
Differential Driver

LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology



Size: A DCC Number: D1500016 Revision: V3

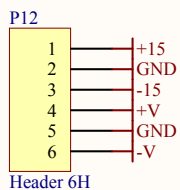
Engineer: R. Abbott

Date: 11/18/2015

Time: 3:30:11 PM

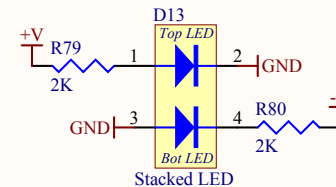
Part2
 Pins for female molex connector
 WM2307-ND
 Quantity: 6

Part3
 Mating 6 pin molex connector
 WM2126-ND

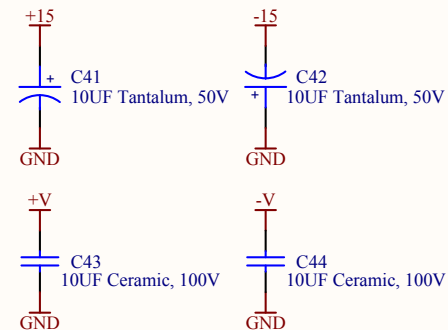
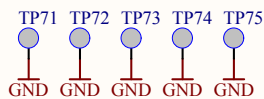
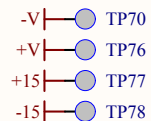
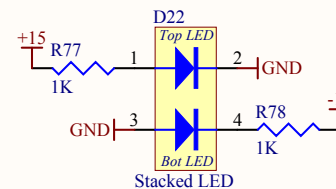


The +/-V input here is to drive the ADA4700 output driver chip. This voltage form can go up to +/-48V. At time of writing, we intend to use +/-24VDC supplies and see how we do.

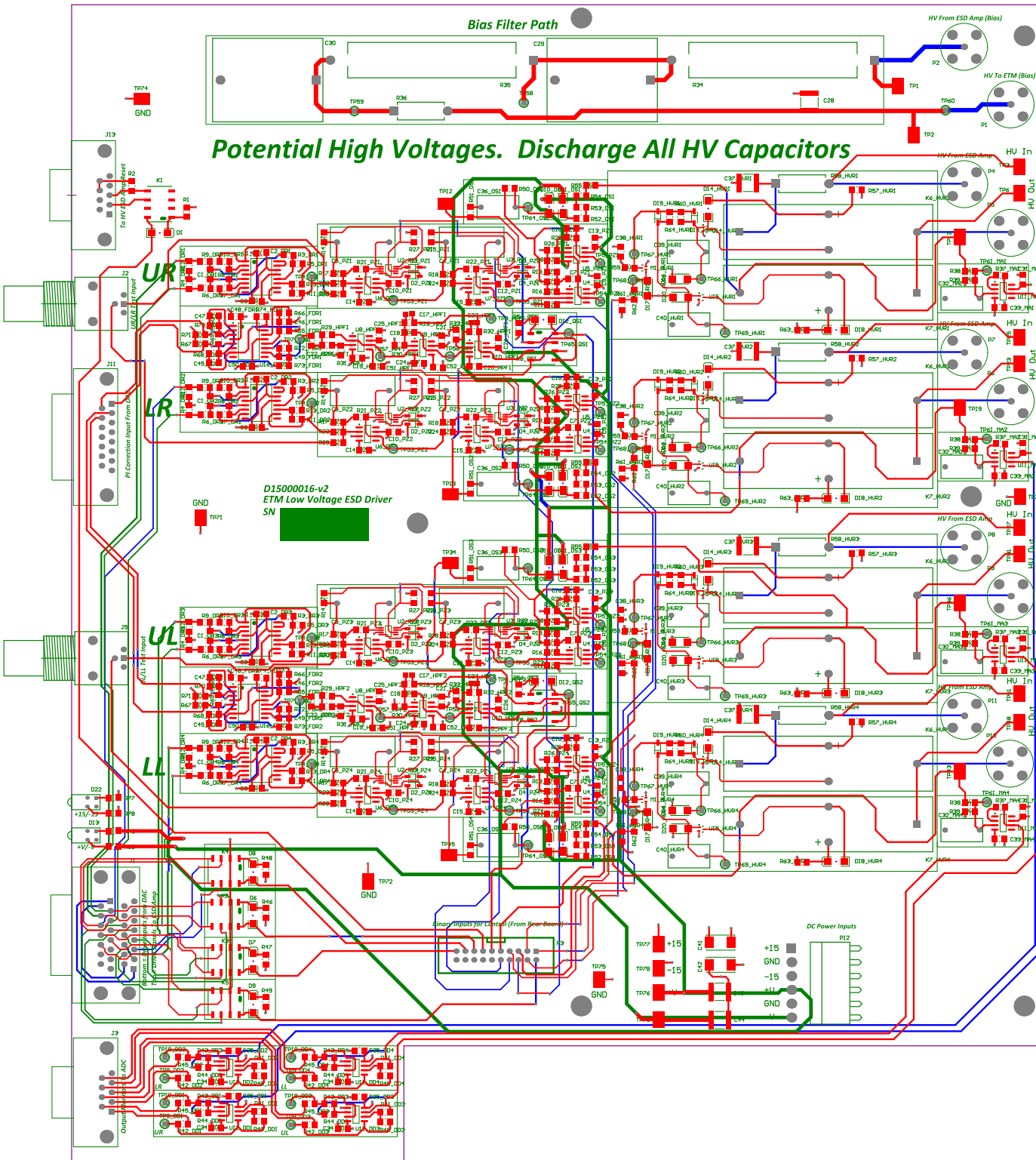
+V/-V Power LED



15VDC Power LED



Title Power Supplies		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology		Last Edited: 9/16/2015	
Size: A	DCC Number: D1500016	Revision: V3	Engineer: R. Abbott	Date: 11/18/2015	LIGO
File: C:\Rich's Files\Mycadfiles\Suspensions\ETM LVLN Driver\PowerSupplies.SchDoc				Time: 3:30:11 PM	
				Sheet 13 of 15	



Bias Filter Path

Potential High Voltages. Discharge All HV Capacitors

**D15000016-v2
ETM Low Voltage ESD Driver
SN**

Binary Inputs for Control (From Back Board)

DC Power Inputs

UR

LR

UL

LL

UR

HV From ESD Amp (Bias)

HV To ETM (Bias)

HV From ESD Amp

HV To ESD Amp

HV From ESD Amp

HV To ESD Amp

HV From ESD Amp

HV To ESD Amp

HV From ESD Amp

HV To ESD Amp

HV From ESD Amp

HV To ESD Amp

HV From ESD Amp

HV To ESD Amp

HV From ESD Amp

HV To ESD Amp

HV From ESD Amp

HV To ESD Amp

LIGO Bill of Materials

Design Data From: Board Designed By: Board Date: Board Revision: Reviser:

ETB L10A Driver_v4_P0P0E R. Abbott 01/2008 V3 None

Creation Date: 11/20/2015 Print Date: 08/26/15

3:30:25 PM 3:30:25 PM

Main Bill of Materials table with columns: Designator, Comment, Description, Quantity, Manufacturer Part Number, Quantity. Contains thousands of rows listing electronic components like resistors, capacitors, diodes, and integrated circuits.