Room Temperature Mechanical Loss of Silicon Nitride-Silica Quarter-wave Stacks Deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) Method

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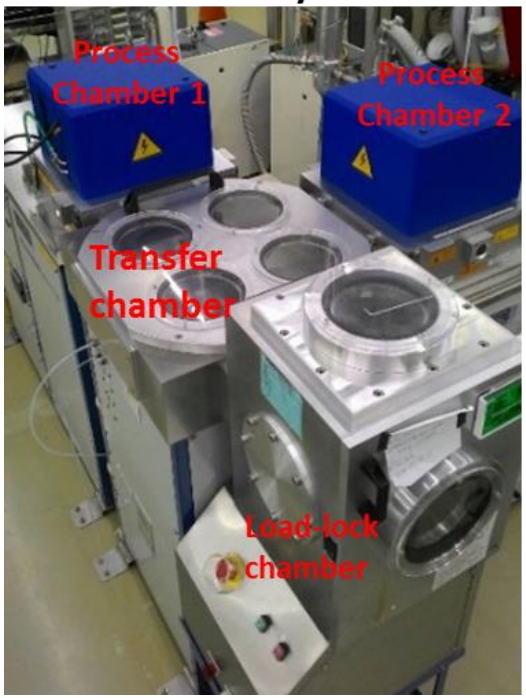
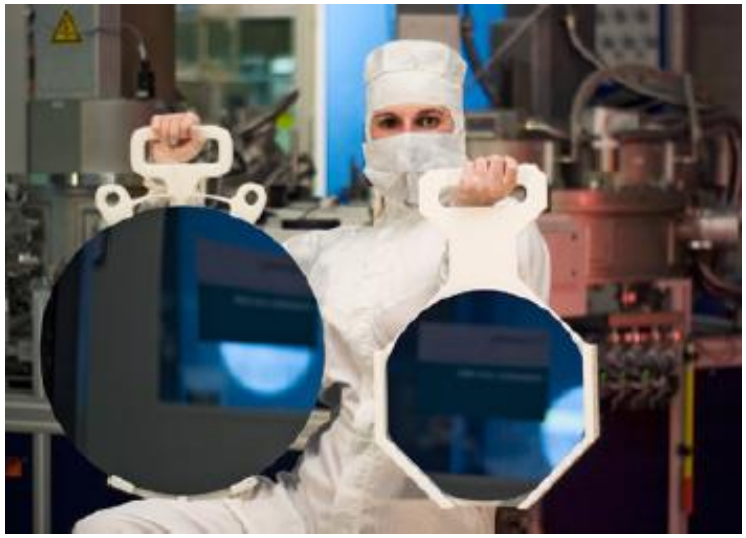
Large area uniform coating on silicon wafer up to 18“ (450mm) by Plasma Enhanced Chemical Vapor Deposition (PECVD) is a common practice in silicon-IC industry

PECVD system





http://www.linx-consulting.com/pages/450mm_processing.html

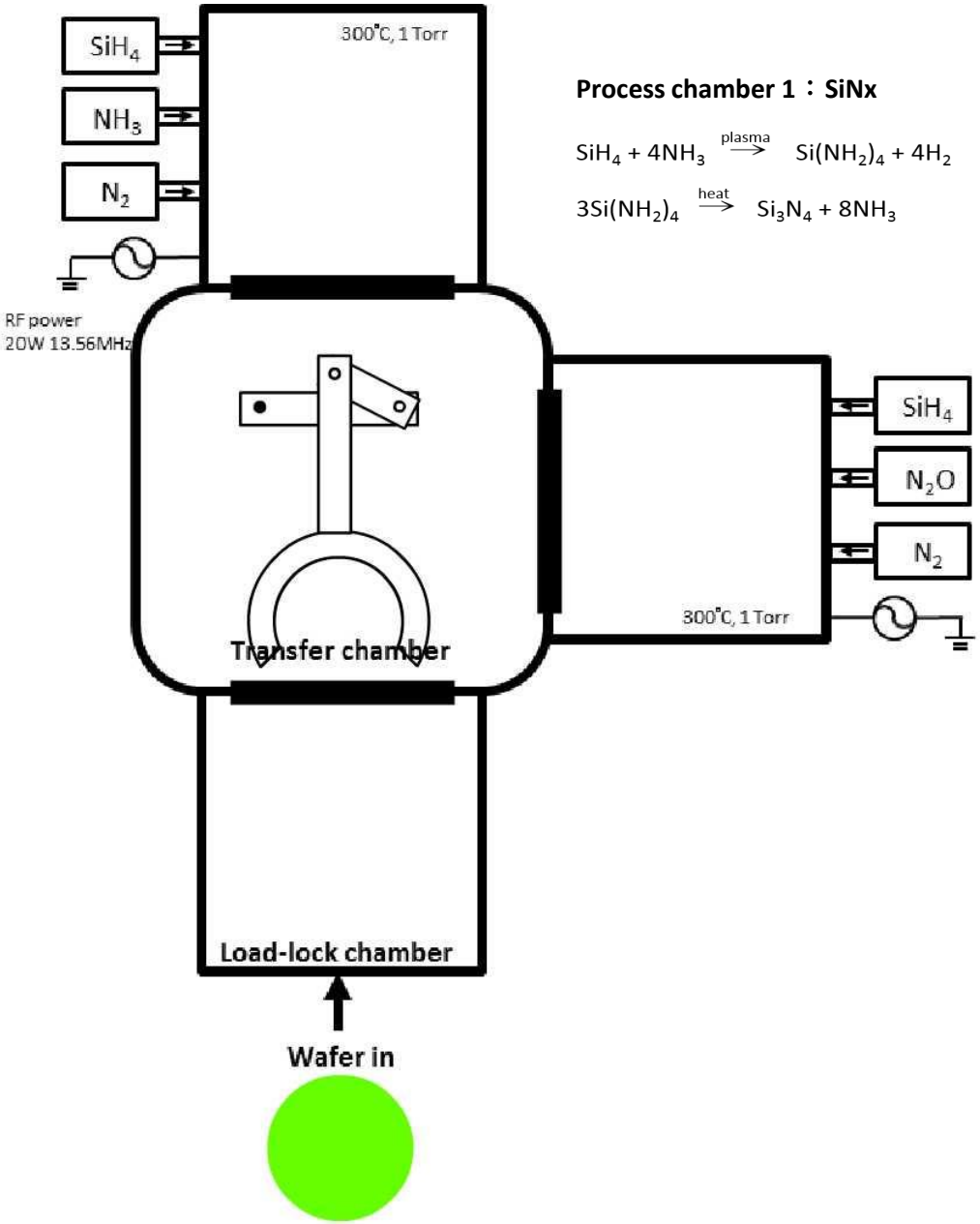
At NTHU, we are exploring mirror deposition for LIGO by using PECVD

Candidate Silicon IC-Compatible CVD Thin Films for Optical Application

	a-Si	SiC	SiNx	SiO_2
Refractive index @ 1550 nm	3.5[1]	3.2-2.6[11,12]	2.6-1.8[16][30]	1.45[19,20]
Absorption range	<700 nm[2]	<380 nm [13]	<510 nm[17]	<200 nm[21]
Young's modulus (GPa)	100 ~ 150[3-5]	392 ~ 694[14]	85~210[16]	72~83[20,22-25]
Stress# (MPa)	-400 ~ -900[6,7]	-160 ~ -510[15]	+600 ~ 1200 [16]	+60 ~ -257[25]
Loss angle at RT	3.3×10^{-4} e beam[8] 5×10^{-4} sputter[8] 4×10^{-4} IBS [31] 9×10^{-5} IBS [10]	--	$\sim2\times10^{-6}$ high stress [18] $\sim3\times10^{-4}$ stress relief [18] 7.5×10^{-5} $SiN_{0.40}$ @107Hz 1.4×10^{-5} $SiN_{0.87}$ @107Hz[30]	1.49×10^{-4} 1×10^{-4} IBS [26-28]
Cryogenic loss peak	Depends on H^+-concentration and heat treatment[8-10]	--	Depends on N-concentration (Preliminary results will be presented in poster session by Mr. Kuo)	5×10^{-4} @20K[29]

- : compressive +: tensile

Plasma Enhanced Chemical Vapor Deposition (PECVD) for multi-layer dielectric mirror coating



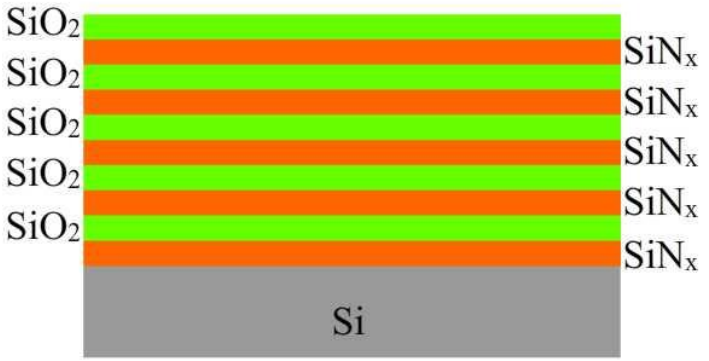
Process chamber 1 : SiNx

$SiH_4 + 4NH_3 \xrightarrow{plasma} Si(NH_2)_4 + 4H_2$

$3Si(NH_2)_4 \xrightarrow{heat} Si_3N_4 + 8NH_3$

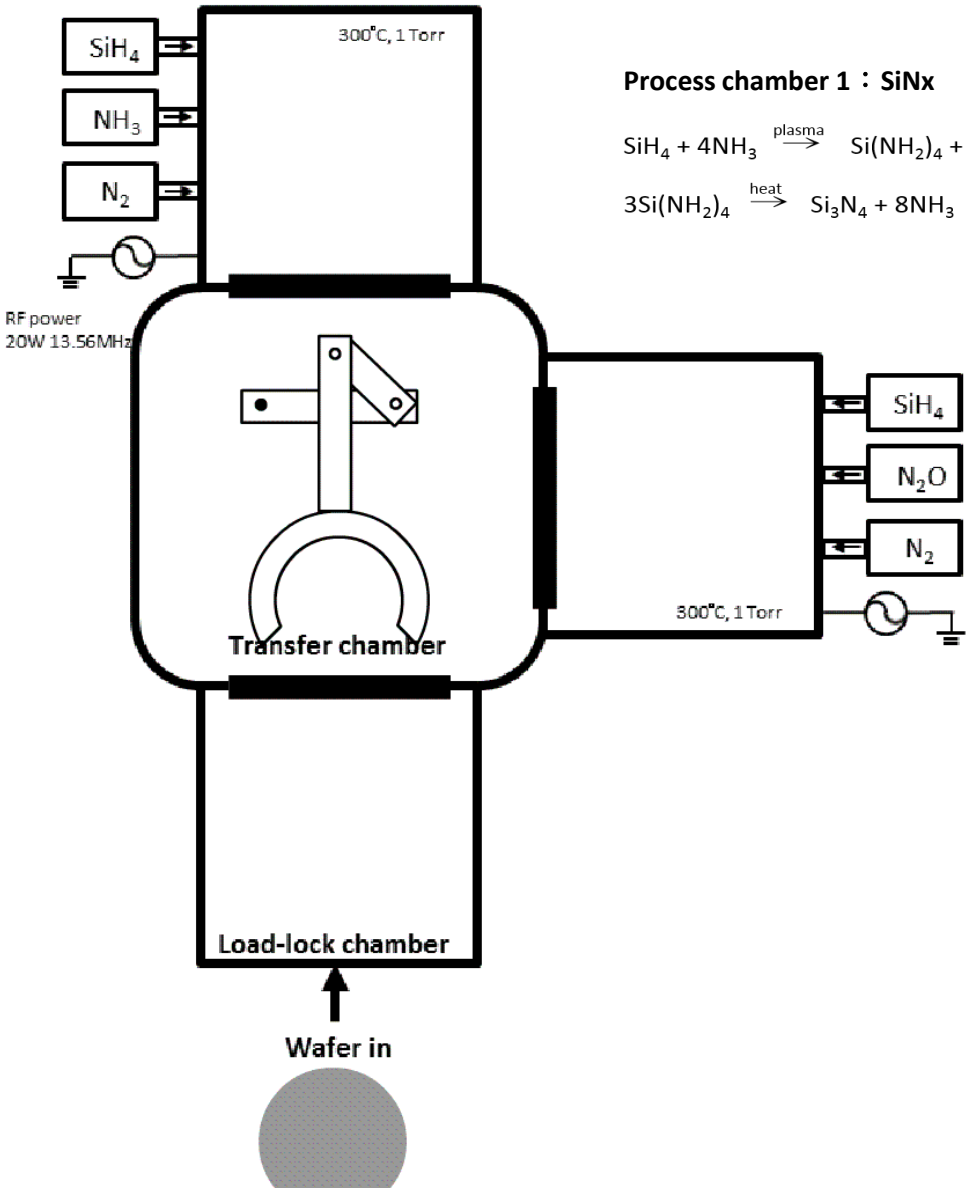
Process chamber 2 : SiO_2

$SiH_4 + 2N_2O \rightarrow SiO_2 + 2N_2 + 2H_2$



Silicon substrate side view

Plasma Enhanced Chemical Vapor Deposition (PECVD) for multi-layer dielectric mirror coating



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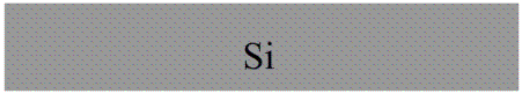
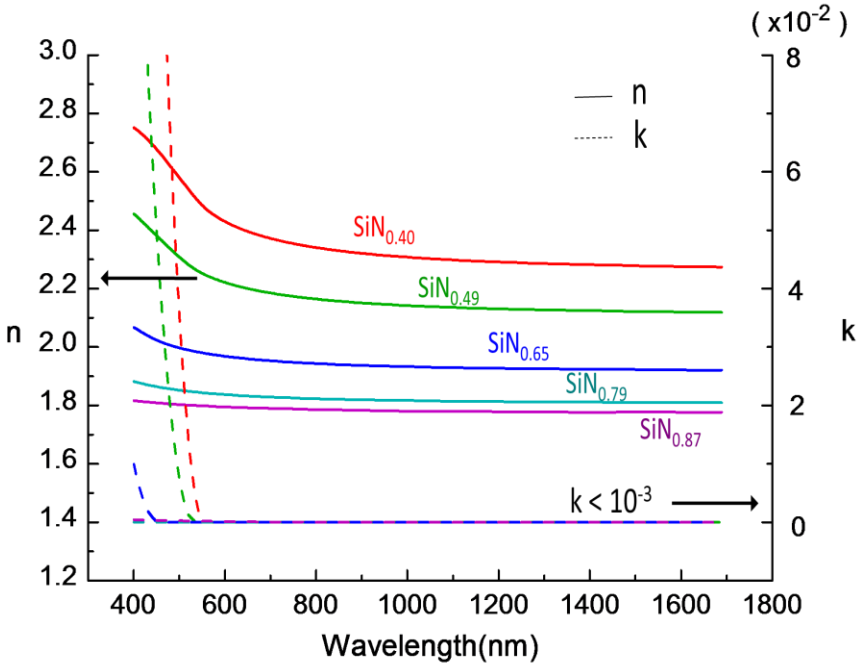
Process chamber 2 : SiO_2

$SiH_4 + 2N_2O \longrightarrow SiO_2 + 2N_2 + 2H_2$

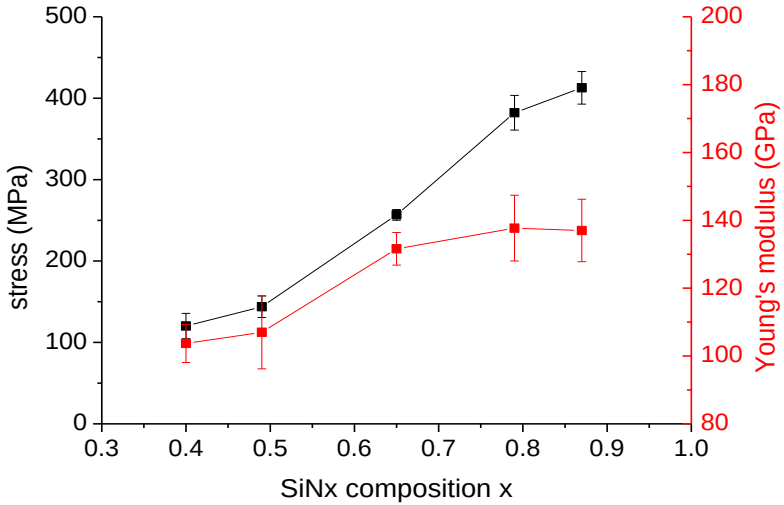


Silicon substrate side view

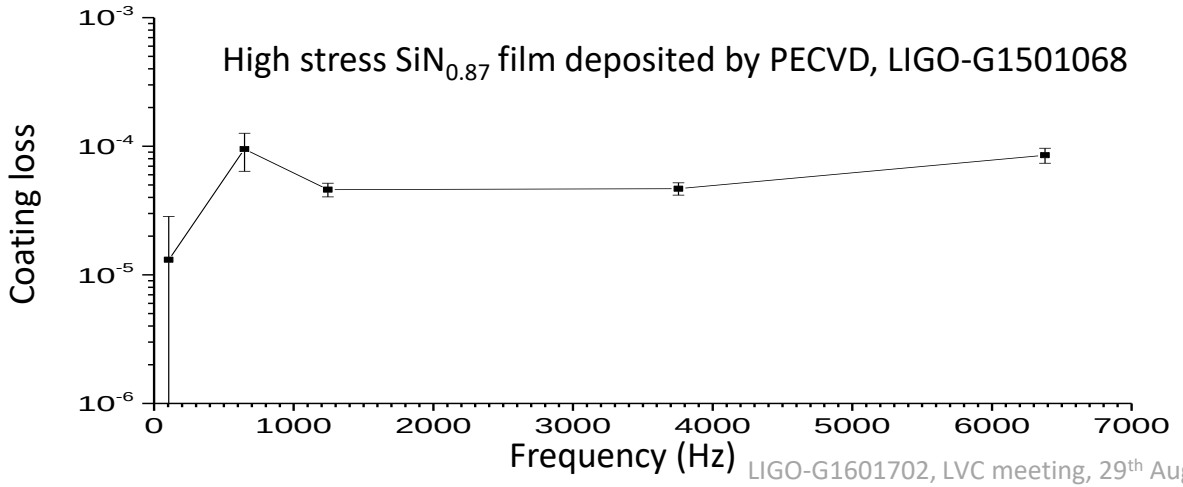
What We Had Last Year for SiNx



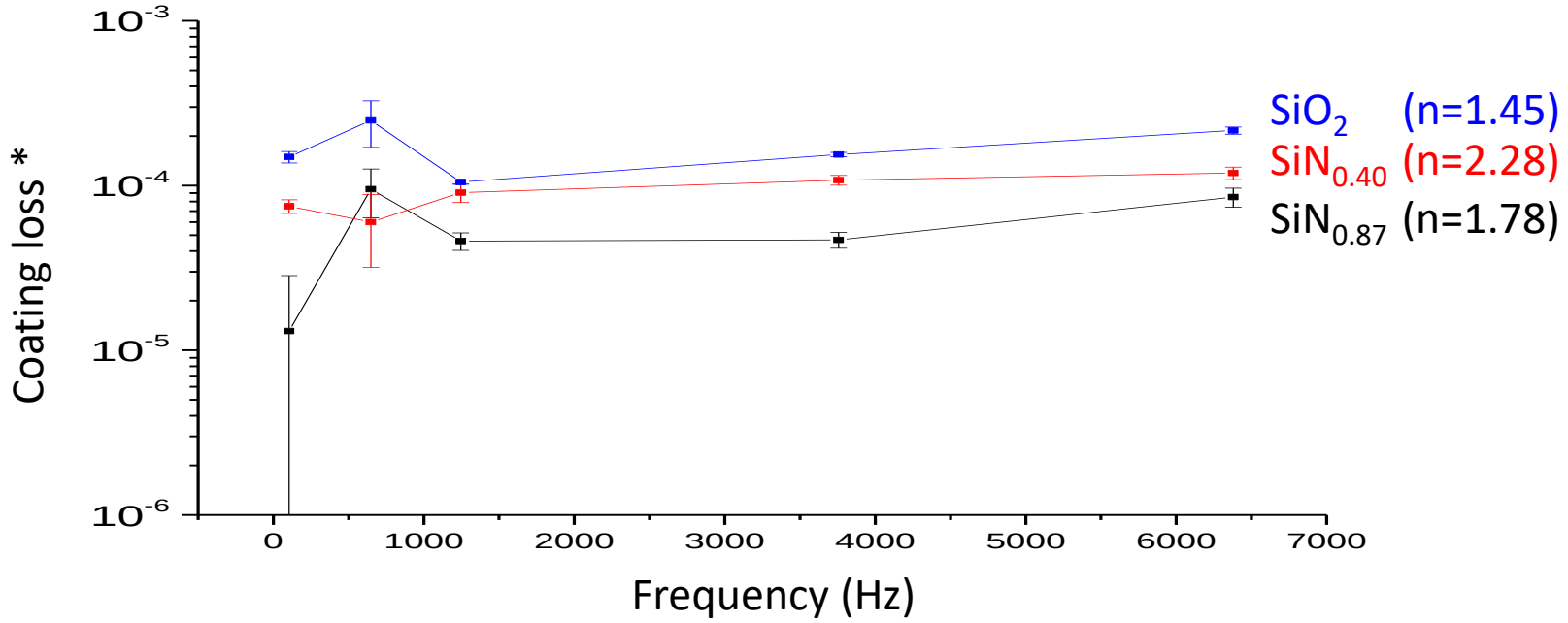
Refractive index and extinction coefficient



Stress and Young's modulus



Coating Loss for PECVD SiO_2, $SiN_{0.40}$ and $SiN_{0.87}$



We chose SiO_2 as the low index layer and $SiN_{0.40}$ as the high index layer for quarter-wave (QW) stacks.

* First two modes are bending modes and others are torsional modes. Higher order bending modes are not shown due to high fluctuation in the clamp loss.

$SiN_{0.4}/SiO_2$ QW Stacks

$SiN_{0.40}$ (n= 2.28)

tensile stress +120MPa

SiO_2 (n=1.45)

compressive stress -150MPa

Stresses are compensated

1-pair $SiN_{0.40}/SiO_2$ QW stack

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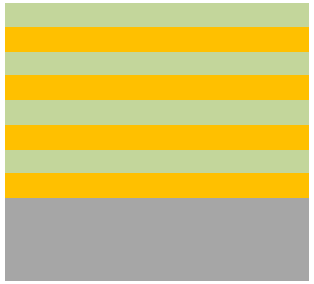


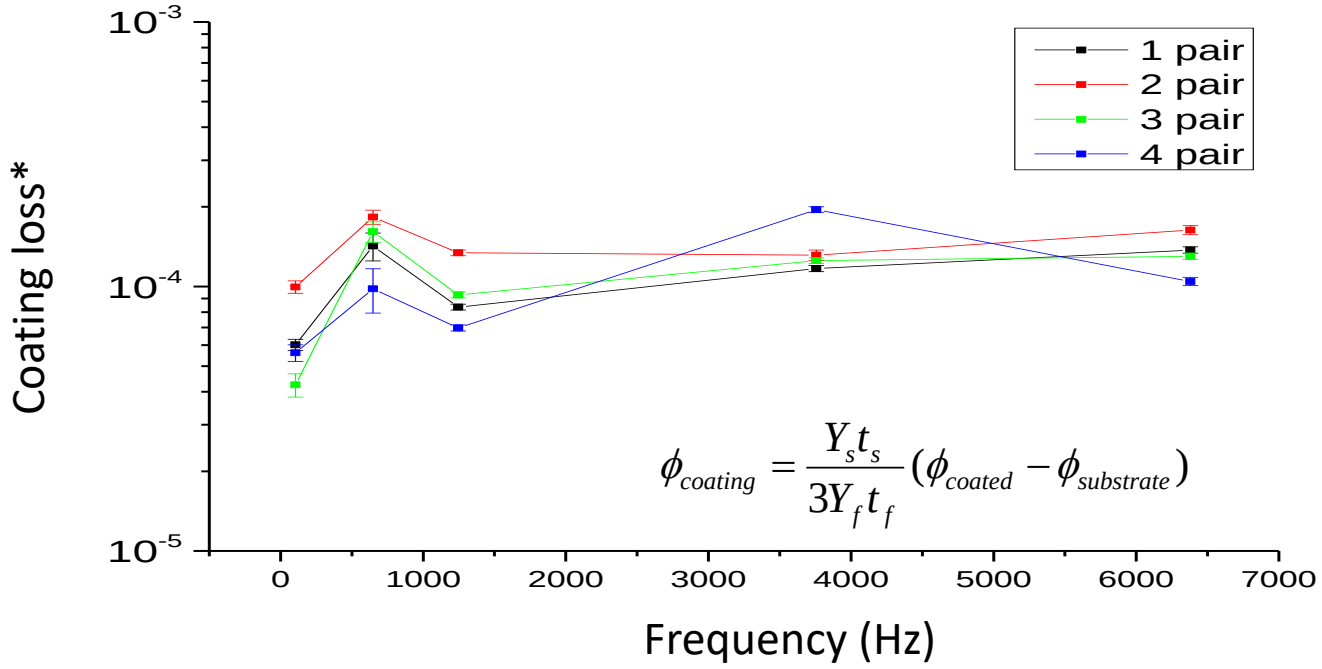
4-pair $SiN_{0.40}/SiO_2$ QW stack

material*	Refractive index# @1550nm	Young's modulus (GPa)	Stress (MPa)	Loss angle ~100Hz @ RT
SiO_2	1.45±0.01	83.8±1.3	-158.2±6.0	(1.49±0.12) x10^{-4}
$SiN_{0.40}$	2.28±0.01	103.7±5.6	120.2±15.5	(7.49±0.72) x10^{-5}

***All films are amorphous structure as deposited**

We have deposited samples with 1, 2, 3 and 4 pairs QW stacks.

Coating Loss of $SiN_{0.40}/SiO_2$ QW Stacks Deposited by PECVD



1. The coating losses of 1-4 pair are in 10^{-5} order at 100 Hz.
2. The coating loss does not increase with pair number, indicating that there is no significant loss in $SiN_{0.40}/SiO_2$ interface.

* First two modes are bending modes and others are torsional modes. Higher order bending modes are not shown due to high fluctuation in the clamp loss.

Conclusion

- Dual-reactor CVD in conventional silicon-IC process can be used for large area HR optical coatings.

- $SiN_{0.40}/SiO_2$ QW pairs deposited by all-CVD process showed room temperature mechanical loss in 10^{-5} at 100 Hz, lower than Ta_2O_5-TiO_2/SiO_2 in current GW detector.

- The coating loss of $SiN_{0.40}/SiO_2$ QW stack does not increase with pair number, indicating that there is no significant loss in $SiN_{0.40}/SiO_2$ interface.

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Thank You For Your Attention