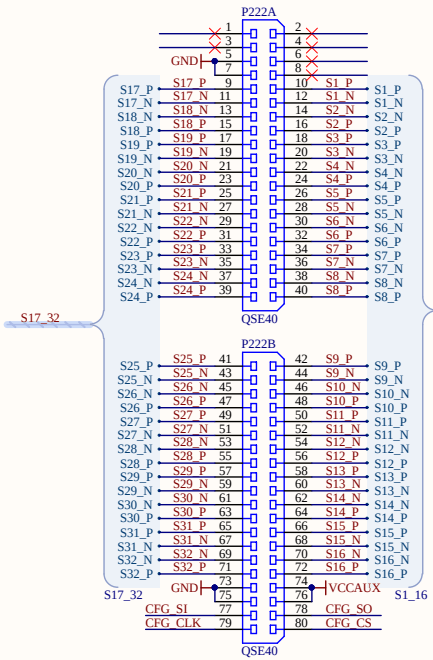
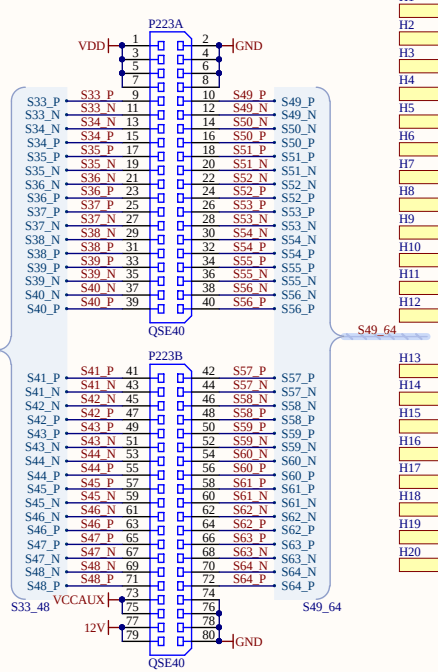
Power Chassis Timing Interface





FPGA
ChassisTimingInterface5.SchDoc

CFG_CLK, CFG_CS, CFG_SI, CFG_SO, CFG_WP
OSCCLK_N, OSCCLK_P, SYNCIN_N, SYNCIN_P, SYNCOUT_N, SYNCOUT_P, CNTROUT_N, CNTROUT_P, SYNC_N, SYNC_P, LED, LOS
PWRSYNC_N, PWRSYNC_P, SYNCLK_N, SYNCLK_P
ACLK_P, ACLK_N, ACNV_P, ACNV_N, AIN_P, AIN_N

DONE, PROG_B, TCK, TDI_B, TDO, TMS, CCLK, D_IN, HSWAP, INIT_B, M0, M1, M2
STCK, STDI, STDO, STMS, SW[10..1], FAIL
S1_16, S17_32, S33_48, S49_64

R1
1.00K
TDI_A

PWR
ChassisTimingInterface4.SchDoc
PWRSYNC_P, PWRSYNC_N
PWR_GOOD

FIB
ChassisTimingInterface2.SchDoc
CNTROUT_P, CNTROUT_N, SYNC_P, SYNC_N, LED
LOS, OSCCLK_P, OSCCLK_N, ACLK_P, ACLK_N, ACNV_P, ACNV_N, AIN_P, AIN_N
M_AIN_P, M_AIN_N, S_AIN_P, S_AIN_N
M_SYNC_P, M_SYNC_N, S_SYNC_P, S_SYNC_N

1PPS_TIMING
ChassisTimingInterface7.SchDoc

CONTEC
ChassisTimingInterface8.SchDoc

Designator
PCI Express_16765X11115_36PIN_Half length.schdoc

DUOTONE
ChassisTimingInterface6.SchDoc
SYNC_P, SYNC_N, SCLK_P, SCLK_N, DIN0_P, DIN0_N, DIN1_P, DIN1_N, DTCLK0_P, DTCLK0_N, DTCLK1_P, DTCLK1_N, INVS_P, INVS_N
DUOTONE0, DUOTONE1, CLOCK_DUOTONE_0, CLOCK_DUOTONE_1

U2A, U2B
TCK_B, TMS_B

PRG
ChassisTimingInterface3.SchDoc
TCK, TDI_A, TDO, TMS, STCK, STDI, STDO, STMS, SW[8..1]
DONE, PROG_B, CCLK, D_IN, HSWAP, INIT_B, M0, M1, M2

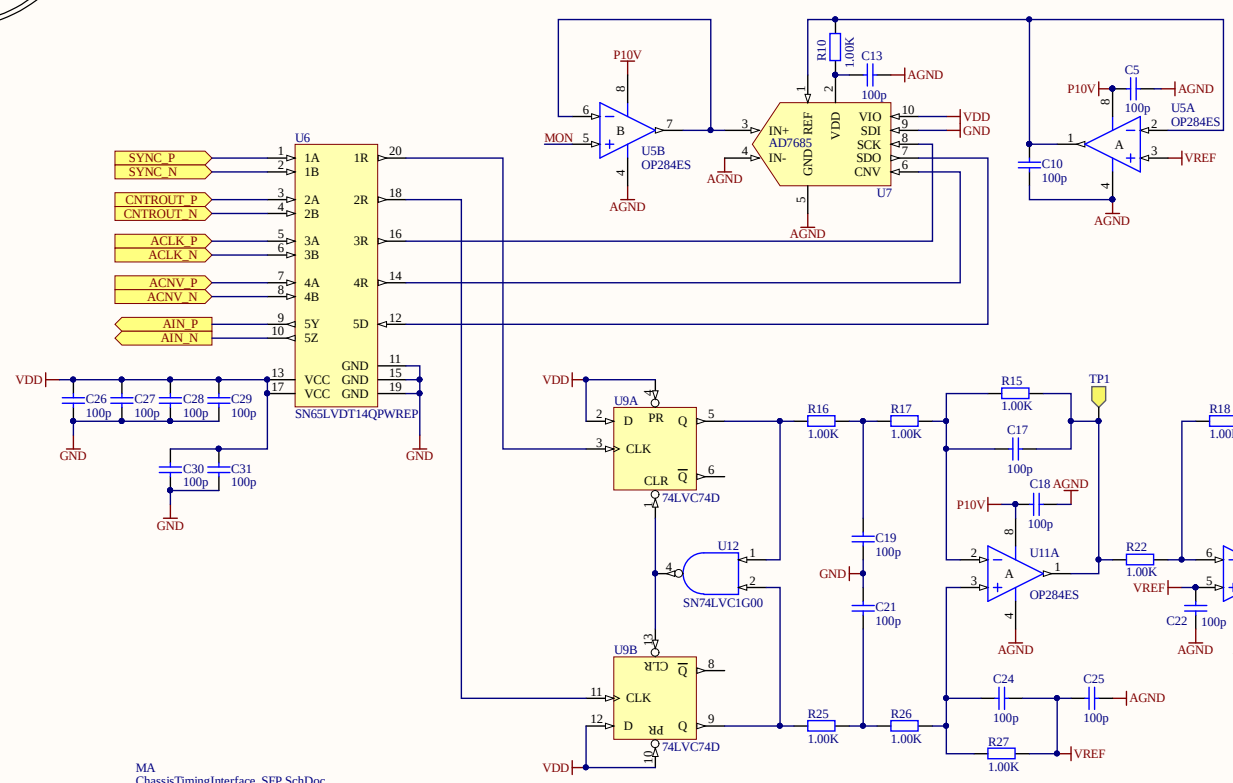
C1
100p
VCCAUX, GND
VDD

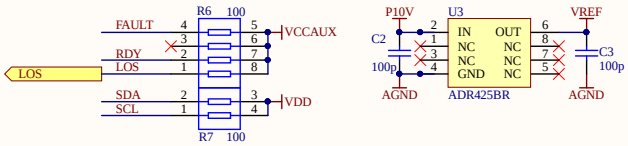
H1 Additional part number
H2 Additional part number
H3 Additional part number
H4 Additional part number
H5 Additional part number
H6 Additional part number
H7 Additional part number
H8 Additional part number
H9 Additional part number
H10 Additional part number
H11 Additional part number
H12 Additional part number
H13 Additional part number
H14 Additional part number
H15 Additional part number
H16 Additional part number
H17 Additional part number
H18 Additional part number
H19 Additional part number
H20 Additional part number

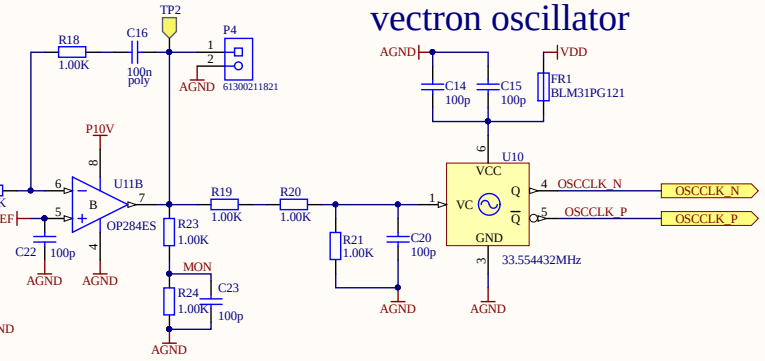
Project	*PCIe Timing Slave*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Timing Interface*		
Size: B-C-D	DCC D070071	Rev: D	
Date: 4/10/2020	Time: 12:32:01 PM	Sheet: 1 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface1.SchDoc			

VCO & Phase Detector

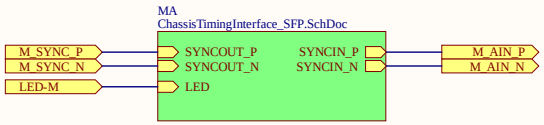
quiet noise for phase detector 10v agnd

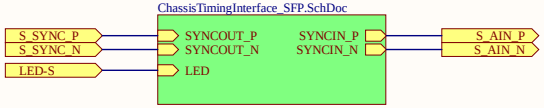


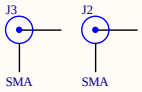




vectron oscillator

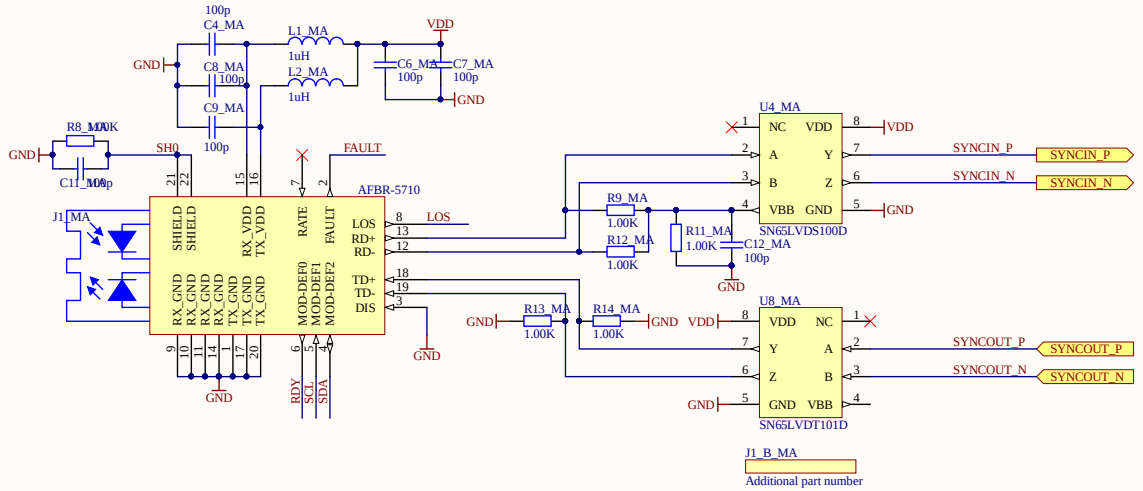






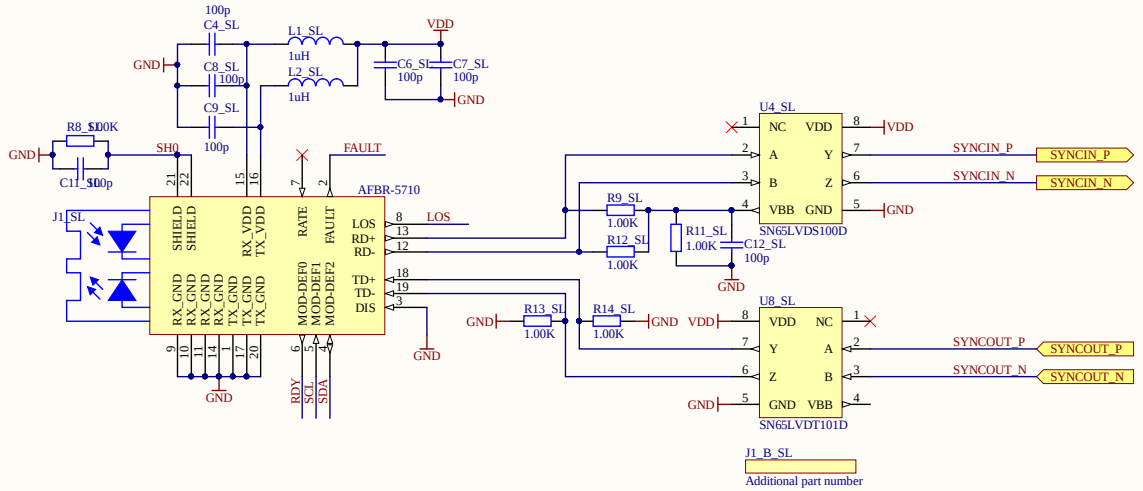
Project	*PCIe Timing Slave*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*VCO & Phase Detector*		
Size: B-C-D	DCC D070071	Rev: D	
Date: 4/10/2020	Time: 12:32:02 PM	Sheet: 2 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface2.SchDoc			

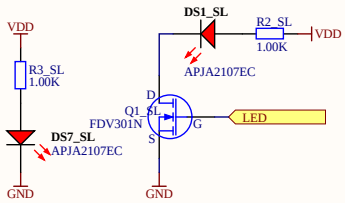
SFP



Project	*PCIe Timing Slave*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*SFP*		
Size: B-C-D	DCC D070071	Rev: D	
Date: 4/10/2020	Time: 12:32:02 PM	Sheet: 3 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface_SFP.SchDoc			

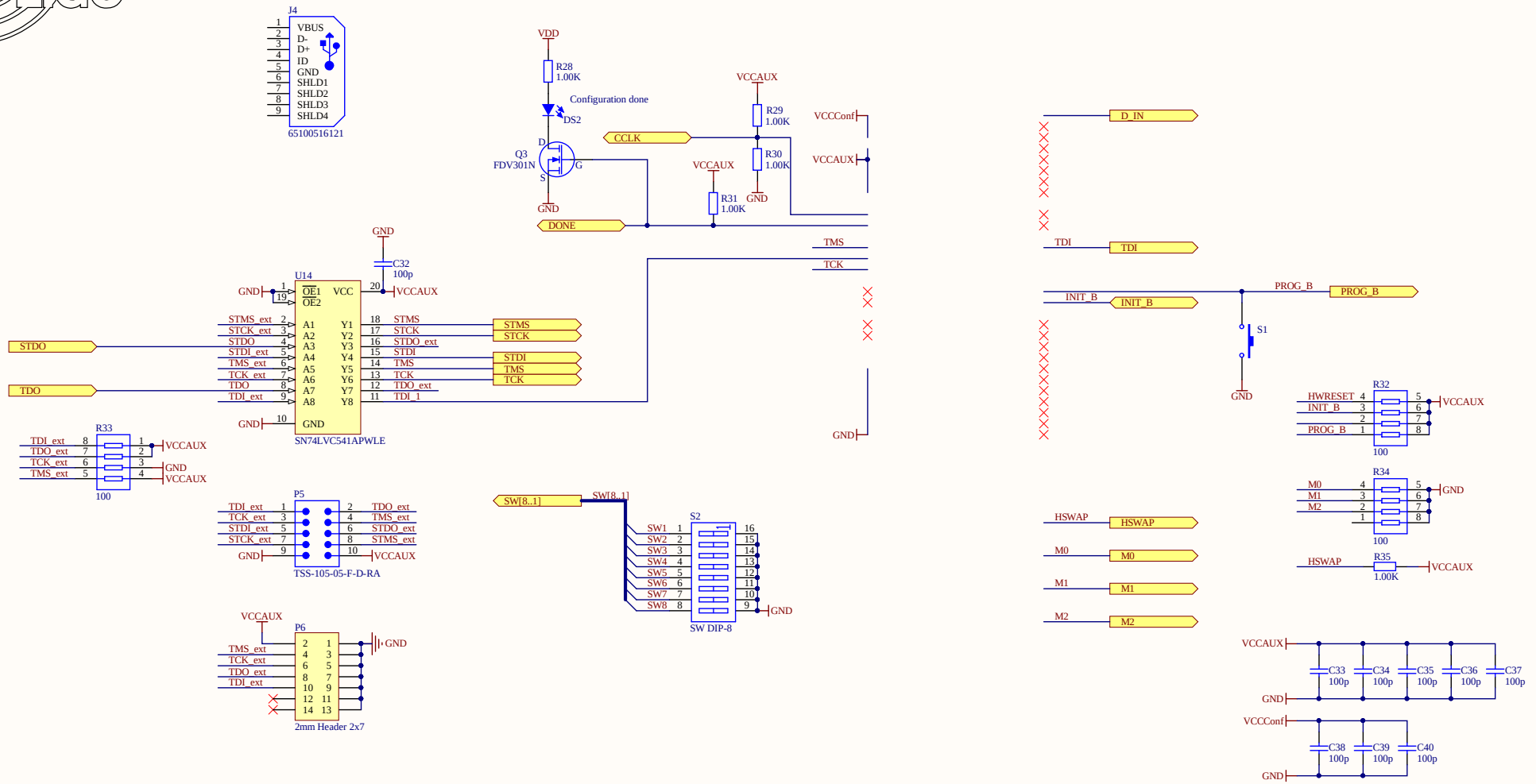
SFP





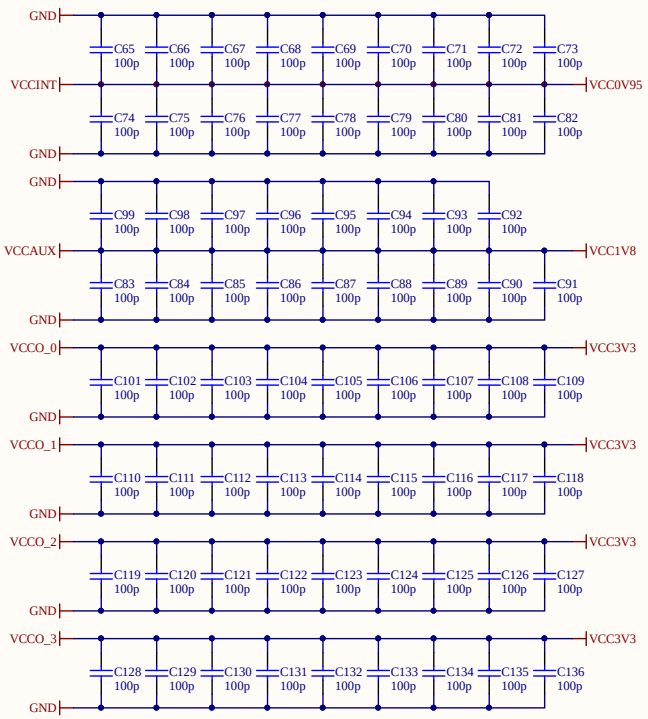
Project	*PCIe Timing Slave*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*SFP*		
Size: B-C-D	DCC D070071	Rev: D	
Date: 4/10/2020	Time: 12:32:03 PM	Sheet: 3 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface_SFP.SchDoc			

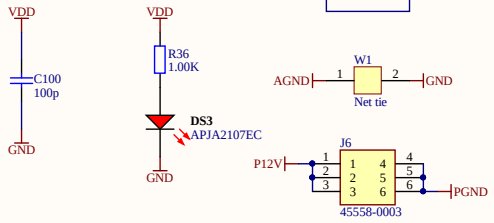
JTAG and SPI Flash

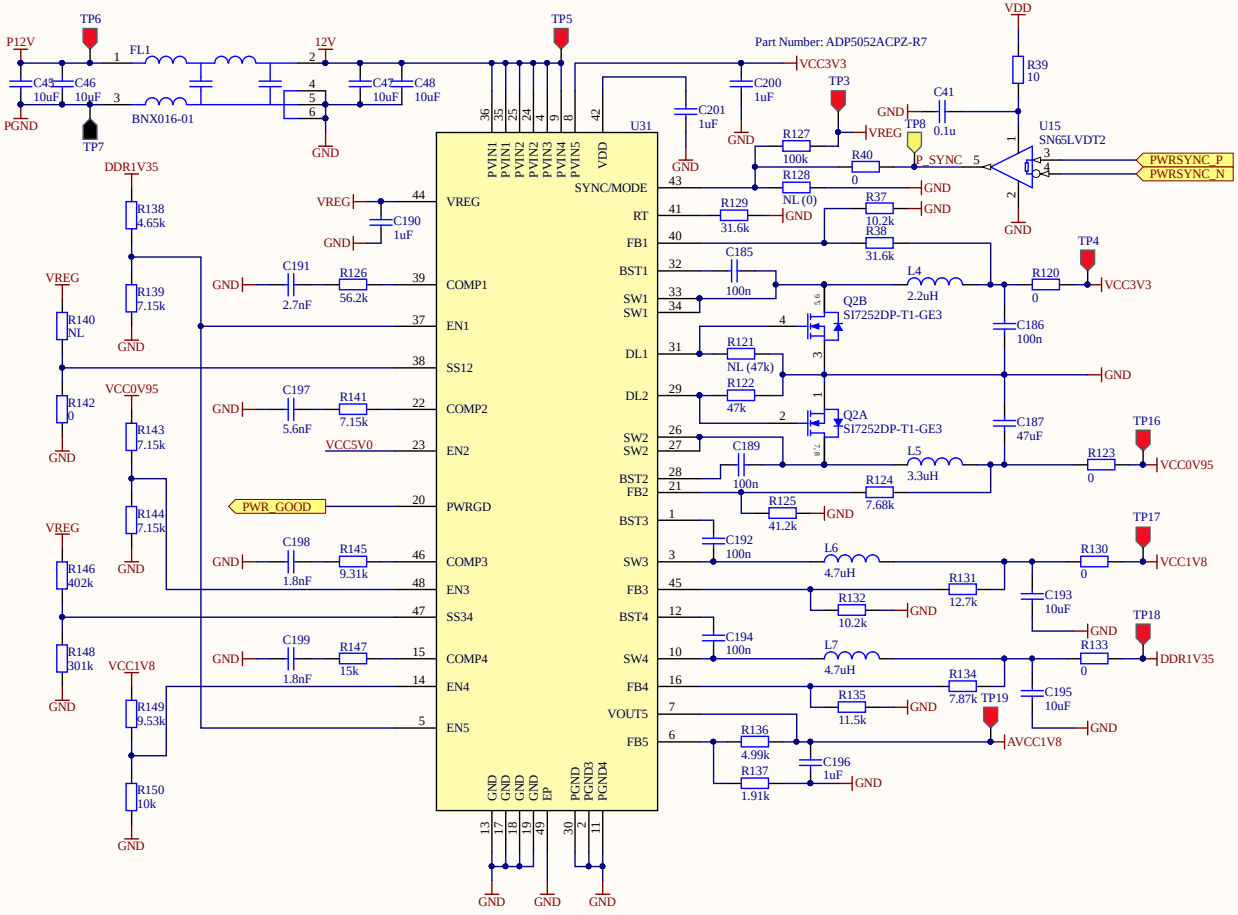


Project	*PCIe Timing Slave*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*JTAG & SPI Flash*		
Size: B-C-D	DCC D070071	Rev: D	
Date: 4/10/2020	Time: 12:32:04 PM	Sheet: 4 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface3.SchDoc			

Power Systems

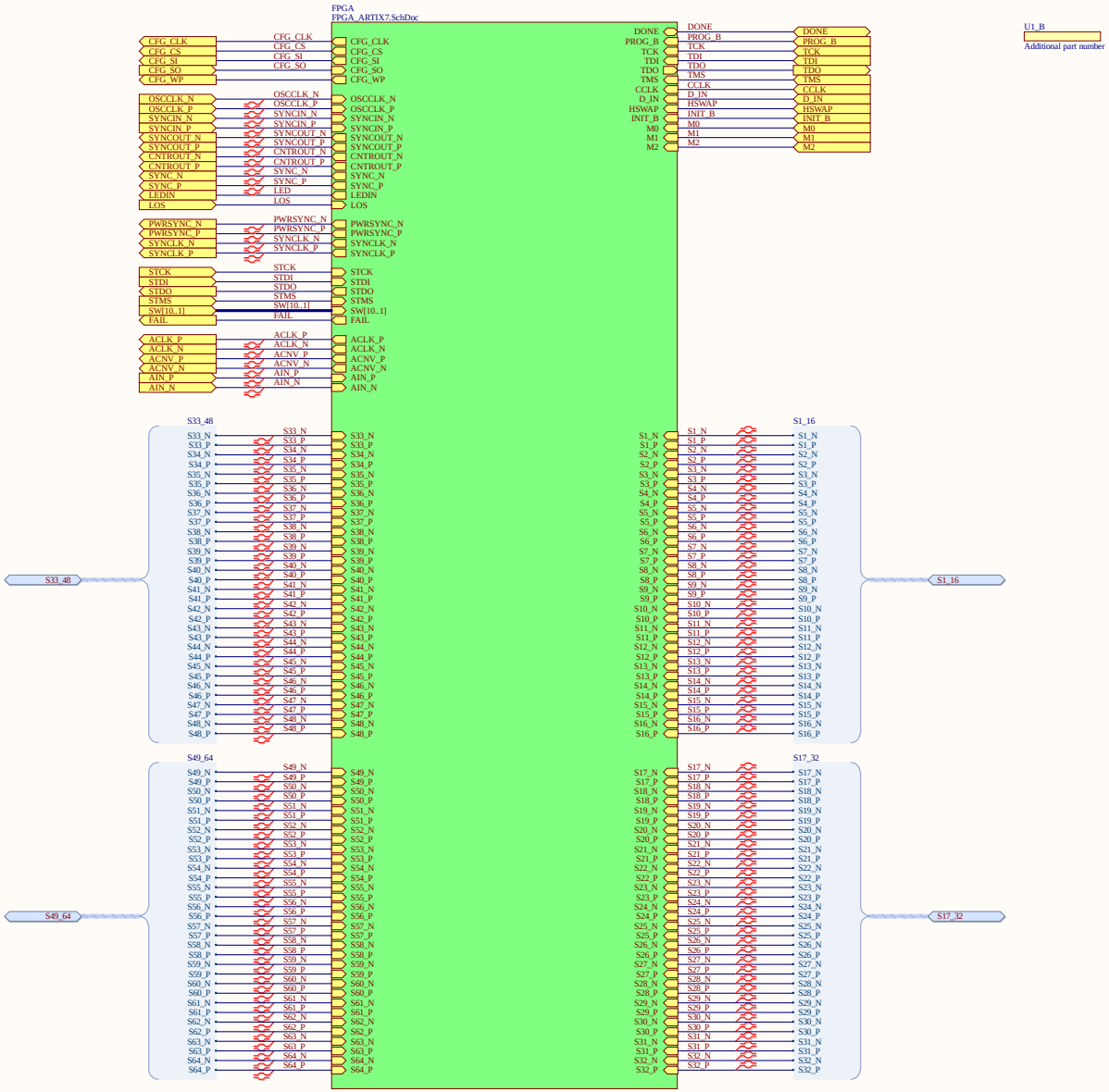




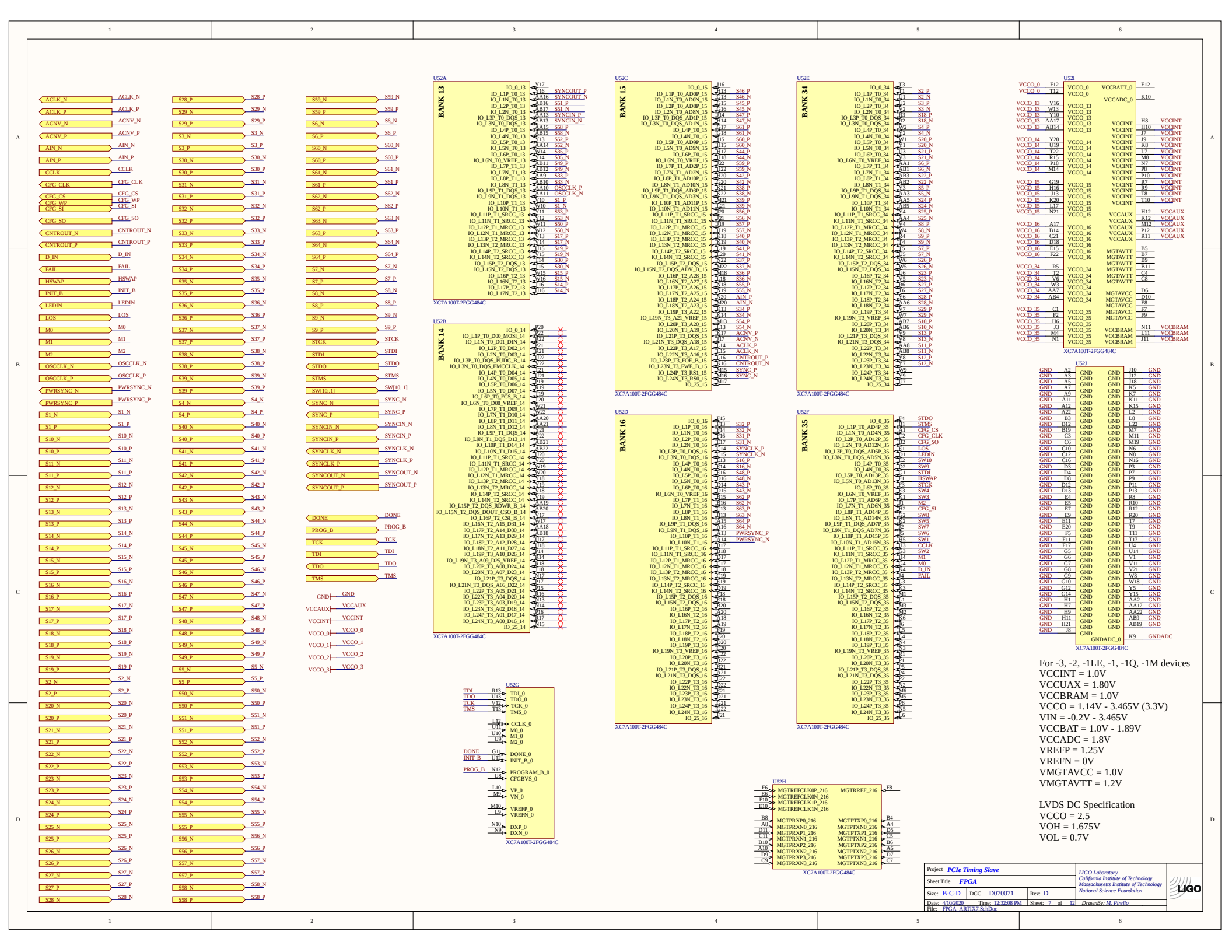


Project	*PCIe Timing Slave*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Power Supply*		
Size: B-C-D	DCC D070071	Rev: D	
Date: 4/10/2020	Time: 12:32:06 PM	Sheet: 5 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface4.SchDoc			

FPGA Interface



Project	*PCIe Timing Slave*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*FPGA Interface*		
Size: B-C-D	DCC D070071	Rev: D	
Date: 4/10/2020	Time: 12:32:07 PM	Sheet: 6 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface5.SchDoc			


ACLK_N
ACLK_P
ACNV_N
ACNV_P
AIN_N
AIN_P
CCLK
CFG_CLK
CFG_CS
CFG_WP
CFG_SI
CFG_SO
CNTROUT_N
CNTROUT_P
D_IN
FAIL
HSWAP
INIT_B
LEDIN
LOS
M0
M1
M2
OSCCLK_N
OSCCLK_P
PWRSYNC_N
PWRSYNC_P
S1_N
S1_P
S10_N
S10_P
S11_N
S11_P
S12_N
S12_P
S13_N
S13_P
S14_N
S14_P
S15_N
S15_P
S16_N
S16_P
S17_N
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S19_N
S19_P
S2_N
S2_P
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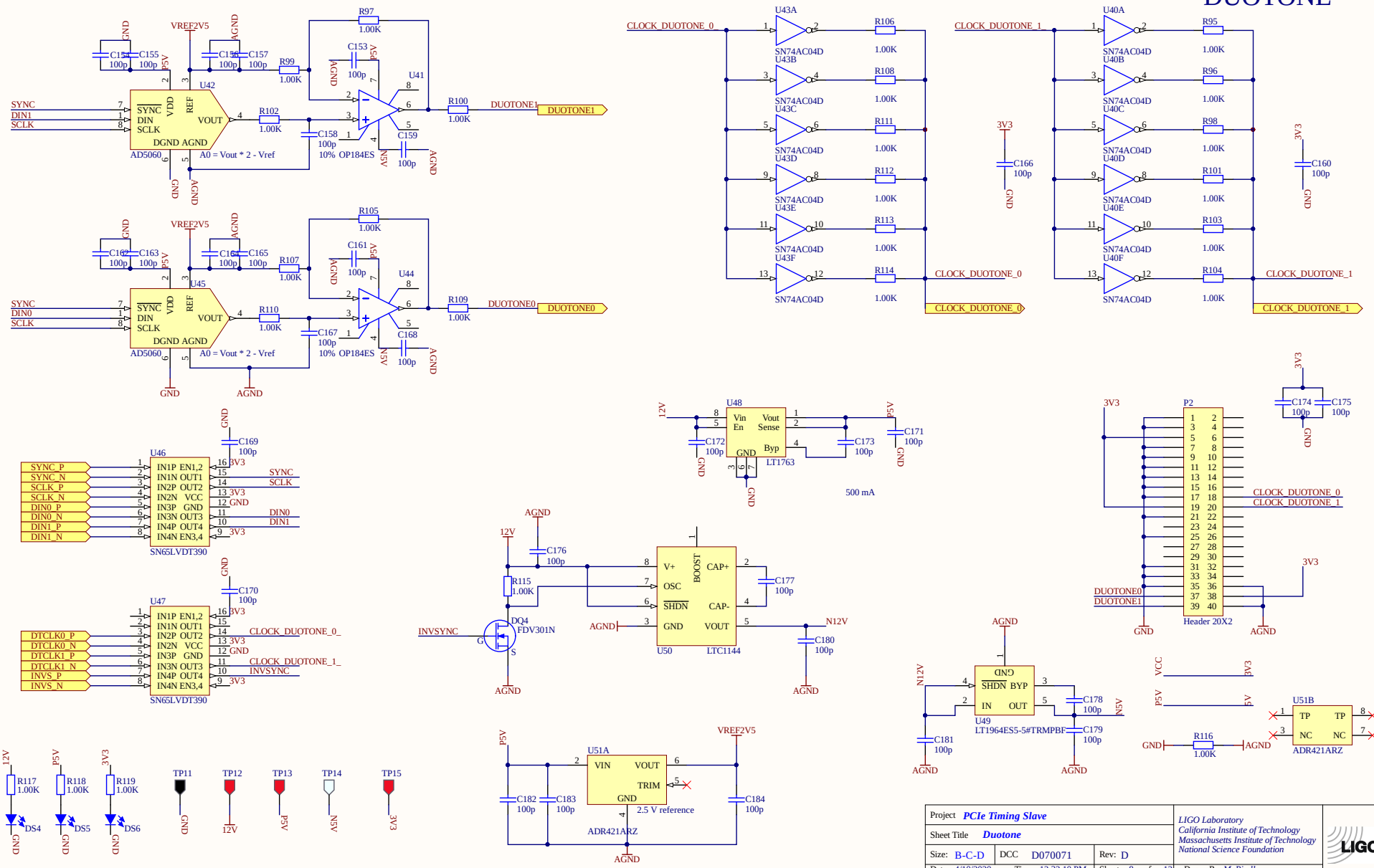
S64_P
S7_N
S7_P
S8_N
S8_P
S9_N
S9_P
STCK
STDI
STDO
STMS
SW[10..1]
SYNC_N
SYNC_P
SYNCIN_N
SYNCIN_P
SYNCLK_N
SYNCLK_P
SYNCOUT_N
SYNCOUT_P
DONE
PROG_B
TCK
TDI
TDO
TMS
GND
VCCAUX
VCCINT
VCCO_0
VCCO_1
VCCO_2
VCCO_3
U52A
BANK 13
XC7A100T-2FGG484C
U52B
BANK 14
XC7A100T-2FGG484C
U52C
BANK 15
XC7A100T-2FGG484C
U52D
BANK 16
XC7A100T-2FGG484C
U52E
BANK 34
XC7A100T-2FGG484C
U52F
BANK 35
XC7A100T-2FGG484C
U52G
XC7A100T-2FGG484C
U52H
XC7A100T-2FGG484C
U52I
XC7A100T-2FGG484C
U52J
XC7A100T-2FGG484C
For -3, -2, -1LE, -1, -1Q, -1M devices
VCCINT = 1.0V
VCCUAX = 1.80V
VCCBRAM = 1.0V
VCCO = 1.14V - 3.465V (3.3V)
VIN = -0.2V - 3.465V
VCCBAT = 1.0V - 1.89V
VCCADC = 1.8V
VREFP = 1.25V
VREFN = 0V
VMGTAVCC = 1.0V
VMGTAVTT = 1.2V
LVDS DC Specification
VCCO = 2.5
VOH = 1.675V
VOL = 0.7V
Project PCIe Timing Slave
Sheet Title FPGA
Size: B-C-D
DCC D070071
Rev: D
Date: 4/10/2020
Time: 12:32:08 PM
Sheet: 7 of 12
File: FPGA_ARTIX7.SchDoc
DrawnBy: M. Pirello
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
LIGO

DUOTONE

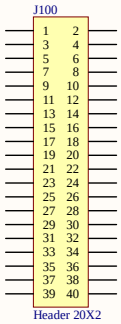


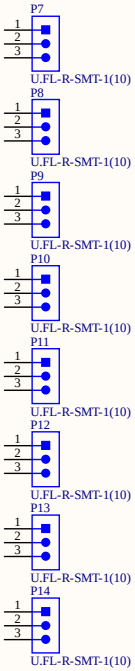
Project	*PCIe Timing Slave*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Duotone*		
Size: B-C-D	DCC D070071	Rev: D	
Date: 4/10/2020	Time: 12:32:10 PM	Sheet: 8 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface6.SchDoc			

1PPS TIMING

Project	***PCIe Timing Slave***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***1PPS Timing***		
Size: B-C-D	DCC D070071	Rev: D	
Date: 4/10/2020 Time: 12:32:10 PM		Sheet: 9 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface7.SchDoc			

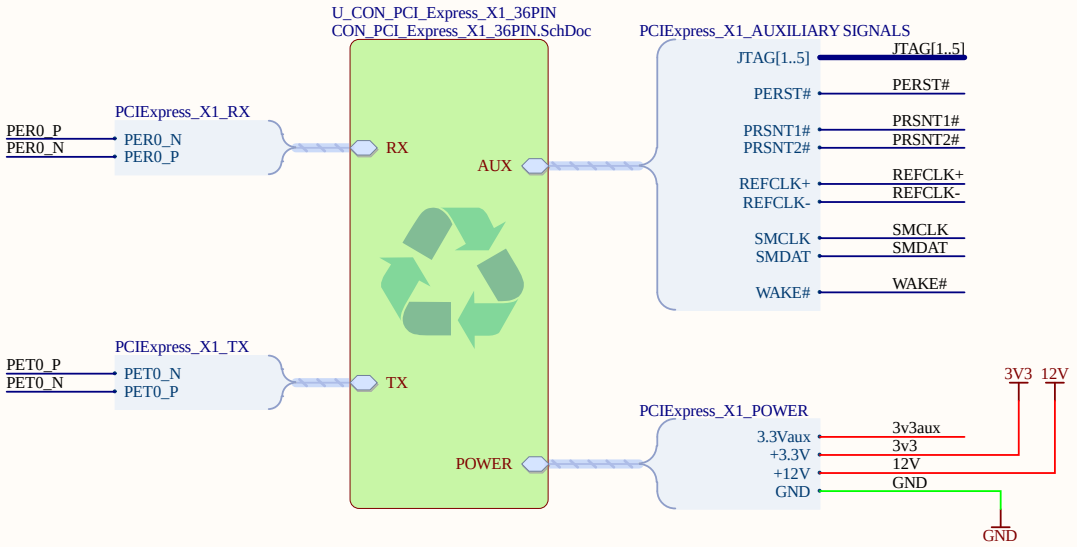
CONTEC & TIMING





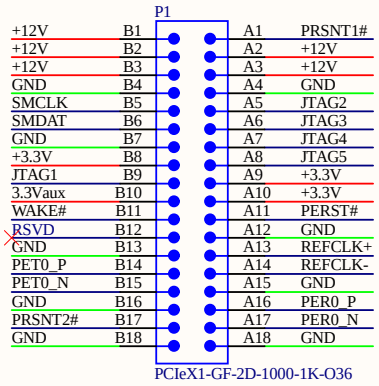
CONTEC TO DO LIST
Investigate timing voltage requirements and locations on the 40 pin header.
Apply new signals to the 40 pin header, and the UMCC connectors.

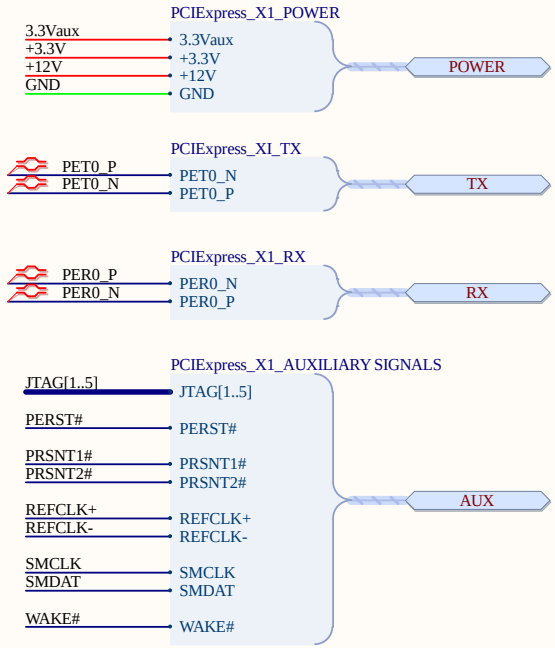
Project	***PCIe Timing Slave***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***CONTEC & Timing***		
Size: B-C-D	DCC D070071	Rev: D	
Date: 4/10/2020 Time: 12:32:10 PM	Sheet: 10 of 12	*DrawnBy: M. Pirello*	
File: ChassisTimingInterface8.SchDoc			



- Nominal values used, dimensions in mm
- The mounting holes and keep-out areas around them are only required when the I/O bracket is mounted on the card directly
- Component height rule and clearance rule derived from PCI_Express_CEM_r2.0.pdf, Page 84.
- Stackup is not specified in PCI_Express_CEM_r2.0.pdf, nor implemented in this template.

Project	***PCIe Timing Slave***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***PCIe Interface***		
Size: B-C-D	DCC D070071	Rev: D	
Date: 4/10/2020	Time: 12:32:10 PM	Sheet: 11 of 12	*DrawnBy: M. Pirello*
File: PCI Express_16765X11115_36PIN_Half length.schdoc			





Title *			*
Size: A4	Number:*	Revision:*	*
Date: 4/10/2020	Time: 12:32:10 PM	Sheet * of *	*
File: C:\Users\marc.pirello\Altium\Solutions\ISC - PCIe Duotone\PCIe_ChassisTimingInterface\Managed\Sheets\02F33160-28A9-45			