Title	*Filter Cavity Receiver Chassis Design Note for A+*
Author	*R. Abbott, Caltech*
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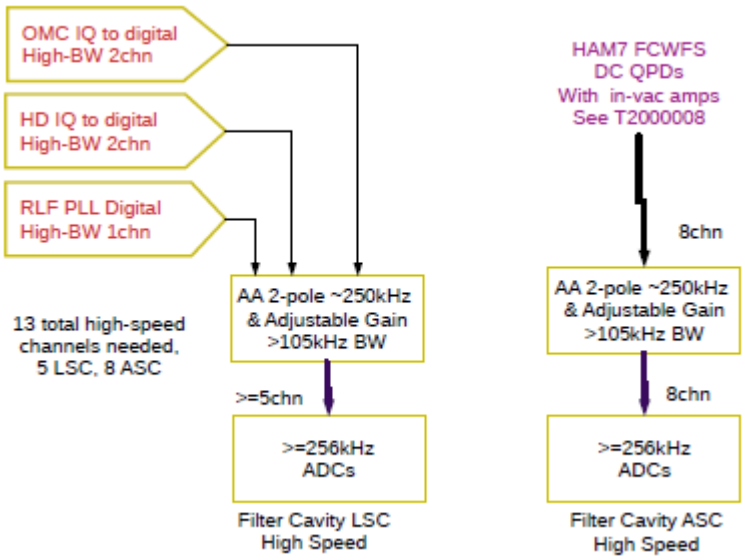
1. Overview

The A+ filter cavity has a number of signals at 105kHz that are required to be digitized by new 16-channel high-speed ADCs (General Standards Corp PN-PCIe66-18AI32SSC1M-16). A snip of E1900201-v5 is shown below along with 13 analog inputs. A new chassis design is envisioned that collects and processes 105kHz signals associated with the A+ Filter Cavity controls. Functions to be provided include Anti-aliasing, fixed gain, and provisions for easy connections to remote signal sources.

A 1U chassis with the above-mentioned functions will be designed and built from the requirements of this document.

Figure 1, snip from E1900201 showing 13 signals to be digitized with a high-speed ADC.



2. Chassis Signal Functional Description

The signal functions and attributes associated with the connectors carrying signals into and out of the chassis shown in Figure 1 are provided in the table below.

Table 1 Signal Descriptions.

Signal Name	Chan. Count	Required Chassis Connector	Front or Rear Input or Output	Description
OMC IQ	2	TNC (x2)	Front/Input	I&Q demodulated signals at 105kHz with a DC component from LSB demodulation of 3.125MHz SSB carrier. Provides information on Filter Cavity length
HD IQ	2	TNC (x2)	Front/Input	This signal originates from the Squeezer Homodyne detector. The 105kHz signal conveys information about the amount of squeezing when the IFO is unlocked.
RLF PLL	1	DB-9M	Front/Input	Resonant Locking Field. This ~105kHz signal is used to provide information about the squeezing angle rotation associated the squeezer output plus phase shift from the Filter Cavity. This RLF signal in conjunction with a VCO-PLL is used to set the angle associated with the frequency dependent squeezing.
Spare Inputs	3	DB-9M	Front/Input	Only 13 of 16 channels are used. This connector gives access to the 3 remaining channels.
HAM7 FC WFS	4 per D-25	DB-25M (x2)	Front/Input	These eight signals are the quadrant outputs plus DC Signals from two in-vacuum QPDs associated with the Filter Cavity alignment and length control. The length control aspect is redundant with that provided by the OMC IQ as mentioned above.
QPD DC Out	8	DB-25F	Rear/Output	Eight differential DC signals to be transmitted to a Beckhoff ADC
QPD AC Out	16	DB-37F	Rear/Output	16 differential AC signals to be transmitted to a high-speed General Standards 18-bit ADC

3. Chassis Circuit Functional Description

Figure 2, individual gain may vary from one channel to another.

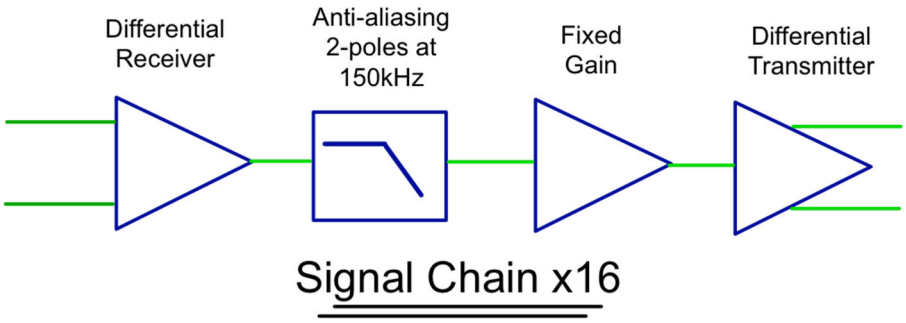
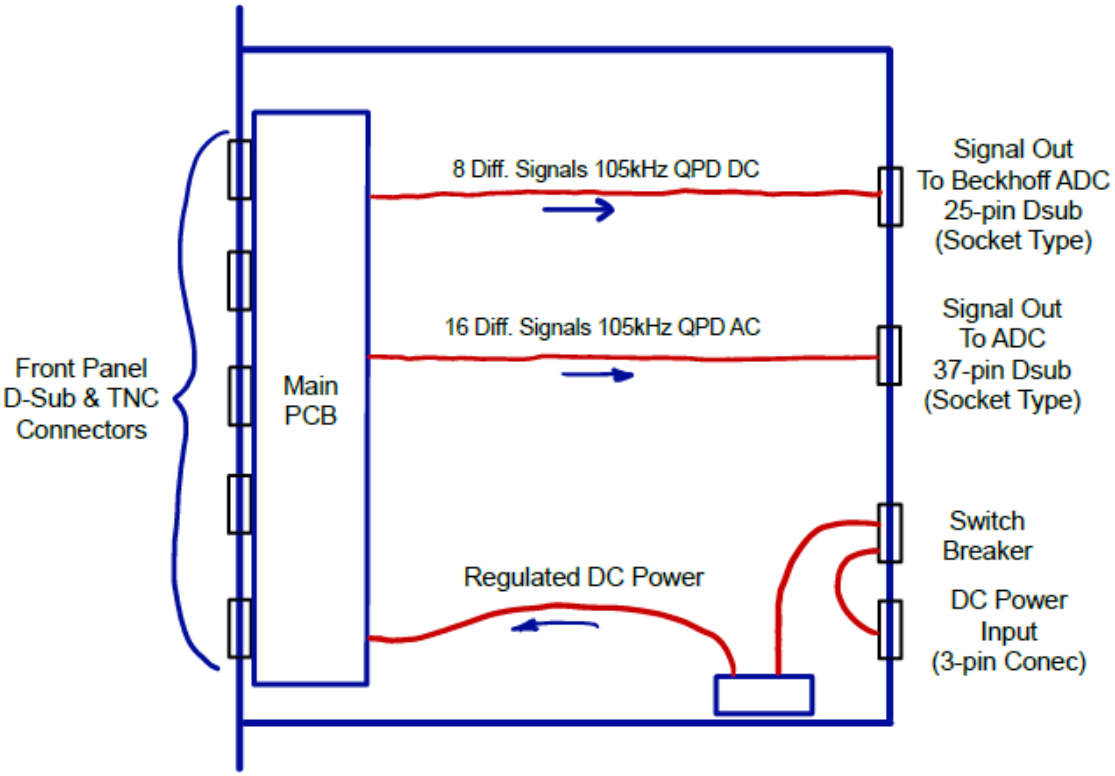


Figure 3, Front-panel connectors are a mixture of TNC and Dsub. Voltage regulator may be incorporated onto the main PCB for convenience if it makes sense from a thermal standpoint.



a. Anti-aliasing

A notional anti-aliasing circuit function for all 16 ADC channels will be provided consisting of a unity-gain active filter with two poles at 150kHz.

b. Signal Conditioning and Concentration

The signals entering this chassis are ultimately combined into a single 37-pin output connector (D-sub 37 pin, socket type) to finish the connection to the ADC. As the ADC has 16 channels, there will be 3 channels left unused. The plan is to make these three channels available in the form of a 9-pin D-sub (pin-type) input.

Each of the 16 channels will also have provisions for allocation of fixed gain prior to differential transmission to the remotely located ADC. As can be seen in the following section on *noise*, the gain will need to be set based on actual measured signal levels, but factors ranging from 1 to 10 are likely. Care must be given to slew-rate and bandwidth such that the 105kHz signals are treated appropriately.

4. Auxiliary functions

a. Chassis must supply electronically fused DC power to the in-vacuum QPD heads via the associated two 25-pin Dsub connectors on the front panel. Loss of one polarity must kill the other polarity.
b. A single switch on the front panel to turn on and off the power to the in-vacuum QPD heads (QPD needs +/-18VDC)
c. LED power indications (Green LEDs):
    i. Front Panel Green LED: +/-15VDC from internal chassis regulator.
    ii. Front Panel Green LED: QPD Head Power. Lit if both power sources to QPD heads are OK, AND the fuse is not blown. Serves as blown fuse indicator if the fuse is blown.
    iii. Front Panel Red LED: Fuse status. Lit if overcurrent shutdown has occurred.
    iv. Rear Panel Green LED: Bulk power indicators indicating whether or not DC power is coming into the chassis from the external power source and tapped off after the rear panel on/off switch (lit when rear panel switch is ON).
d. A single DC switch/breaker on the rear panel to turn main power (+/-18VDC) on and off.

5. Dynamic Range

The high-speed ADC envisioned for this application has various configurable input-voltage dynamic range settings. In keeping with the existing ADC input dynamic range used elsewhere in the LIGO controls, the ADC (General Standards Corp PN-PCIe66-18AI32SSC1M-16) will be configured for +/-10V input range. This often-misunderstood input range specification can be viewed best by considering that a 20V battery can be connected across the input terminals of the ADC and will be measurable (common-mode voltage issues aside). Flipping the battery polarity will also be measurable implying that a full range of +20V to -20V (40Vp-p) can be measured. This voltage is divided into steps as dictated by the total number of bits used (the ADC in question can be configured for 16 or 18 bits).

6. Noise

A test was performed with the proposed ADC to measure the input referred noise. A 105kHz signal of several volts peak-to-peak was applied to the ADC and the resulting digitized noise was found to be ~10uVrms/√Hz close into the carrier and flat as observed for carrier offset frequencies of several kHz on either side of the 105kHz carrier.

By taking a ratio of the peak signal voltage to the spectrally flat measured noise, an angular jitter can be specified and compared to the maximum allowable angular noise. The maximum allowable noise is specified (email correspondence with Lee McCuller and Peter Fritschel) to be 1×10^{-5} rad/√Hz. Given this limit, and assuming a 5Vpk signal at 105kHz, the ratio of the 5Vpk signal to the 10uVrms/√Hz yields 2×10^{-6} rad/√Hz, which is well within the allowable range.

The noise analysis done for a 5Vpk signal does have a cautionary aspect though. If the 105kHz signal is 1Vpk or less, the alignment system will become noise limited due to ADC noise.

7. Packaging

The resulting chassis can be reasonably accommodated in a 1U, 19-inch rack-mounted chassis. The front panel would have the differential input signals from the field, and the rear panel will have a single 37-pin D-sub (socket type) as the interconnect to the remote ADC. Regulated DC power indication will be provided on the front panel, and an ON/OFF switch/breaker will be provided on the rear panel. Input power annunciation will also be present on the rear panel in the form of green LEDs.

A single PCB will be designed and mounted to the front panel. Ribbon cable will be used internal to the chassis to carry the signals out of the PCB to the rear panel connector. A LIGO standard wall mount