

LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

LIGO Laboratory / LIGO Scientific Collaboration

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Test Procedure for PCIe Timing Interface

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1 Introduction

The following Test Procedure describes the test of proper operation of the PCIe Timing Interface.

S/N	FPGA: XC7A	T

Tester _____

Date				

2 Test Equipment

- Voltmeter
- Oscilloscope
- RF frequency synthesizer
- Fiber from a Timing Master/Fanout,
- Windows PC with open motherboard with at least 1 PCIe slot free. Alternatively, use a PC with an PCIe extender like the Adnaco.
- Extra PC ATX power supply
- Adapter: Dual PSU power supply 24-pin adapter cable for ATX motherboard, and
- IDC-10 header test adapter, and
- D-Sub test adapters, see <u>D2100517</u>.
- Test daughter board, <u>D080192</u>.
- 2 test adapter board for backplane, <u>D2100184</u>.
- Breakout Boards DB37, DB25 if needed

3 Preparations

- PC needs to run Windows 10, 64-bit.
- Install Vivado 2020.1 or later.
- Download the FPGA test code, <u>E2100232</u>, and the production FPGA code, <u>E2000337</u>.
- Install the device driver for LIGO Timing.
- Install the LIGOTimingApp and LIGOTimingVerify programs.

4 Caution

When connecting test adapters, backplanes and daughter cards, it is important that the correct FPGA program is loaded. Otherwise, it is possible to short two outputs together which can potentially damage the board.

- Test adapters, <u>D2100517</u> and <u>D080192</u>, require the FPGA timing test code, <u>E2100232</u>, to be loaded.
- The backplane, <u>D20000297</u>, daughter board, <u>D2000331</u>, and the GPS expansion module, <u>D2000301</u>, require the FPGA timing code, <u>E2000337</u>.

5 Timing Interface Tests

The PCIe Timing Interface is powered by either PCIe slot or External PCIe power. For this testing use the External PCIe power to measure current draw on the bench. Use grounding strap while testing. Properly ground board before applying any voltage.

1) Verify the proper current draw without FPGA program. Using a bench DC supply apply +12 Volts to the PCI power connector. Measure the current draw of the board prior to flashing the FPGA.

+12 Volt current _____ 0.1 A Nom. (20mA)

2) Check voltages on the following test points prior to flashing FPGA program. Come back after flashing the FPGA program and verify that the voltages did not change.

TP30 (+12V)	TP40 (EXT12V)
TP32 (VDD 2.5V)	TP26 (VREG)
TP18 (VCC1V8)	TP17 (AVCC1V8)
TP21 (VCC)	TP34 (VCCINT1.0)
TP12 (P12V)	TP10 (N12V)
TP1 (P5V)	TP3 (N5V)
TP4 (VREF2V5)	TP11 (BGND)
TP36 (A12V)	TP35 (AGND)
_ TP19 (P10V)	
TP14 (AVCC)	TP15 (AVTT)

- **3)** Flash the FPGA with the test code. Using an FPGA programmer, flash the test program, <u>E2100232</u>, to the on-board SPI memory and press the program button (S2) on the back of the PCB behind the JTAG programming header. Ensure that the done light (DS1) is on when the process is complete. Return to step 2 and verify the voltages did not change, note any changes.
- 4) Verify the synchronization frequencies. Using a scope, check

TP20 (PSYNC)_____ Nominal: 524.288 kHz

TP10/R41 bracket side (INV SYNC) Nominal: 32.768 kHz

5) Verify the proper current draw with FPGA program. Using a bench DC supply apply +12Volts to the PCIE power connector. Measure the current draw of the board prior to flashing the FPGA.

+12 Volt current _____ Nom: $0.57 \pm 0.1A$

6) Mount the test daughter board and D-Sub/IDC-10 test adapters, insert PCIe board into PC, and reboot. Run the LIGO Timing Verify program

😚 LIGO Timing Verify	🛛 💀 🔽 🔲 🐺 🐼 🕜 Hot Reload 🛛 <	_	
Global Test/Verify Advanced Diag	nostics		Registers
GPS Seconds: 000000043	GPS Fraction: 2535498176	GPS Time: 43.590342	
Time UTC: 1980-01-06 00:00:43	Leap Seconds: 0 Time Mode:	Valid: Add:	Sub:
Local Time: 1980-01-05 16:00:43	Clock Diff (s): 1308936199.005080	Firmware Revision: 451	
Timing: OK	Root: La Ja Master	Fanout: 🔄 Supported	
	VCXO: Out-of-Range		
GPS. Locked 3	OCXO: Cocked 4		
Interrupt Enable: ✔ MSI 0 🖌 MSI 1 ✔ MSI	2 🖌 MSI 3		
2			1
GPS Time: 43 Statue: Device \\2\		8/25/201#48/267c08a68/08/0054#/9ad	187c8b-d169
Status. Device (): (

7) Check PCIe functionality

1: Device driver connected	Nominal: green
2: GPS Time display	Nominal: counting at 1 sec
3: LOS (Loss of signal)	Nominal: red without fiber
4: VCXO out-of-range	Nominal: red
5: Timing OK/Uplink UP	Nominal: green
On board green LED	Nominal: off

8) Timing fiber connection

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😚 LIGO Timing Verify	🛛 💀 🔽 🔲 🐺 🐼 🖉 Hot Reload	< — — ×
Global Test/Verify Advanced [Diagnostics	Registers
GPS Seconds: 1308937496	GPS Fraction: 1939693888	GPS Time: 1308937496.451620
Time UTC: 2021-06-28 17:44:38	Leap Seconds: 18 Time Mo	de: 📕 Valid: 🔽 Add: 🗌 Sub: 🗌
Local Time: 2021-06-28 10:44:38	Clock Diff (s): -0.000072	Firmware Revision: 451
Timing: 🔽 OK	Root: S Master	Fanout: 🔄 Supported
Uplink: Up Los	VCXO: Out-of-Range	
Interrupt Enable: 🗹 MSI 0 文 MSI 1 文 M	MSI 2 🖌 MSI 3	
GPS Time: 1308937496 Status: Device	\\?\PCI#VEN <u>1</u> 0EE&DEV_D8C6&SUBSYS_D8C	610EE&REV_01#4&267c08a6&0&00E4#{9ad87c8b-d169
3: LOS (Loss of signal)		Nominal: green
5: Timing OK/Uplink UP		Nominal: green
On board green LED		Nominal: on
2: GPS Time display		Nominal: large number
4: VCXO out-of-range		Nominal: green

Global	Test/Verify	Advanced	Diagnostics			Registe
Supply 1	2V: 11.886		Current	(A): 0.570	Power (W):	6.775
VCC 3.	3V: 3.308		Current	(A): 0.650	Power (W):	2.152
VDD 2.	5V: 2.516		Current	(A): 0.326	Power (W):	0.820
VCCAUX 1.	8V: 1.815		Current	(A): 0.301	Power (W):	0.547
VCCINT 1.	0V: 0.995		Current	(A): 0.150	Power (W):	0.149
AVTT 1.	2V: 1.208		AVCC 1	0V: 0.995	VADC 1.8V:	1.805
VCCBRAM 1.	0V: 0.995		VREG 5	1V: 5.130	P10 10.0V:	9.965
N12 -1	2V: -11.610		P5 +	5V: 4.985	N5 -5V:	-4.989
Aları Supj	ms: 🔜 Any oly: 🔜 Main S	Supply	°C	°C VCCINT ·	<97% VCCAUX <97%	XADC Enabled
Ext. Sy	nc.: 0	Ν	Divi	sor: 19 M	Frequency (Hz):	3355443.2
Optic	ons: 🔄 GPS	~	ОСХО	PPS	RS422	IRIG-B
	PCI-E	~	BRAM	XO Locking	2 Link Version	EEPROM read
	ons: 🖌 GPS		Daughter	Fanout		
Expansio						

9) Voltage and current readbacks

Supply 12V:	Nom: +12V	Current (A)	_ Nom: ~0.58A
VCC 3.3V:	Nom: +3.3V	Current (A)	_ Nom: ~0.65A
VDD 2.5V:	Nom: +2.5V	Current (A)	_ Nom: ~0.34A
VCCAUX:	Nom: +1.8V	Current (A)	_Nom: ~0.30A
VCCINT:	Nom: +1.0V	Current (A)	_Nom: ~0.15A
AVTT:	Nom: +1.2V	AVCC:	Nom: +1.0V
		VADC:	Nom: +1.8V
VCCBRAM:	Nom: +1.0V	VREG:	Nom: +5.1V

P10:	Nom: +10V	N12:	Nom: -10V
P5:	Nom: +5V	N5:	_Nom: -5V
10) Check temperature and al	arms		
Temp:	Nom: 50°C to	80°C	
Alarms Any:	Nom: varies	>95°C:	Nom: green
>75°C:	Nom: varies	VCCINT:	Nom: green
VCCAUX:	Nom: green	XADC:	_Nom: green
Supply:	Nom: green	Giga TRX:	Nom: green

If the temperature reads below 75°C, all alarms must show green. If not, "Any" and "75" will show red.

11) Check DIP switches

Nominal switch position of the DIP switch of the board are up. Readback should show 0xFFFF. Now toggle on-off-on each switch in succession starting towards the front of the board (SW1). The readbacks should go from 0xFFFE, 0xFFFD, 0xFFFB, 0xFFF7, 0xFFEF, 0xFFDF, 0xFFBF, to 0xFF7F.

SW1-8: _____: Nom: OK

Now press the two buttons S1 and S2 on the test daughter board and check again the readbacks. They should be 0xFEFF and 0xFDFF.

SW9/10:	: Nom: OK
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12) Check VCXO readback voltage.

This voltage goes from 0-10V and should be somewhat centered to be able to correct for the crystal aging over the years.

VCXO Voltage (V):	: Nominal range: 3–7V
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13) Check external frequency synchronization.

The default settings for Ext. Sync. N and the Divisor M are 0 and 19, respectively. The frequency should then read 3355443.2 Hz. Connect the scope to J9/J10 of the header test adapter and check that there is a differential RS422 square wave signal present at a frequency of 3.3554432 MHz.

J9/J10: _____ Nom: 3.3554432 MHz 3.3V TTL differential

Leave J9 on channel A, and connect channel B to J5 through J8 in turn. The nominal frequencies will be 8 times lower and at different phases.

J9/J5:	Nom: 419.4304 kHz at 0° phase, 3.3V TTL
J9/J6:	Nom: 419.4304 kHz at 135° phase, 3.3V TTL
J9/J7:	Nom: 419.4304 kHz at 90° phase, 3.3V TTL
J9/J8:	Nom: 419.4304 kHz at 45° phase, 3.3V TTL

Leave the scope on J9/J5 and check through the following N/M values.

N=0/M=0:	Nom: no frequency signal
N=1/M=0:	Nom: 2.048 kHz/256 Hz
N=15/M=0:	Nom: 33.554432/4.194304 MHz
N=0/M=1234:	Nom: 54.339/6.792 kHz

14) Check internal frequency synchronization.

Use a scope probe and check on testpoints TP20 (PWRSYNC) and R41 (INVSYNC).

TP20 (PWRSYNC): _____ Nom: 524.288 kHz 3.3V TTL

R41 (INVSYNC): _____ Nom: 32.768 kHz 12V

15) Check DuoTone

Connect the scope to J2 of the DB37 test adapter. It should show 2 sine waves at 960 Hz and 961 Hz and a amplitude ratio of 2. This generates a 1 Hz beat note.

DuoTone: _____ Nom: Present

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16) Check OCXO locking.

LIGO Timing Verify	-+ 0 /							_		
Global	st/verity	Advanced	Diagnostics						Register	5
Daughter 0-31:	0x97F2BE98		Loopbac	k: 0x97F2BE98		Error:	0x00000000			
Daughter 32-63:	0xC00BE4FA		Loopbac	k: 0xCC0BE4FA		Error:	0x0C000000			
Dsub 0-16/17-27:	0xF36CA4EF		Loopbac	k: 0x036DA4EF		Error:	0xF0010000			
	Start Lo	opback Test	X5 Tes	t: 🔄 Include						
Control Set:	0V	+5V	-5V	+2.5V	-2.5V		2.5			
OCXO Error (s):	0.000007637	7				OCXO Control (V):	2.500			
Measured Freq.:	0033554312		Preset Frequenc	y: 0						
Test completed Errors in pins: S59_P/S60_P S59_N/S60_N	- Errors: 0x00	000000 0x0CC	000000 0x00000000							

Connect an OCXO, for example T0900279, to SMA input J5 on the rear side of the board. Check the measured frequency.

Measured frequency: _____ Nom: crystal frequency

Now check the control output by hitting the Control Set buttons in turn, while measuring the voltage at J5 of the DB25 test adapter.

Control set 0V:	Nom: +0.00V
Control set +5V:	Nom: +5.00V
Control set –5V:	Nom: -5.00V
Control set +2.5V:	Nom: +2.50V
Control set -2.5V:	Nom: -2.50V

17) Loopback testing.

Start the test by pressing the "Start Loopback Test" button. The test should return with "Test completed - No errors." If not, write down the failed signals:

Failed:

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- 18) Flash the FPGA with the production code. After removing all test adapters: Using an FPGA programmer, flash the production program, code, <u>E2000337</u>, to the on-board SPI
- FPGA programmer, flash the production rogram, code, $\underline{E2000337}$, to the on-board SPI memory and press the program button (S2) on the back of the PCB behind the JTAG programming header. Ensure that the done light (DS1) is on when the process is complete.

Put the board back into the test computer

19) Verify the proper current draw with FPGA program. Using a bench DC supply apply +12Volts to the PCIE power connector. Measure the current draw of the board prior to flashing the FPGA.

+12 Volt current _____ Nom: $0.7 \pm 0.1A$

6 Backplane Test

Continue with test procedure $\underline{T2100299}$, if this timing interface is used with a backplane.

7 Pass/Fail