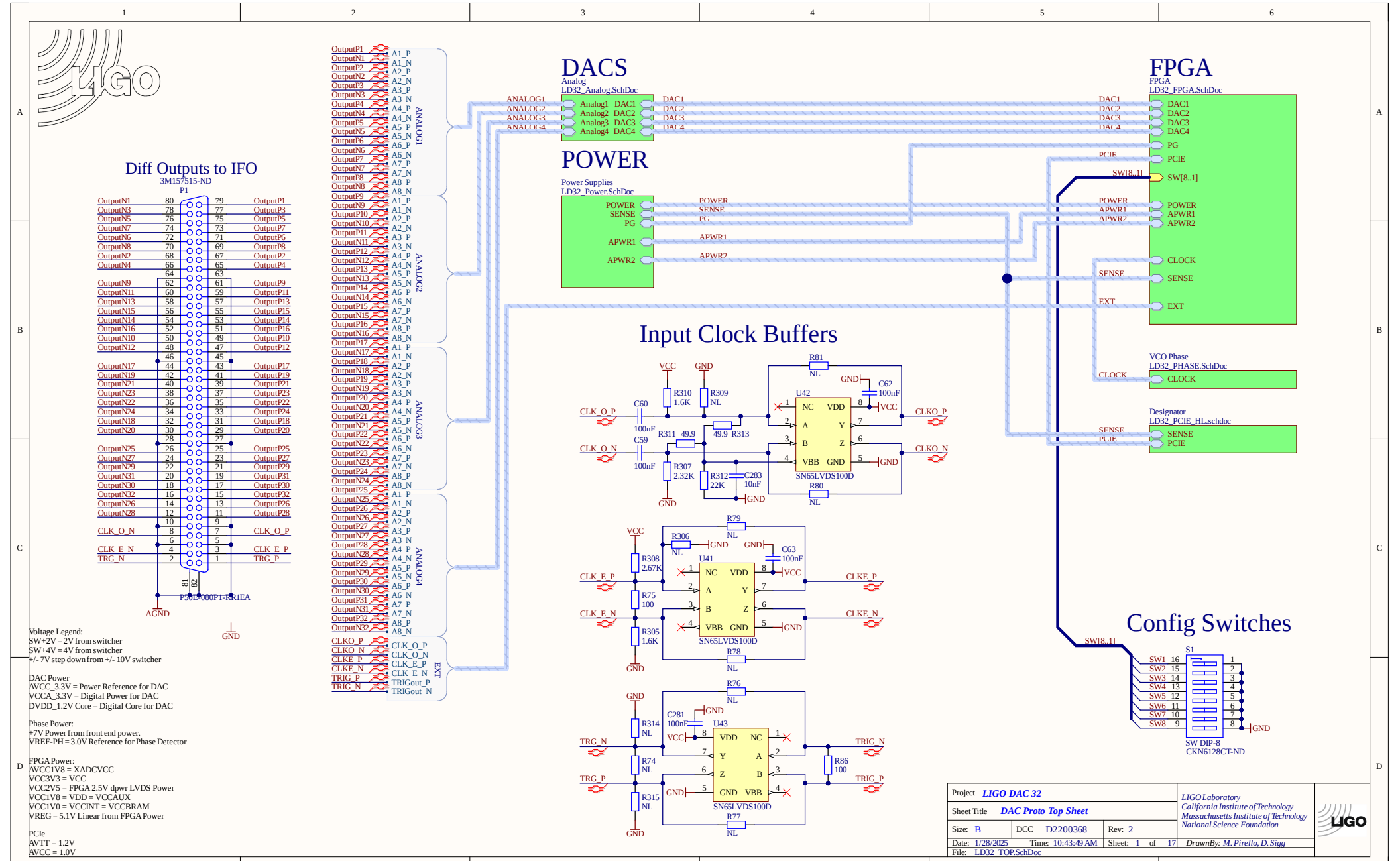
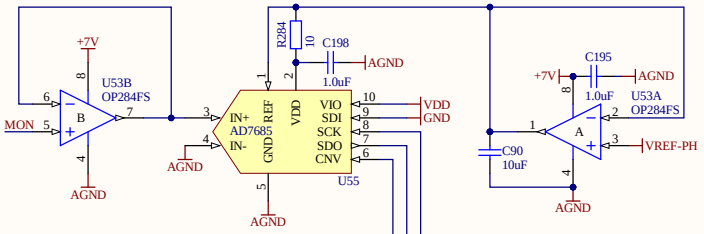
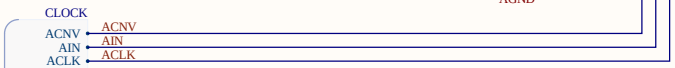

DACS
Analog
LD32_Analog.SchDoc
POWER
Power Supplies
LD32_Power.SchDoc
FPGA
FPGA
LD32_FPGA.SchDoc
VCO Phase
LD32_PHASE.SchDoc
Designator
LD32_PCIE_HL.schdoc
Diff Outputs to IFO
3M157515-ND
P1
P50L-080P1-RR1EA
Input Clock Buffers
SN65LVDS100D
Config Switches
SW DIP-8
CKN6128CT-ND
Voltage Legend:
SW+2V = 2V from switcher
SW+4V = 4V from switcher
+/- 7V step down from +/- 10V switcher
DAC Power
AVCC_3.3V = Power Reference for DAC
VCCA_3.3V = Digital Power for DAC
DVDD_1.2V Core = Digital Core for DAC
Phase Power:
+7V Power from front end power.
VREF-PH = 3.0V Reference for Phase Detector
FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM
VREG = 5.1V Linear from FPGA Power
PCIe
AVTT = 1.2V
AVCC = 1.0V
Project LIGO DAC 32
Sheet Title DAC Proto Top Sheet
Size: B
DCC D2200368
Rev: 2
Date: 1/28/2025
Time: 10:43:49 AM
Sheet: 1 of 17
File: LD32_TOP.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello, D. Sigg

Control Voltage Monitor





Voltage Legend:
SW+2V = 2V from switcher
SW+4V = 4V from switcher
+/- 7V step down from +/- 10V switcher

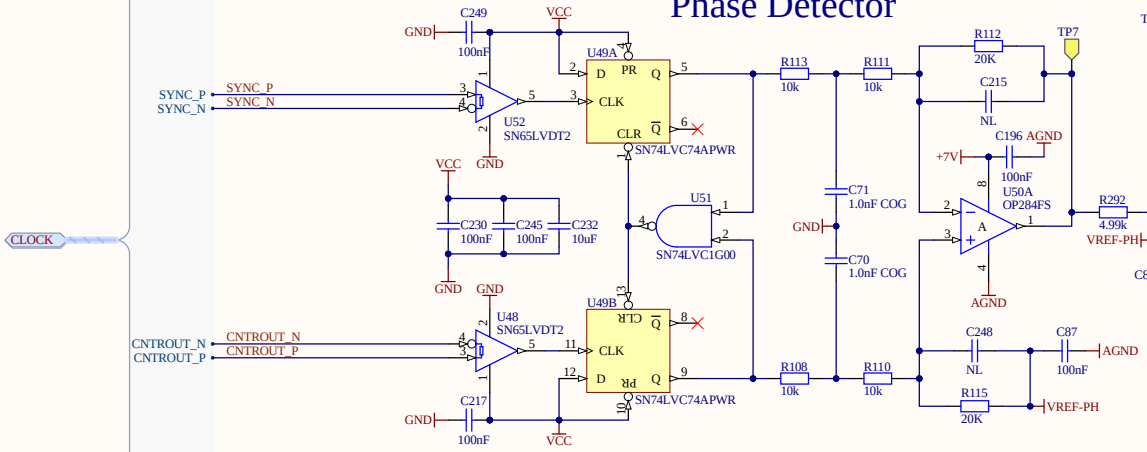
DAC Power
AVCC_3.3V = Power Reference for DAC
VCCA_3.3V = Digital Power for DAC
DVDD_1.2V Core = Digital Core for DAC

Phase Power:
+7V Power from front end power.
VREF-PH = 3.0V Reference for Phase Detector

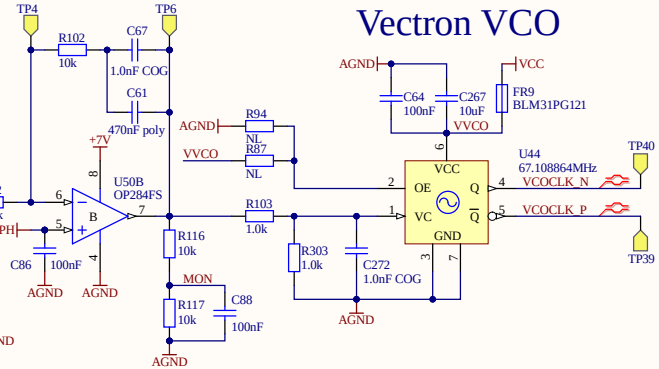
FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM
VREG = 5.1V Linear from FPGA Power

PCIe
AVTT = 1.2V
AVCC = 1.0V

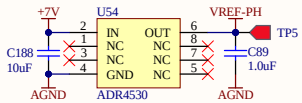
Phase Detector



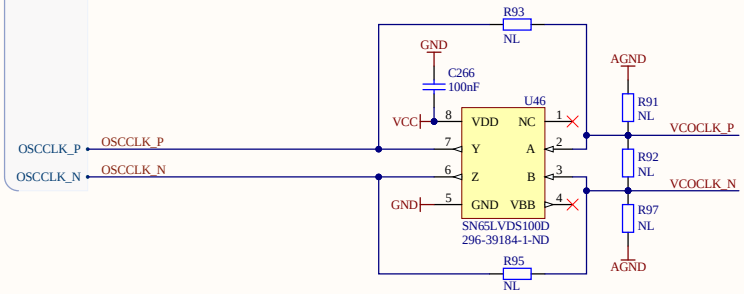
Vectron VCO



3.0V Reference

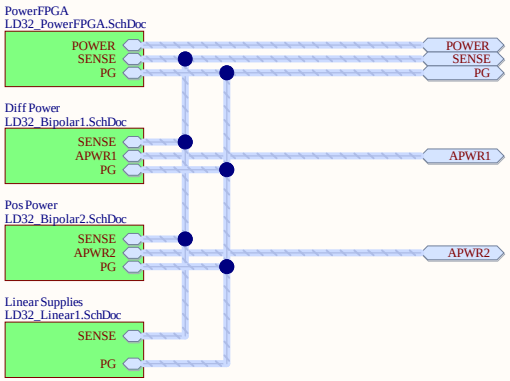


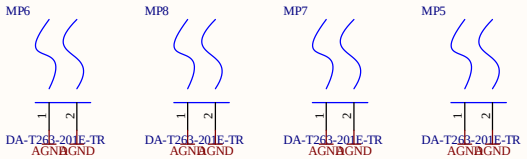
Optional LVPECL-LVDS Translator



Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*VCO & Phase Detector*		
Size: B	DCC D2200368	Rev: 2	
Date: 1/28/2025	Time: 10:43:49 AM	Sheet: 2 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_PHASE.SchDoc			

Power Top Sheet





Voltage Legend:
SW+2V = 2V from switcher
SW+4V = 4V from switcher
+/- 7V step down from +/- 10V switcher

DAC Power
AVCC_3.3V = Power Reference for DAC
VCCA_3.3V = Digital Power for DAC
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+7V Power from front end power.
VREF-PH = 3.0V Reference for Phase Detector

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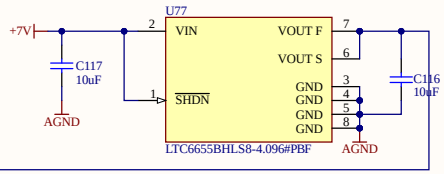
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM
VREG = 5.1V Linear from FPGA Power

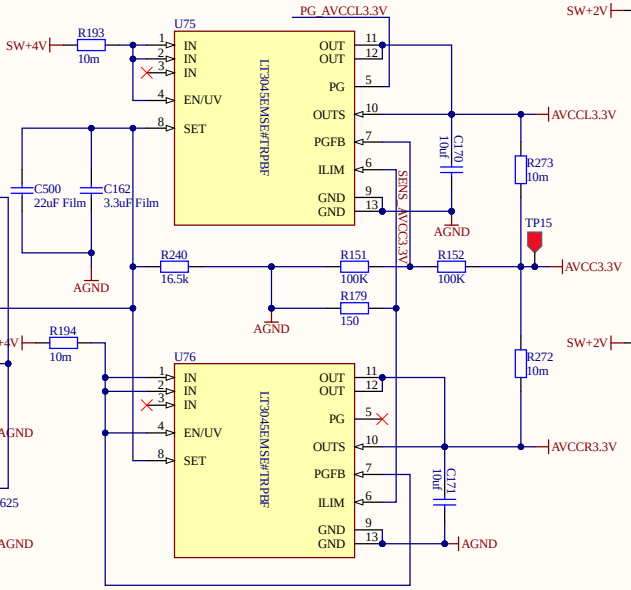
PCIe
AVTT = 1.2V
AVCC = 1.0V

Project	***LIGO DAC 32***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***Power Top***		
Size: B	DCC D2200368	Rev: 2	
Date: 1/28/2025 Time: 10:43:49 AM		Sheet: 3 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_Power.SchDoc			

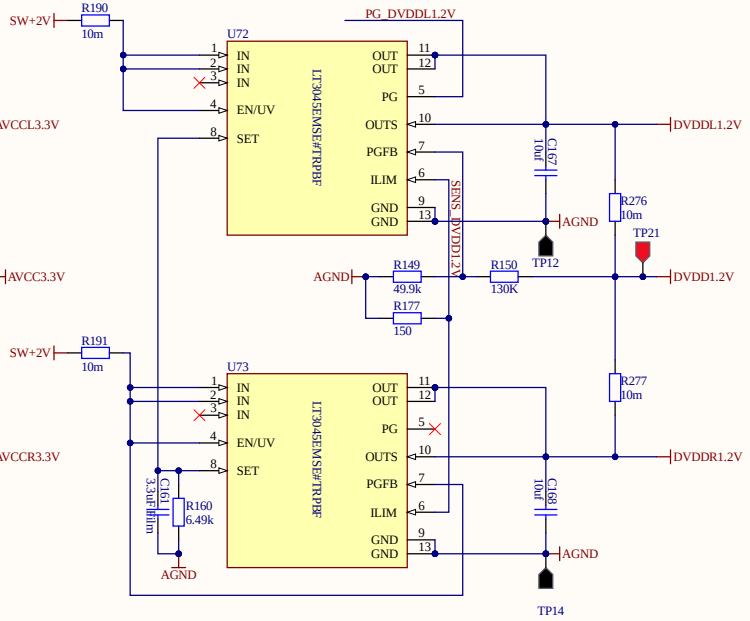
DAC Linear Power Supplies



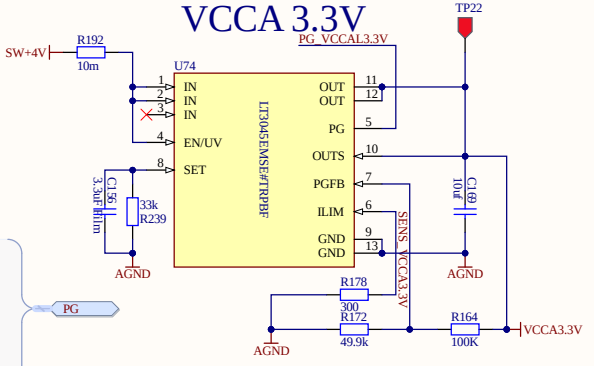
AVCC 3.3V

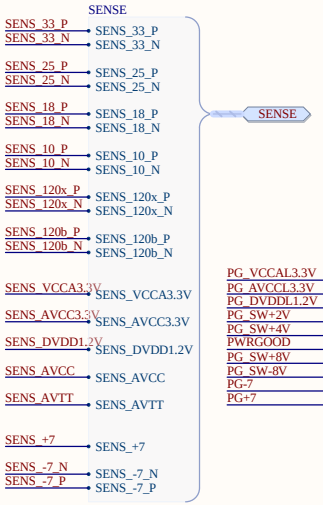


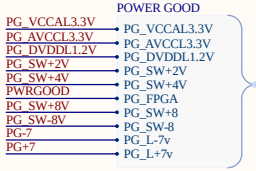
DVDD 1.2V Core



VCCA 3.3V







LT3045-1 Configs:
VCCA3V3
Vset = Iset * Rset = 100uA * Rset
Rs = 33k
Vset = 33k *100uA = 3.3V
PGFB:
Vset = 3.3V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(3.3V/0.3V-1) = 10k < 11k

AVCC3V3:
Vset = Iset * Rset = 100uA * Rset
Rs = 33k
Vset = 33k *100uA = 3.3V
PGFB:
Vset = 3.3V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(3.3V/0.3V-1) = 10k < 11k

LT3045-1 Configs:
DVDD1V2:
Vset = Iset * Rset = 100uA * Rset
Rs = 12.1k
Vset = 12.1k *100uA = 1.21V
PGFB:
Vset = 1.2V ; RPG1 = 50k
Vset = 0.3*(1+RPG2/RPG1)
RPG2 = (Vset/0.3V-1)*50k
RPG2 = (1.2/0.3-1)*50k = 150k > 133k

Voltage Legend:
SW+2V = 2V from switcher
SW+4V = 4V from switcher
+/- 7V step down from +/- 10V switcher

DAC Power
AVCC_3.3V = Power Reference for DAC
VCCA_3.3V = Digital Power for DAC
DVDD_1.2V Core = Digital Core for DAC

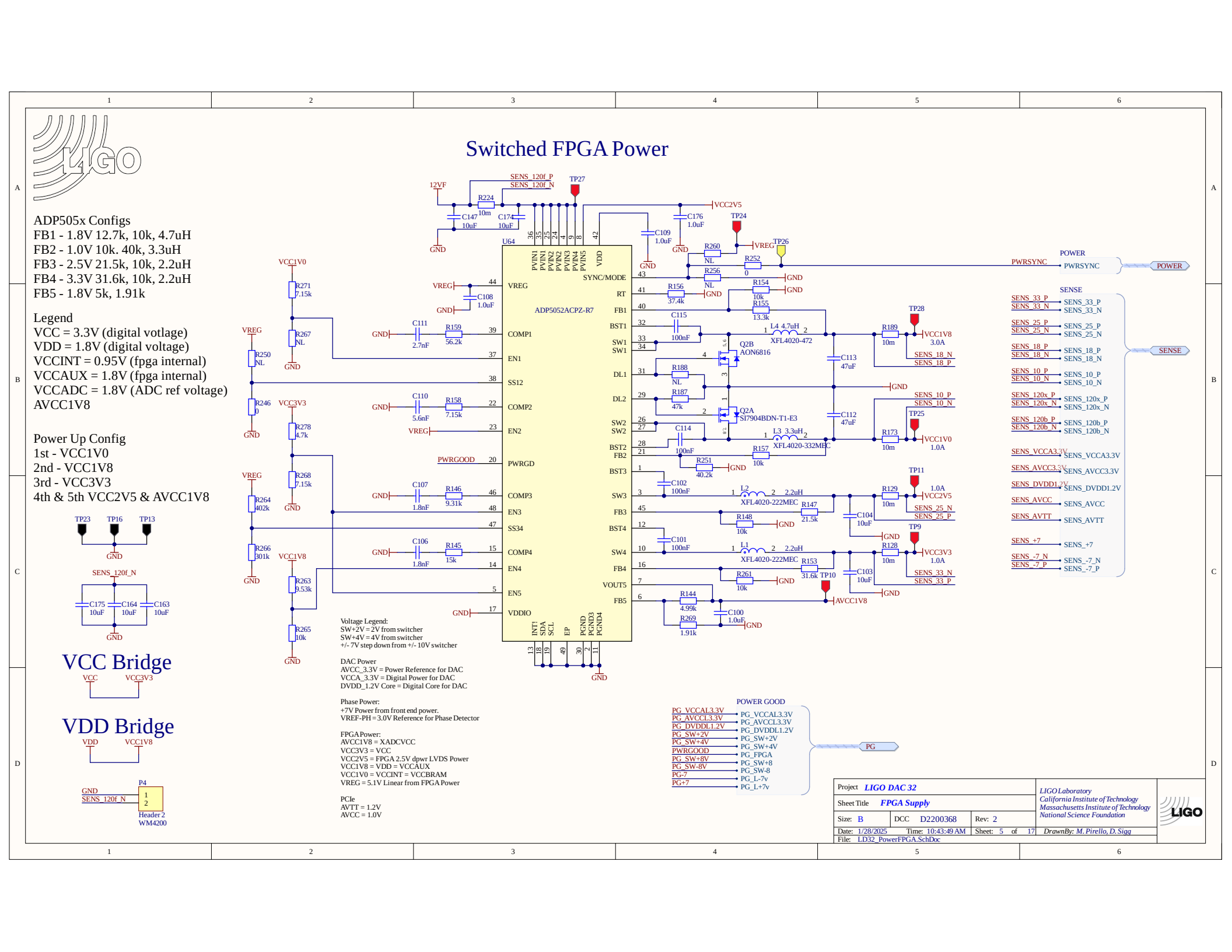
Phase Power:
+7V Power from front end power.
VREF-PH = 3.0V Reference for Phase Detector

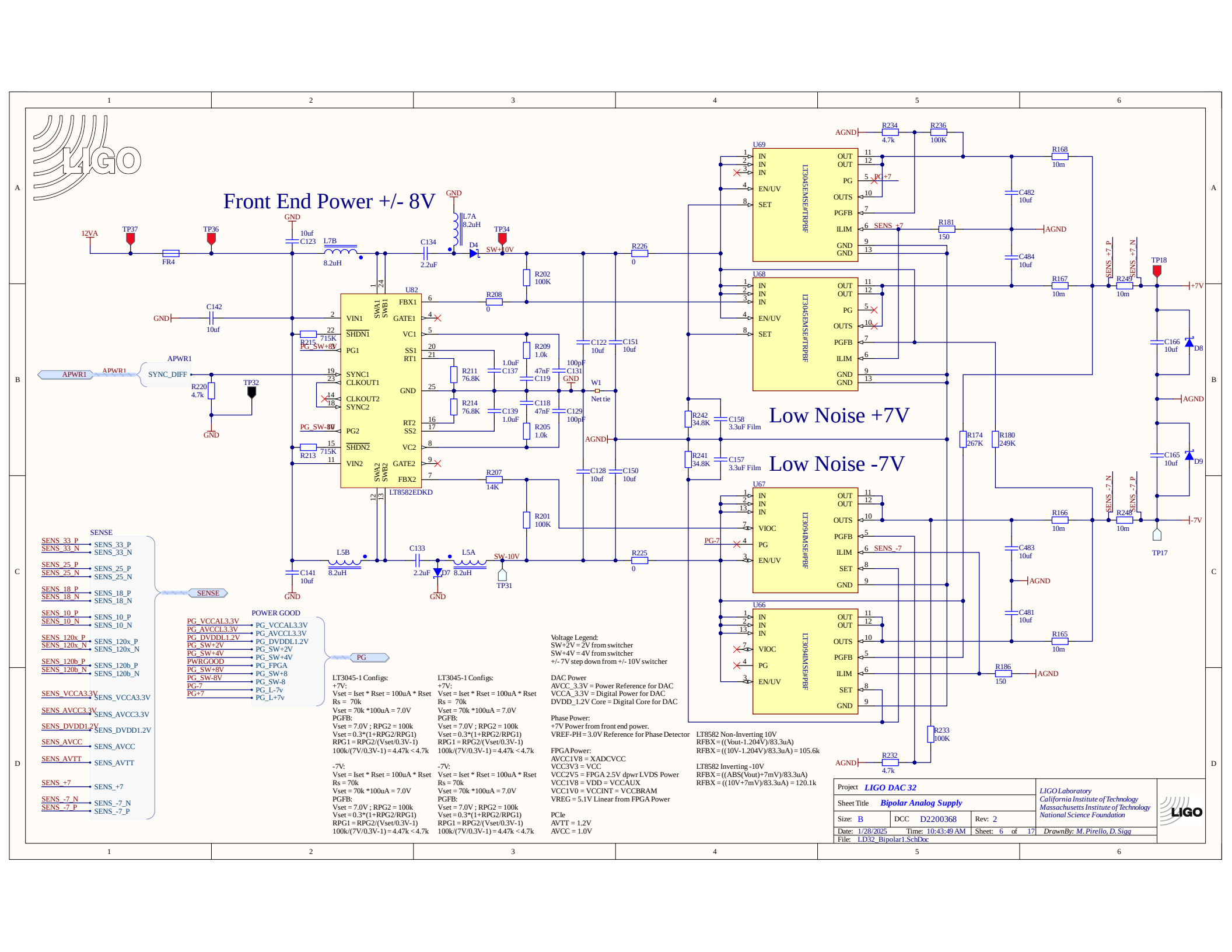
FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM
VREG = 5.1V Linear from FPGA Power

PCIe
AVTT = 1.2V
AVCC = 1.0V

Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Linear Supplies*		
Size: B	DCC D2200368	Rev: 2	
Date: 1/28/2025	Time: 10:43:49 AM	Sheet: 4 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_Linear1.SchDoc			

Switched FPGA Power




Front End Power +/- 8V
Low Noise +7V
Low Noise -7V
U82
LT8582EDKD
U69
U68
U67
U66
LT3045EMSE#TRPBF
LT3094IMSE#PBF
SENSE
POWER GOOD
PG
Voltage Legend:
SW+2V = 2V from switcher
SW+4V = 4V from switcher
+/- 7V step down from +/- 10V switcher
DAC Power
AVCC_3.3V = Power Reference for DAC
VCCA_3.3V = Digital Power for DAC
DVDD_1.2V Core = Digital Core for DAC
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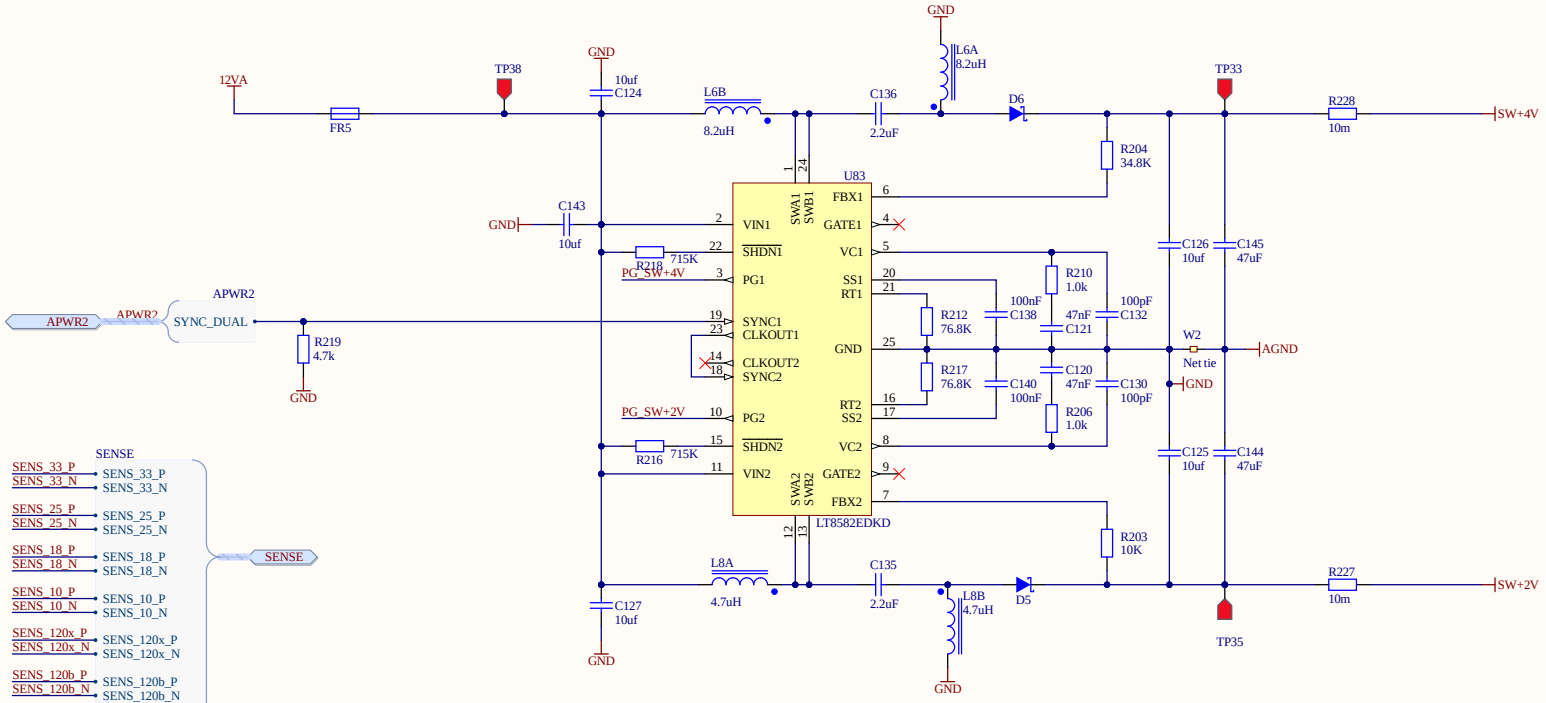
FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM
VREG = 5.1V Linear from FPGA Power
PCIe
AVTT = 1.2V
AVCC = 1.0V
LT8582 Non-Inverting 10V
RFBX = ((Vout-1.204V)/83.3uA)
RFBX = ((10V-1.204V)/83.3uA) = 105.6k
LT8582 Inverting -10V
RFBX = ((ABS(Vout)+7mV)/83.3uA)
RFBX = ((10V+7mV)/83.3uA) = 120.1k
LT3045-1 Configs:
+7V:
Vset = Iset * Rset = 100uA * Rset
Rs = 70k
Vset = 70k *100uA = 7.0V
PGFB:
Vset = 7.0V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(7V/0.3V-1) = 4.47k < 4.7k
-7V:
Vset = Iset * Rset = 100uA * Rset
Rs = 70k
Vset = 70k *100uA = 7.0V
PGFB:
Vset = 7.0V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(7V/0.3V-1) = 4.47k < 4.7k
Project LIGO DAC 32
Sheet Title Bipolar Analog Supply
Size: B DCC D2200368 Rev: 2
Date: 1/28/2025 Time: 10:43:49 AM Sheet: 6 of 17
File: LD32_Bipolar1.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello, D. Sigg

DAC Switcher



SENSE

SENS_33_P → SENS_33_P
SENS_33_N → SENS_33_N
SENS_25_P → SENS_25_P
SENS_25_N → SENS_25_N
SENS_18_P → SENS_18_P
SENS_18_N → SENS_18_N
SENS_10_P → SENS_10_P
SENS_10_N → SENS_10_N
SENS_120x_P → SENS_120x_P
SENS_120x_N → SENS_120x_N
SENS_120b_P → SENS_120b_P
SENS_120b_N → SENS_120b_N
SENS_VCCA3.3V → SENS_VCCA3.3V
SENS_AVCC3.3V → SENS_AVCC3.3V
SENS_DVDD1.2V → SENS_DVDD1.2V
SENS_AVCC → SENS_AVCC
SENS_AVTT → SENS_AVTT
SENS_+7 → SENS_+7
SENS_-7_N → SENS_-7_N
SENS_-7_P → SENS_-7_P

→ SENSE

POWER GOOD

PG_VCCAL3.3V → PG_VCCAL3.3V
PG_AVCCL3.3V → PG_AVCCL3.3V
PG_DVDDL1.2V → PG_DVDDL1.2V
PG_SW+2V → PG_SW+2V
PG_SW+4V → PG_SW+4V
PWRGOOD → PG_FPGA
PG_SW+8V → PG_SW+8
PG_SW-8V → PG_SW-8
PG-7 → PG_L-7v
PG+7 → PG_L+7v

→ PG

Voltage Legend:
SW+2V = 2V from switcher
SW+4V = 4V from switcher
+/- 7V step down from +/- 10V switcher

DAC Power
AVCC_3.3V = Power Reference for DAC
VCCA_3.3V = Digital Power for DAC
DVDD_1.2V Core = Digital Core for DAC

Phase Power:
+7V Power from front end power.
VREF-PH = 3.0V Reference for Phase Detector

FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM
VREG = 5.1V Linear from FPGA Power

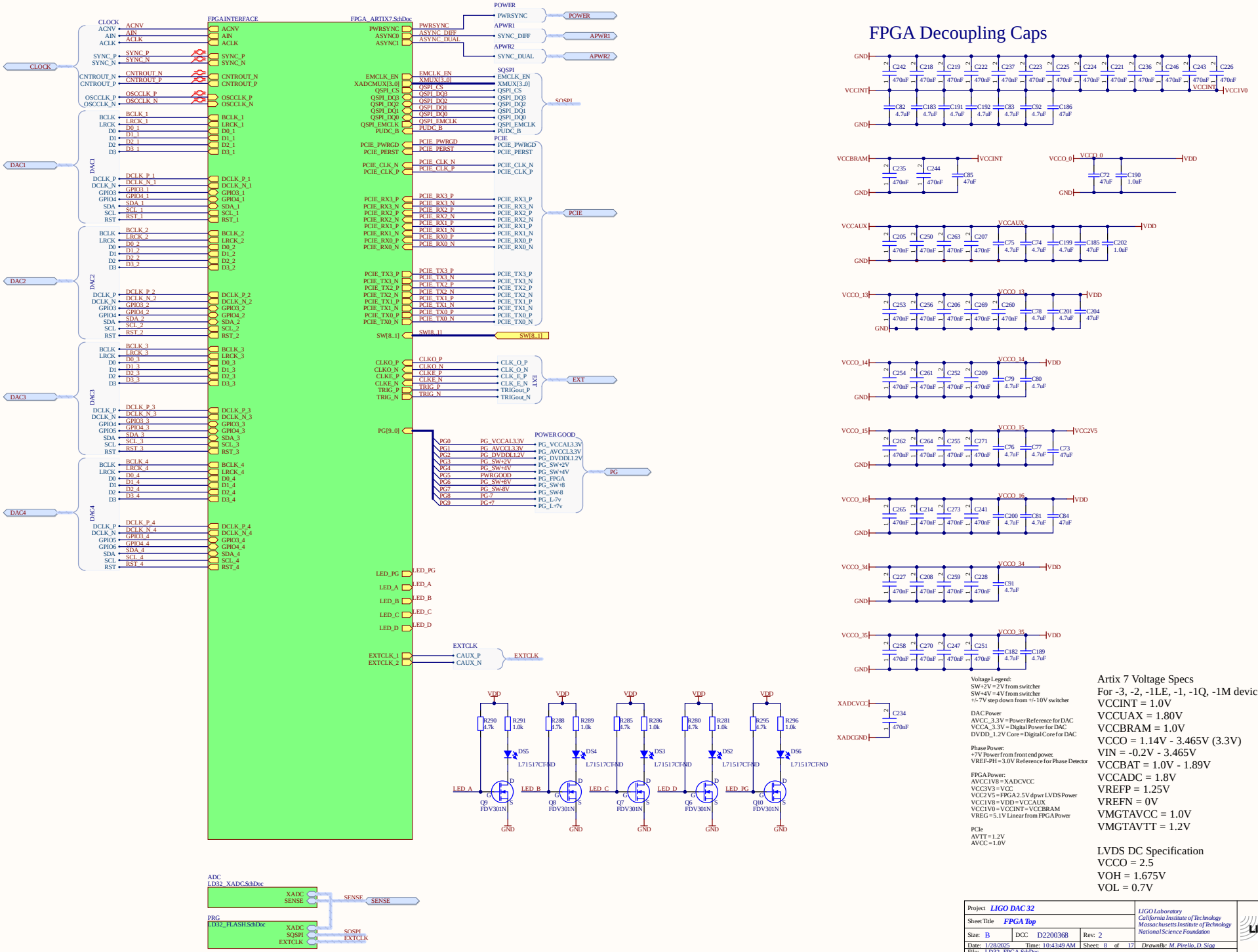
PCIe
AVTT = 1.2V
AVCC = 1.0V

LT8585EDKD Configs:
+4V
RFBX = (Vout-1.204V)/83.3uA
RFBX = (4.0V-1.204V)/83.3uA
RFBX = 33.565k #NAME? 34.8k
RT = 76k (1MHz)
C1 > 1uF
4uH < Ltyp < 22uH
COUT >33uF

+2V
RFBX = (Vout-1.204V)/83.3uA
RFBX = (2.0V-1.204V)/83.3uA
RFBX = 9.55k #NAME? 10k
RT = 76k (1MHz)
C1 > 1uF
2.3uH < Ltyp < 12.6uH
COUT >45uF

Front End Power +/- 7V
QC per channel 5.5mA * 64 = 352mA so single supplies are sufficient
DVDD 1.2V 128 * 4 = 512mA > 500mA so two supplies
VCCA 3.3V one supply
AVDD 1.8V one suppply
AVCC_R 3.3V 90*4 = 360mA one supply
AVCC_L 3.3V 90*4 = 360mA one supply
VDD_R, VDD_L 3.3V 128 per DAC * 4 = 512mA > 500mA is two supplies

Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Dual Analog Supply*		
Size: B	DCC D2200368	Rev: 2	
Date: 1/28/2025 Time: 10:43:49 AM	Sheet: 7 of 17	*DrawnBy: M. Pirello, D. Sigg*	
File: LD32_Bipolar2.SchDoc			



FPGA Decoupling Caps

Voltage Legend:
SW+2V = 2V from switcher
SW+4V = 4V from switcher
+/- 7V step down from +/- 10V switcher

DAC Power
AVCC_3.3V = Power Reference for DAC
VCCA_3.3V = Digital Power for DAC
DVDD_1.2V Core = Digital Core for DAC

Phase Power:
+7V Power from front end power.
VREF-PH = 3.0V Reference for Phase Detector

FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM
VREG = 5.1V Linear from FPGA Power

PCIe
AVTT = 1.2V
AVCC = 1.0V

Artix 7 Voltage Specs

For -3, -2, -1LE, -1, -1Q, -1M devices
VCCINT = 1.0V
VCCUAX = 1.80V
VCCBRAM = 1.0V
VCCO = 1.14V - 3.465V (3.3V)
VIN = -0.2V - 3.465V
VCCBAT = 1.0V - 1.89V
VCCADC = 1.8V
VREFP = 1.25V
VREFN = 0V
VMGTAVCC = 1.0V
VMGTAVTT = 1.2V

LVDS DC Specification

VCCO = 2.5
VOH = 1.675V
VOL = 0.7V

Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*FPGA Top*		
Size: B	DCC: D2200368	Rev: 2	
Date: 1/28/2025	Time: 10:43:49 AM	Sheet 8 of 17	*DrawnBy: M.Pirello, D.Sigg*
File: LD32_FPGA.SchDoc			

JTAG and SPI Flash

VDD is 1.8V for this design

SPI Memory

100 MHz Program Clock

AUX Input Clock Buffers

JTAG Header

Voltage Legend:
SW+2V = 2V from switcher
SW+4V = 4V from switcher
+/- 7V step down from +/- 10V switcher

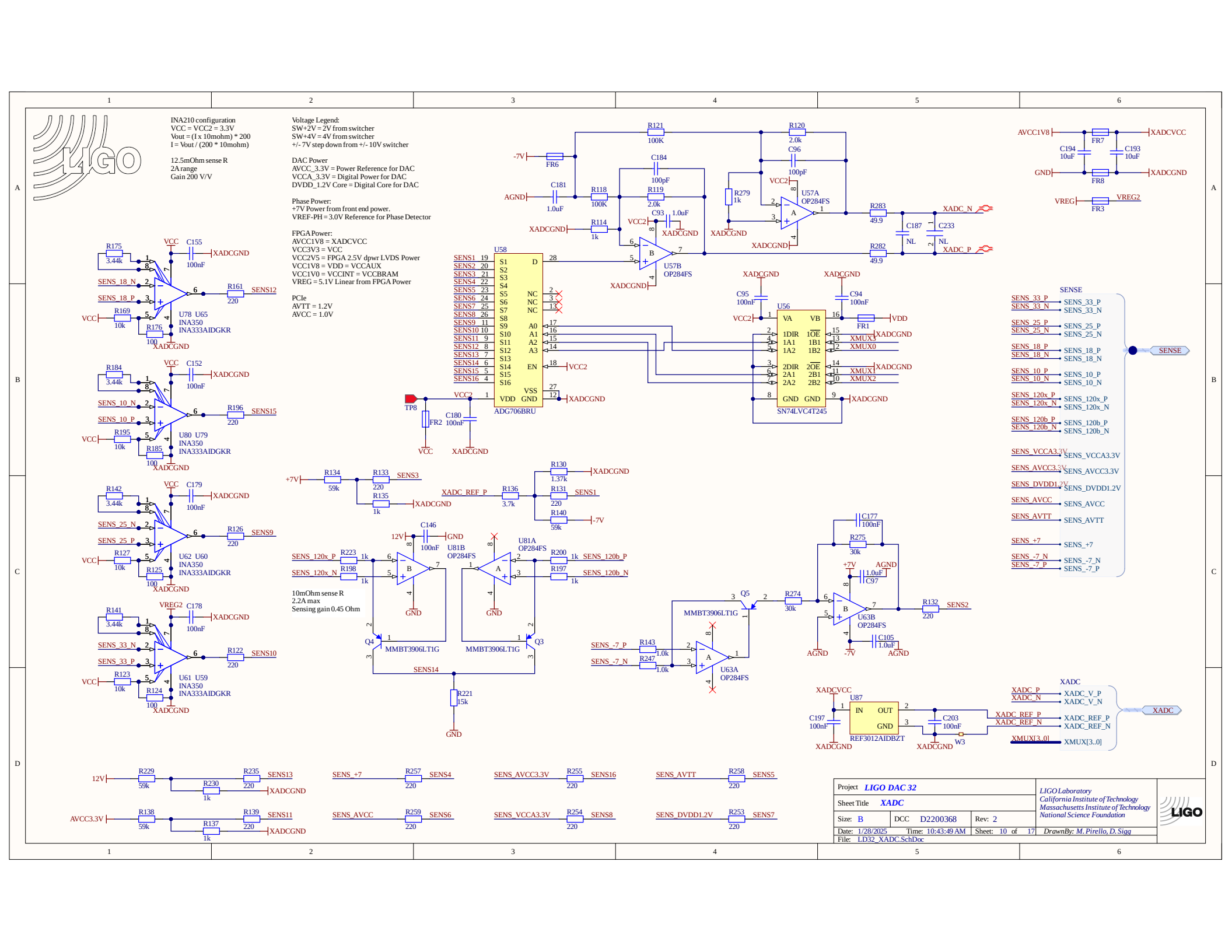
DAC Power
AVCC_3.3V = Power Reference for DAC
VCCA_3.3V = Digital Power for DAC
DVDD_1.2V Core = Digital Core for DAC

Phase Power:
+7V Power from front end power.
VREF-PH = 3.0V Reference for Phase Detector

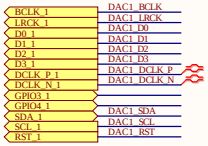
FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM
VREG = 5.1V Linear from FPGA Power

PCIe
AVTT = 1.2V
AVCC = 1.0V

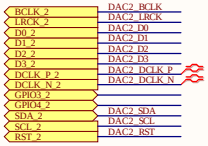
Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*JTAG & SPI Flash*		
Size: B	DCC D2200368	Rev: 2	
Date: 1/28/2025	Time: 10:43:49 AM	Sheet: 9 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FLASH.SchDoc			


INA210 configuration
VCC = VCC2 = 3.3V
Vout = (I x 10mohm) * 200
I = Vout / (200 * 10mohm)
12.5mOhm sense R
2A range
Gain 200 V/V
Voltage Legend:
SW+2V = 2V from switcher
SW+4V = 4V from switcher
+/- 7V step down from +/- 10V switcher
DAC Power
AVCC_3.3V = Power Reference for DAC
VCCA_3.3V = Digital Power for DAC
DVDD_1.2V Core = Digital Core for DAC
Phase Power:
+7V Power from front end power.
VREF-PH = 3.0V Reference for Phase Detector
FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM
VREG = 5.1V Linear from FPGA Power
PCIe
AVTT = 1.2V
AVCC = 1.0V
U78 U65
INA350
INA333AIDGKR
U80 U79
U62 U60
U61 U59
U58
ADG706BRU
U56
SN74LVC4T245
U57A
U57B
OP284FS
U81A
U81B
U63A
U63B
MMBT3906LT1G
U87
REF3012AIDBZT
10mOhm sense R
2.2A max
Sensing gain 0.45 Ohm
SENSE
XADC
Project LIGO DAC 32
Sheet Title XADC
Size: B
DCC D2200368
Rev: 2
Date: 1/28/2025
Time: 10:43:49 AM
Sheet: 10 of 17
File: LD32_XADC.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello, D. Sigg

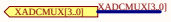
DAC 1



DAC2

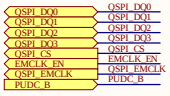


FPGA xADC

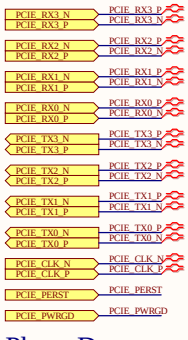


FPGA Config

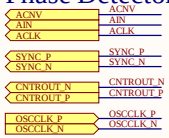
FPGA Flash



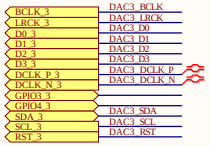
PCIe Connector



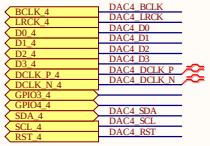
Phase Detector

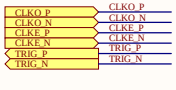


DAC3

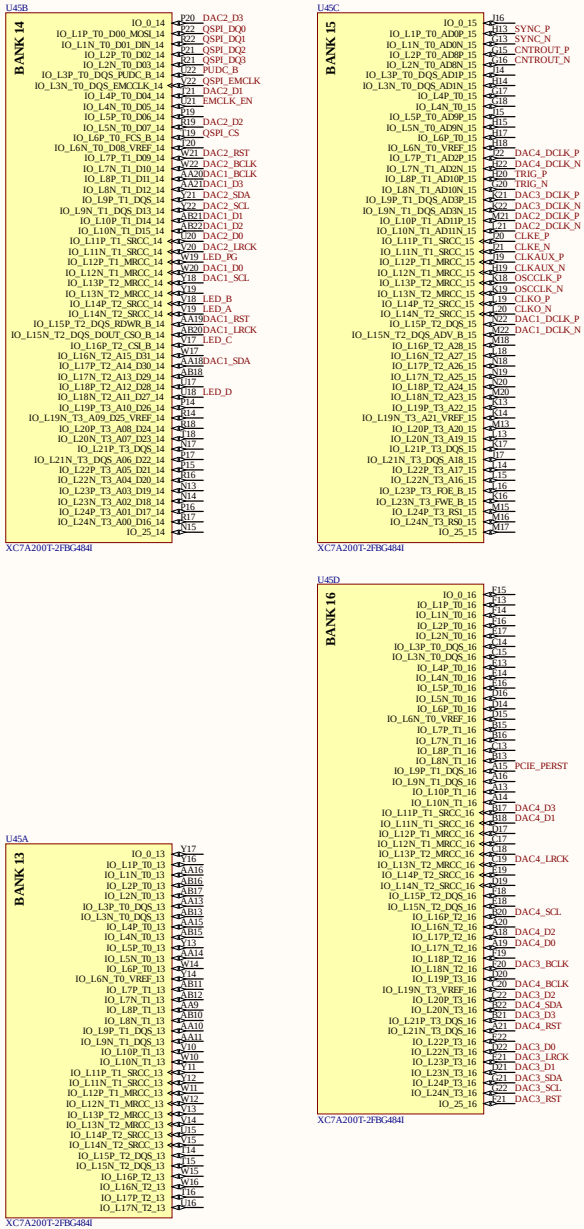


DAC4



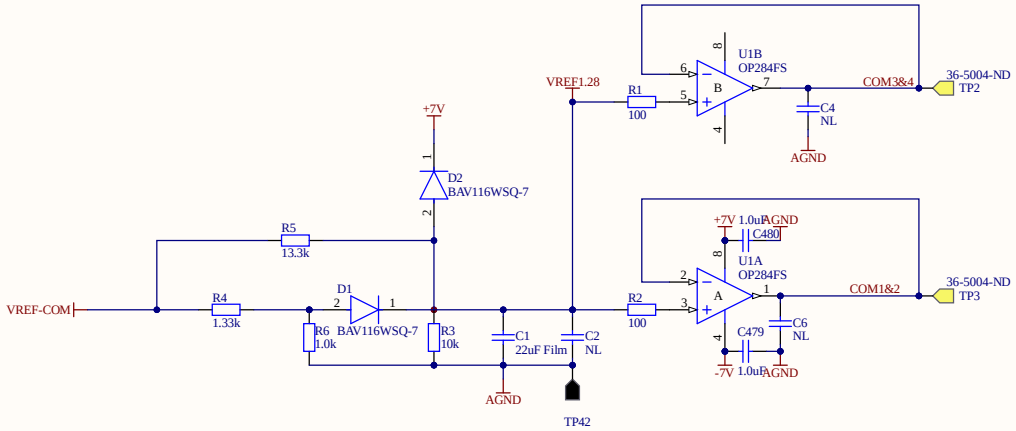


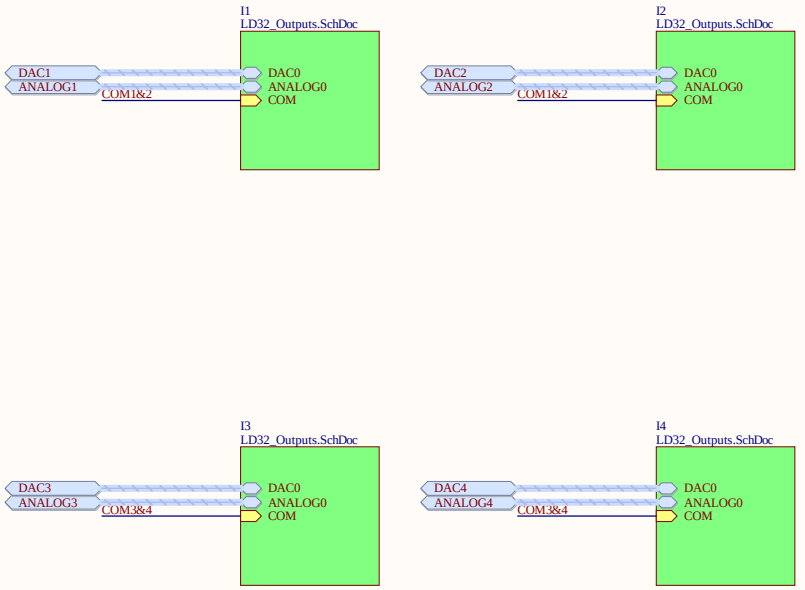
Optional External Clock



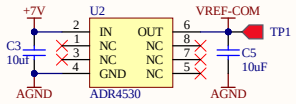
Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*FPGA*		
Size: B	DCC: D2200368	Rev: 2	
Date: 1/28/2025	Time: 10:43:50 AM	Sheet 11 of 17	*Drawn By: M.Pirello, D.Sigg*
File: FPGA_ARTIX7.SchDoc			

Multiple DAC's COM Distro





3.0V COM Reference



Voltage Legend:
SW+2V = 2V from switcher
SW+4V = 4V from switcher
+/- 7V step down from +/- 10V switcher

DAC Power
AVCC_3.3V = Power Reference for DAC
VCCA_3.3V = Digital Power for DAC
DVDD_1.2V Core = Digital Core for DAC

Phase Power:
+7V Power from front end power.
VREF-PH = 3.0V Reference for Phase Detector

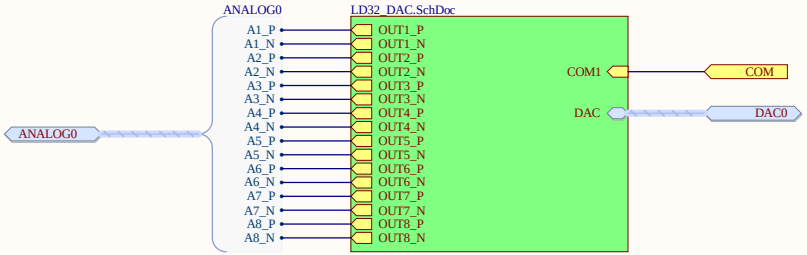
FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM
VREG = 5.1V Linear from FPGA Power

PCIe
AVTT = 1.2V
AVCC = 1.0V

Parts Checked for =Value and Consistency

Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *DAC Top*			
Size: B	DCC D2200368	Rev: 2	
Date: 1/28/2025	Time: 10:43:50 AM	Sheet: 12 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_Analog.SchDoc			

DAC Overview



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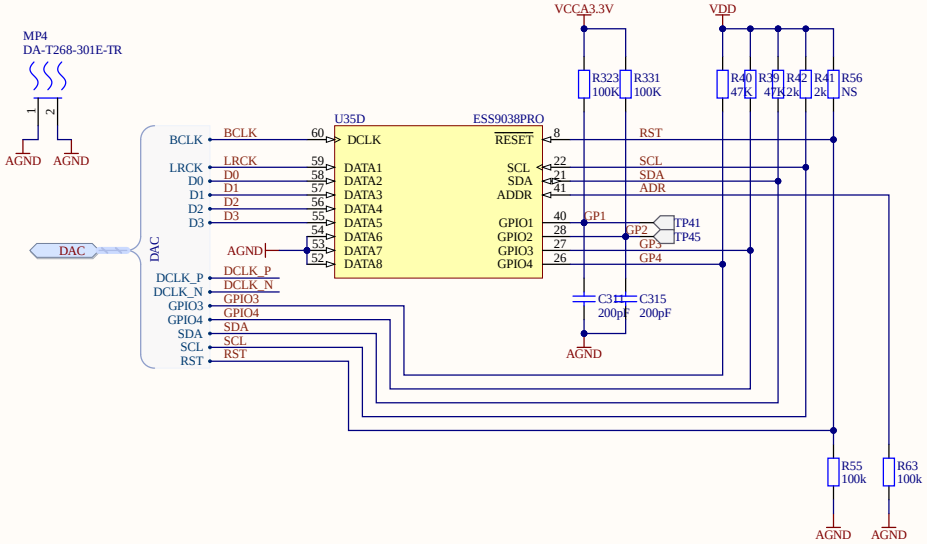
VCC1V0 = VCCINT = VCCBRAM
VREG = 5.1V Linear from FPGA Power

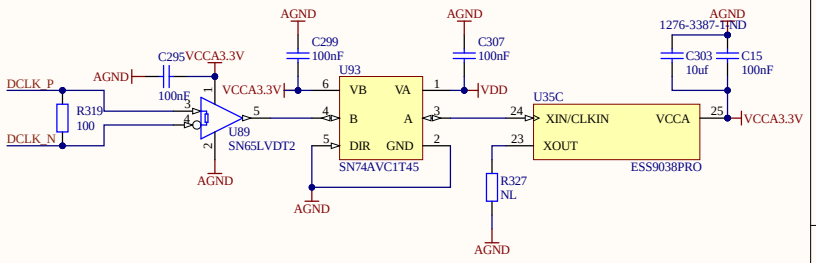
PCIe
AVTT = 1.2V
AVCC = 1.0V

Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *DAC Overview*			
Size: B	DCC D2200368	Rev: 2	
Date: 1/28/2025 Time: 10:43:50 AM		Sheet: 13 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_Outputs.SchDoc			

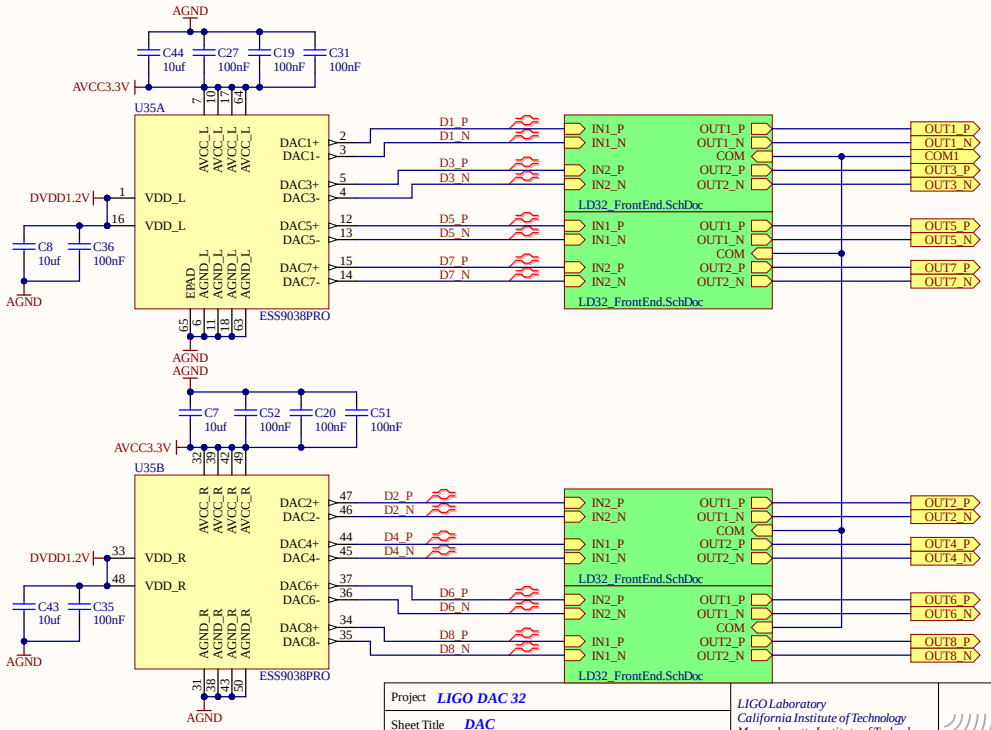
DAC Inputs



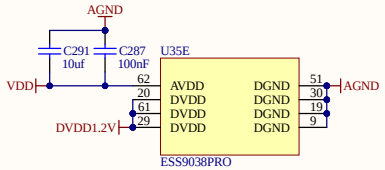
Main Clock



DAC Outputs



Core Power



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VCC1V0 = VCCINT = VCCBRAM
VREG = 5.1V Linear from FPGA Power

PCIe
AVTT = 1.2V
AVCC = 1.0V

Parts Checked for =Value and Consistency

Clock lines and reset could be shared in principle.

You also routed more lines than we really need.

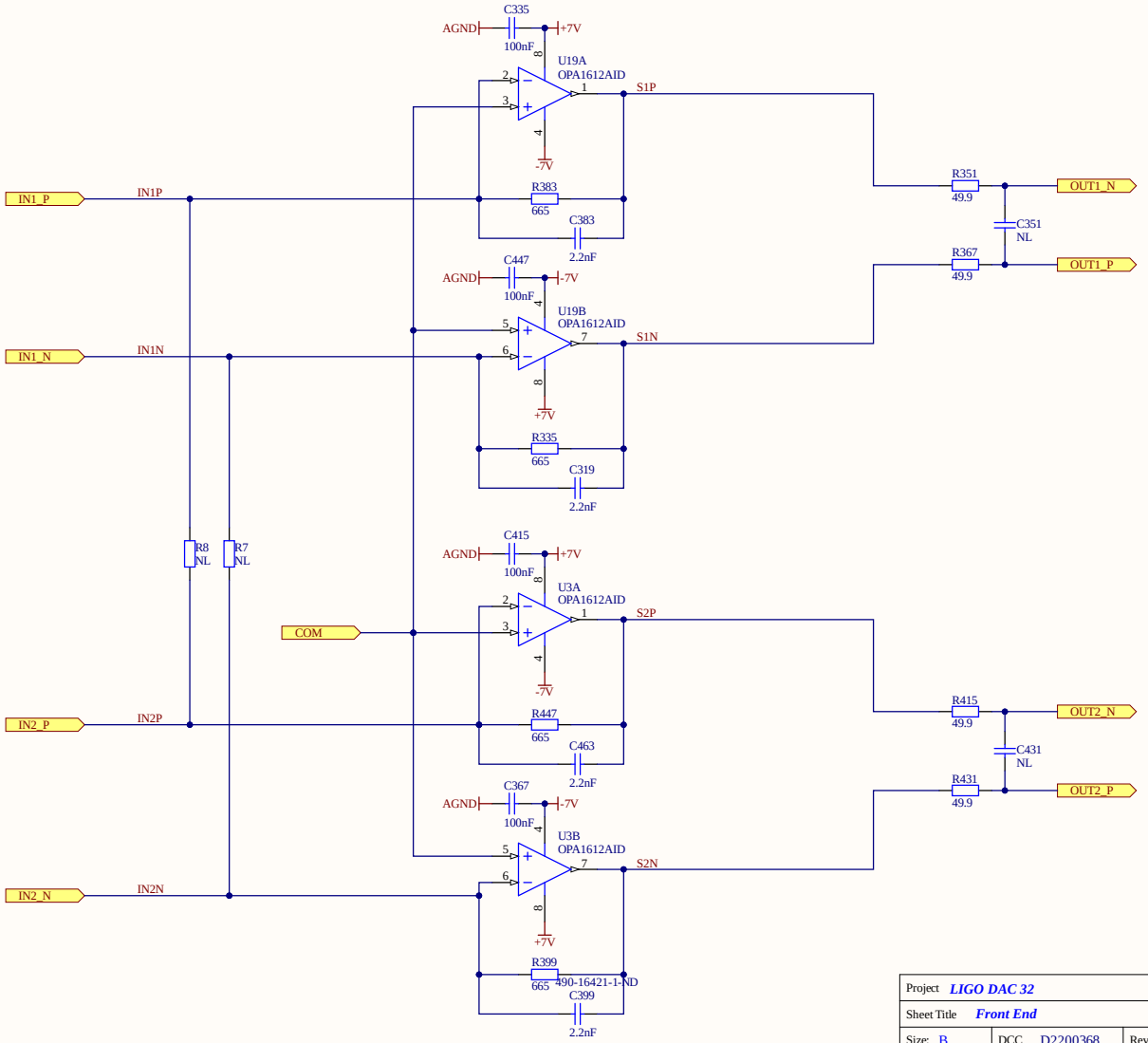
1 fast clock (LVDS, SN65LVDS104 for FO)
1 BCLK
1 LRCLK
4 D lines
2 I2C lines
is needed per DAC.

There will be a difference between Artix-7 and Artix Ultrascale with later only supporting 1.8V.

Daniel

Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*DAC*		
Size: B	DCC D2200368	Rev: 2	
Date: 1/28/2025	Time: 10:43:50 AM	Sheet: 14 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_DAC.SchDoc			

Front End Amplifiers



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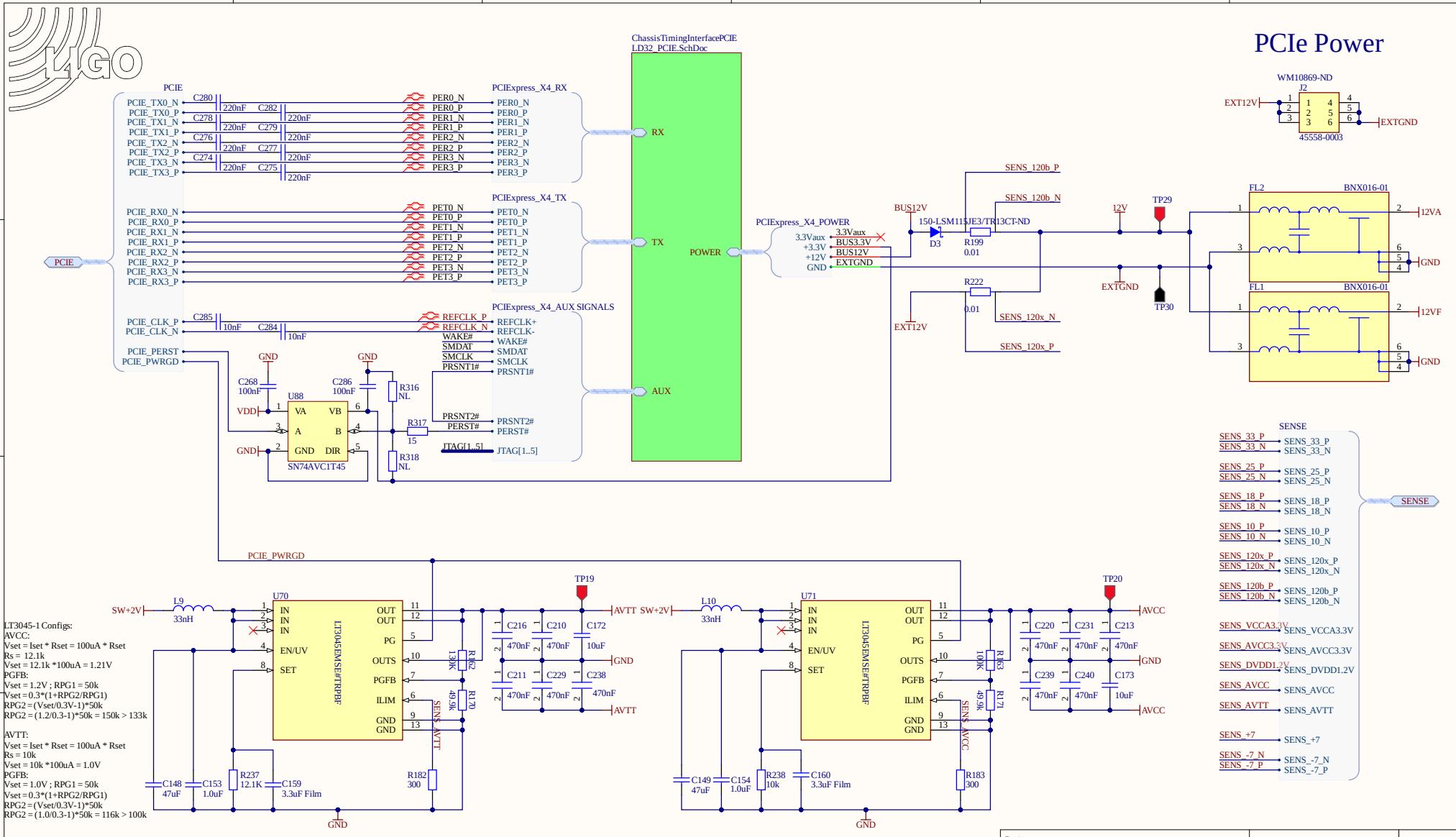
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM
VREG = 5.1V Linear from FPGA Power

PCIe
AVTT = 1.2V
AVCC = 1.0V

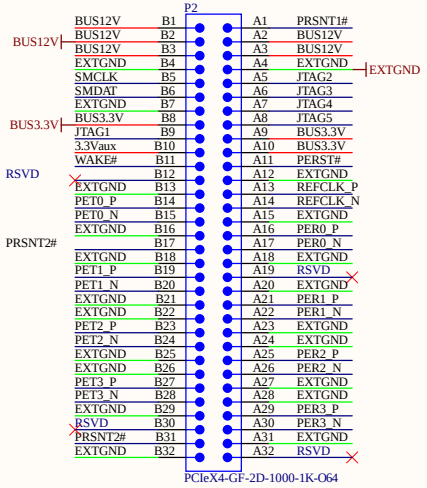
Parts Checked for =Value and Consistency

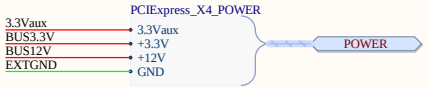
Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *Front End*			
Size: B	DCC D2200368	Rev: 2	
Date: 1/28/2025 Time: 10:43:50 AM		Sheet: 15 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FrontEnd.SchDoc			

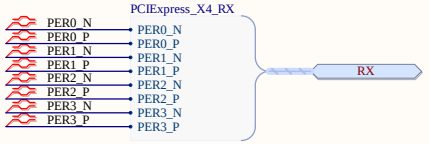
PCIe Power

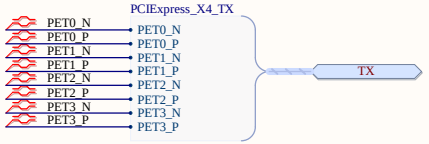

ChassisTimingInterfacePCIE
LD32_PCIE.SchDoc
PCIE
PCIExpress_X4_RX
PCIExpress_X4_TX
PCIExpress_X4_AUX SIGNALS
PCIExpress_X4_POWER
RX
TX
AUX
POWER
WM10869-ND
J2
45558-0003
EXT12V
EXTGND
BUS12V
150-LSM115JE3/TR13CT-ND
D3
R199
0.01
R222
SENS_120b_P
SENS_120b_N
SENS_120x_N
SENS_120x_P
TP29
TP30
FL2
FL1
BNX016-01
12VA
12VF
GND
SENSE
SN74AVC1T45
U88
PCIE_PWRGD
PCIE_PERST
U70
U71
LT3045EMSE#TRPBF
SW+2V
AVTT
AVCC
TP19
TP20
L9
L10
33nH
LT3045-1 Configs:
AVCC:
Vset = Iset * Rset = 100uA * Rset
Rs = 12.1k
Vset = 12.1k *100uA = 1.21V
PGFB:
Vset = 1.2V ; RPG1 = 50k
Vset = 0.3*(1+RPG2/RPG1)
RPG2 = (Vset/0.3V-1)*50k
RPG2 = (1.2/0.3-1)*50k = 150k > 133k
AVTT:
Vset = Iset * Rset = 100uA * Rset
Rs = 10k
Vset = 10k *100uA = 1.0V
PGFB:
Vset = 1.0V ; RPG1 = 50k
Vset = 0.3*(1+RPG2/RPG1)
RPG2 = (Vset/0.3V-1)*50k
RPG2 = (1.0/0.3-1)*50k = 116k > 100k
Parts Checked for =Value and Consistency
0201 parts need to be hand sorted
- Nominal values used, dimensions in mm
- The mounting holes and keep-out areas around them are only required when the I/O bracket is mounted on the card directly
- Component height rule and clearance rule derived from PCI_Express_CEM_r2.0.pdf, Page 84.
- Stackup is not specified in PCI_Express_CEM_r2.0.pdf, nor implemented in this template.
Project LIGO DAC 32
Sheet Title PCIe Interface
Size: B
DCC D2200368
Rev: 2
Date: 1/28/2025
Time: 10:43:50 AM
Sheet: 16 of 17
File: LD32_PCIE_HL.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello, D. Sigg

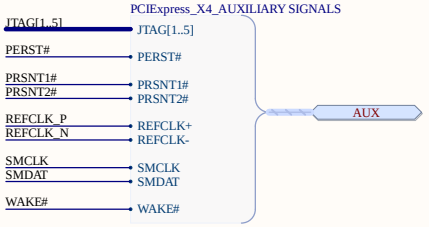
PCIe 4x Slot











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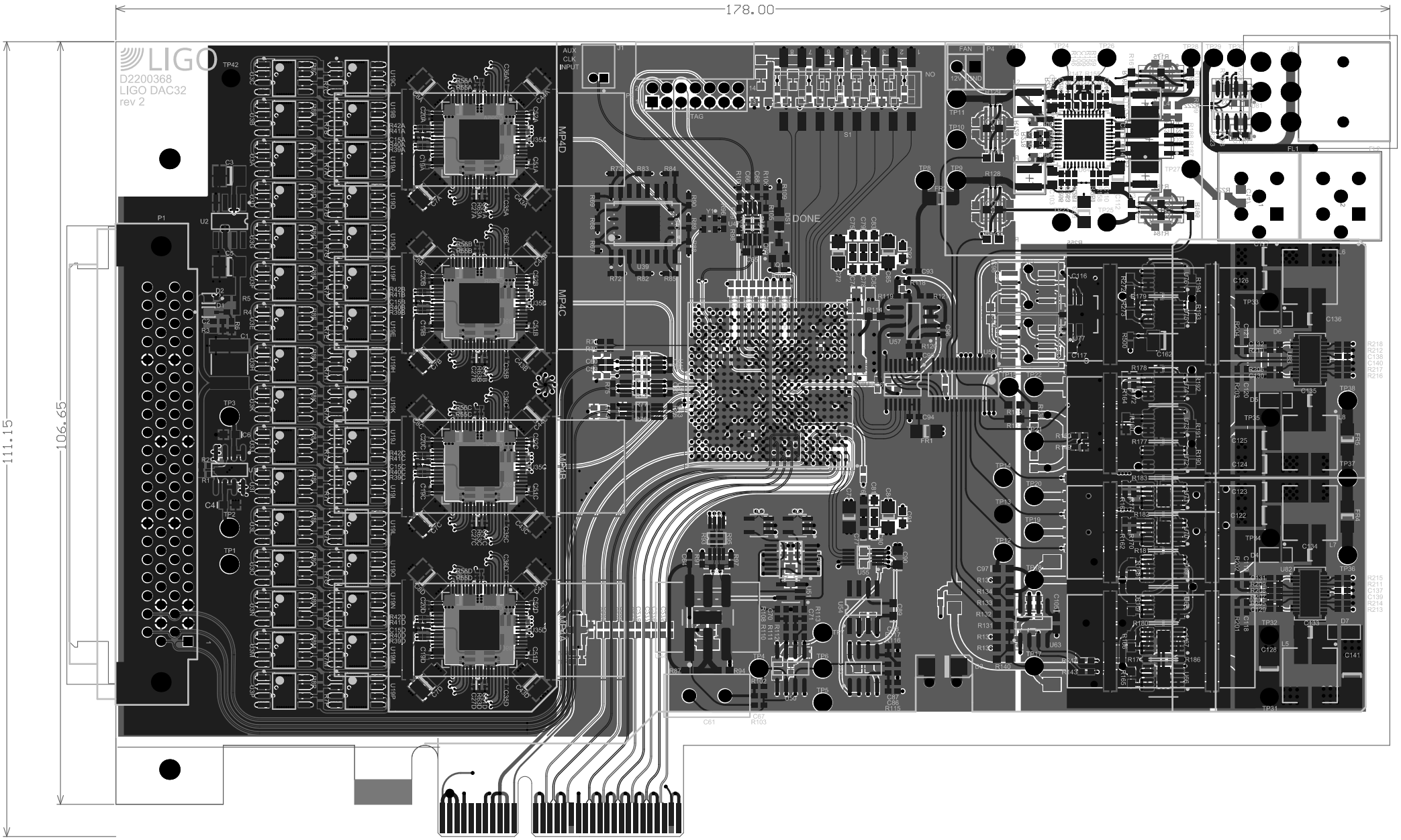
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM
VREG = 5.1V Linear from FPGA Power

PCIe
AVTT = 1.2V
AVCC = 1.0V

Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *PCIe*			
Size: B	DCC D2200368	Rev: 2	
Date: 1/28/2025	Time: 10:43:50 AM	Sheet: 17 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_PCIE.SchDoc			


178.00
111.15
106.65
LIGO
D2200368
LIGO DAC32
rev 2
AUX CLK INPUT
MP4D
MP4C
MP4B
MP4A
TAG
DONE
FAN
12V
GND
NO