LIGO Converter Design
Basic Features

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Some Meeting
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Converter R&D Direction

- Long R&D Goal:
  - Buy or make a PCIe board that could replace the common mode servos
  - Something like FPGA & 4 Inputs & 2 Outputs & >1MHz sampling
  - All signal processing for servo network in FPGA
  - **Integration with our RTCDS, strive for a similar feel as much as possible**
  - FPGA filters which try to emulate current filter module, use foton for design
  - Data acquisition and excitation channels through PCIe
- Short term need:
  - Replace failing 18-bit DAC (GS 20-bit DAC very expensive, i.e., ~$7000 for 8 channels)
  - Design a prototype 16-32 channel DAC board
- 32 channel ADC board?
- Direct RF down-conversion using ADCs with GHz sampling?
  - Requires phase locked RF demodulation/modulation signals

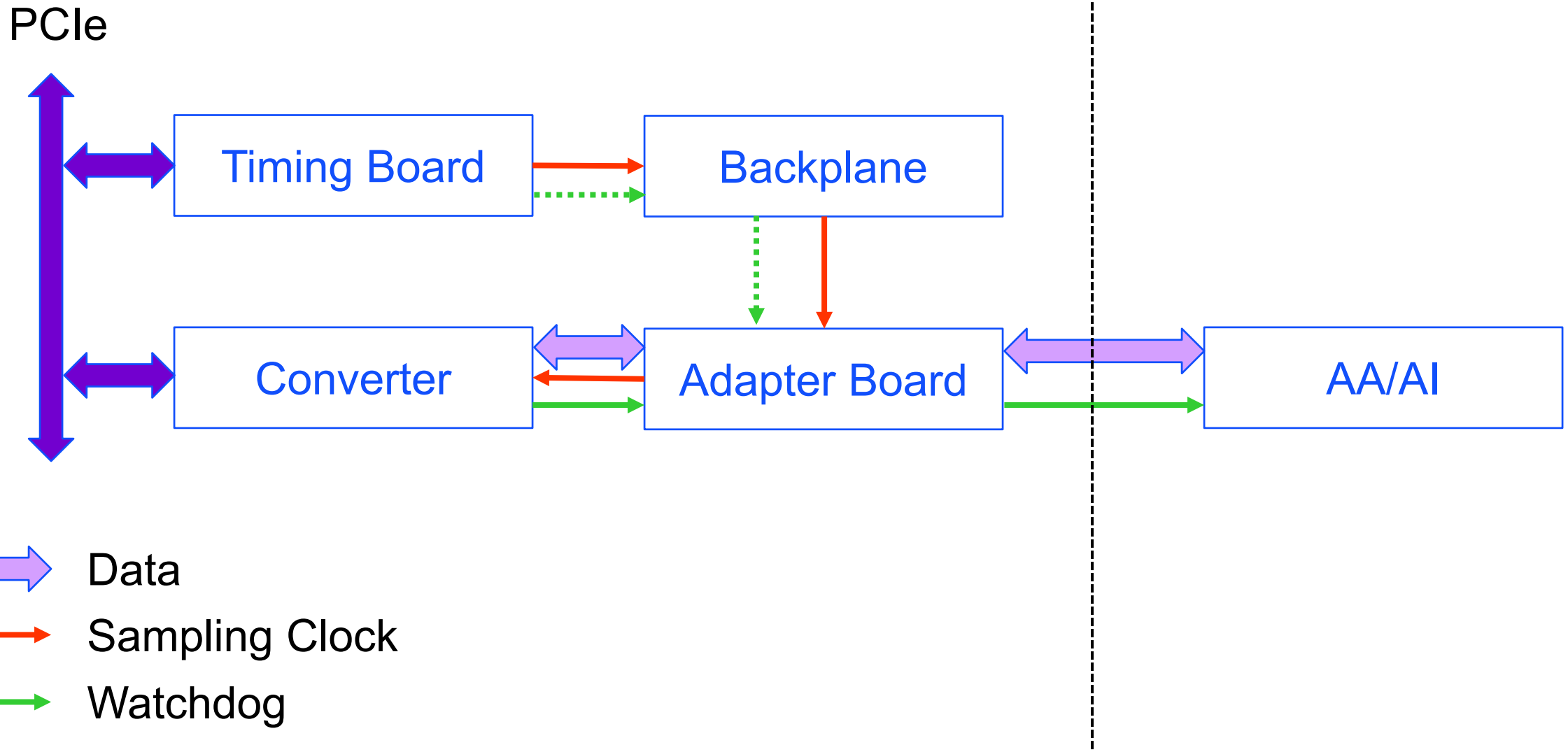
Status

- DAC Daughter Board
  - Partially successful (issues with power supply)
  - FPGA code to send sine waves to DAC completed and tested
  - FPGA code for IIR filters completed and simulated
  - FPGA code to interface PCIe completed (not tested, but mostly copied from Xilinx)
    - Front-end driver required!
  - Analog notch filter for testing completed
  - Some promising noise measurements but incomplete
  - DC accuracy not able to assess
- DAC Prototype Design
  - Mostly done
  - Design checks ongoing

Schedule

- DAC Board
  - Prototype by March (design is close to ready)
  - Testing April- July
  - First article by August/September (if needed)
- ADC Board
  - Design starting soon-ish
  - Prototype by August
  - Testing September-November
  - First article by December (if needed)
- Fast Servo Board: Start design next year
- Costs:
  - Each prototype/1st article run: $5000-$7000
  - Required this year: $15k to $25k
  - Estimated final costs: ~$1200-$1800 in quantity of 100 (16/32 channels)

Front-End Chassis



Clocking Improvements

- Use timing distribution signal as input clock
  - Local 2^{26} Hz VCXO is locked to input clock
  - Converter knows GPS time
- Allows for time stamped data transfers
  - Watchdog: Outputs can be stopped when no valid data is received
- No special startup synchronization procedure required
  - Converter is always synchronized to GPS (currently clock must start at 1sec boundary)
- Clock rate is set by the converter and not by the timing board
  - Only 2^{n} Hz conversion rates available, so

Signal Processing Support

- Board will use a modern FPGA (e.g., Artix-7/Artix Ultrascale)
  - Support for PCIe 2.1/3.0
  - Support for 4x possible (current Adnaco boards only supports V2.1 at 1x)
- FPGA is large enough to support high precision IIR Filters
  - Up and down sampling filters in FPGA
  - No requirement to increase IOP rate beyond required rate for servos
  - Could implement down-conversion as well
- Converter runs at optimal rate
  - Usually faster than required sampling rate
- Include support for sampling rate > transfer rate
  - Multiple samples per channel per DMA transfer
- DMA is double buffered to reduce IOP timing constraints

Converter Technology

- First prototype is 32 channel DAC
  - Price estimate ~$1500/card in quantities of 100 (~$2000/card in qty 10)
  - Channel bonding possible to improve SNR, i.e., 16 channel or 8 channel
- Uses ΣΔ-Technology
  - Tend to have better linearity than other technologies
  - Preferred by audiophiles (10Hz to >20kHz)
- Delays
  - Old ΣΔ-converters implemented FIR filters for up-sampling which introduced long delays
  - New ΣΔ-converters allow to implement filters externally → use IIR filters on FPGA
  - New ΣΔ-converters are much faster, so sample delays matter much less
- Improvement output stage of ΣΔ-DACs
  - Much lower resistance in current drive reduces flicker noise
  - Full differential design improves DC accuracy, but is it good enough?