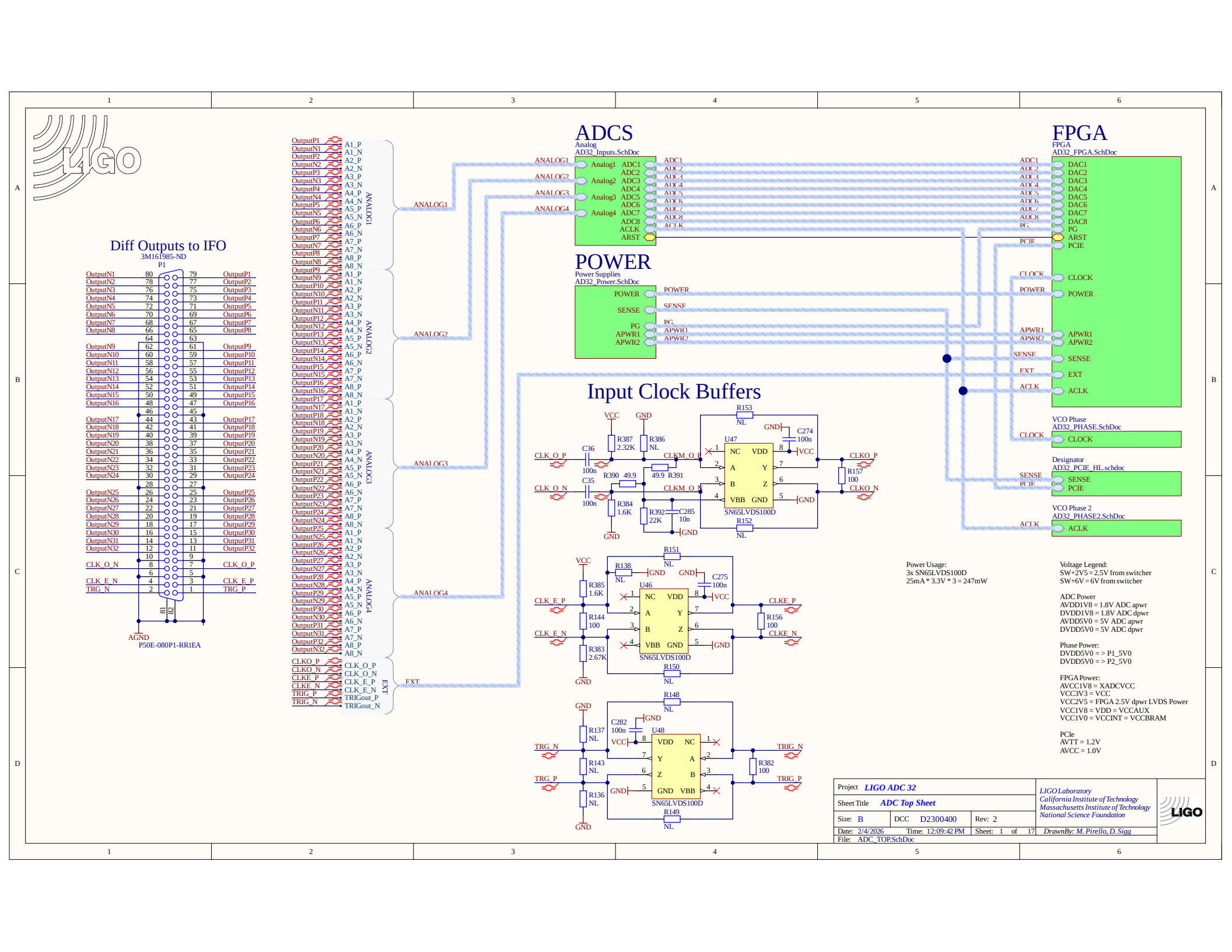
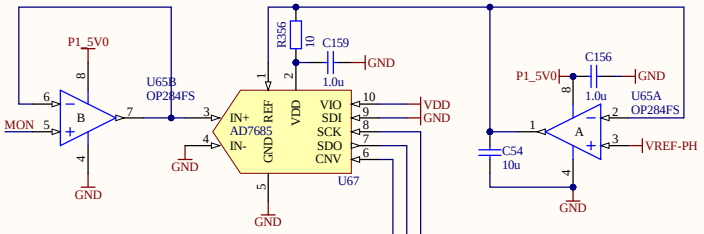

Diff Outputs to IFO
3M161985-ND
P1
P50E-080P1-RR1EA
AGND
ADCS
Analog
AD32_Inputs.SchDoc
POWER
Power Supplies
AD32_Power.SchDoc
FPGA
FPGA
AD32_FPGA.SchDoc
Input Clock Buffers
VCO Phase
AD32_PHASE.SchDoc
Designator
AD32_PCIE_HL.schdoc
VCO Phase 2
AD32_PHASE2.SchDoc
SN65LVDS100D
Power Usage:
3x SN65LVDS100D
25mA * 3.3V * 3 = 247mW
Voltage Legend:
SW+2V5 = 2.5V from switcher
SW+6V = 6V from switcher
ADC Power
AVDD1V8 = 1.8V ADC apwr
DVDD1V8 = 1.8V ADC dpwr
AVDD5V0 = 5V ADC apwr
DVDD5V0 = 5V ADC dpwr
Phase Power:
DVDD5V0 = > P1_5V0
DVDD5V0 = > P2_5V0
FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM
PCIe
AVTT = 1.2V
AVCC = 1.0V
Project LIGO ADC 32
Sheet Title ADC Top Sheet
Size: B
DCC D2300400
Rev: 2
Date: 2/4/2026
Time: 12:09:42 PM
Sheet: 1 of 17
File: ADC_TOP.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello, D. Sigg

Control Voltage Monitor



Power Usage (343mW)
AD7685 2.5V*50uA = <1mW
2x OP284FS 20mA * 5V * 2 = 200mW
2x SN74LVC74APWR 10uA*3.3V*2 = <1mW
SN74LVC1G00 10uA * 3.3V = >1mW
2x SN65LVDT2 8mA * 3.3V * 2 = 53mW
SN65LVDS100D 25mA * 3.3V = 82.5mW
ADR4525 950uA * 5V = 4.75mW
OCXO = n/a

Voltage Legend:
SW+2V5 = 2.5V from switcher
SW+6V = 6V from switcher

ADC Power
AVDD1V8 = 1.8V ADC apwr
DVDD1V8 = 1.8V ADC dpwr
AVDD5V0 = 5V ADC apwr
DVDD5V0 = 5V ADC dpwr

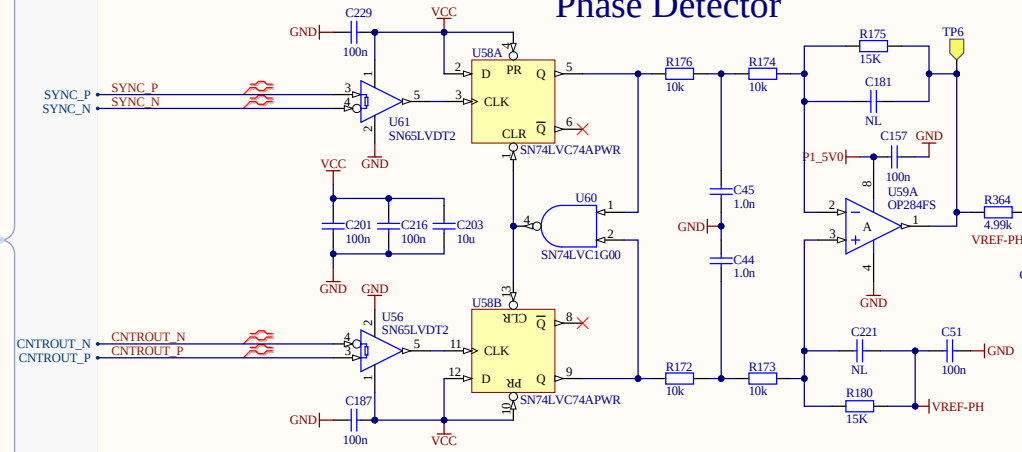
Phase Power:
DVDD5V0 = > P1_5V0
DVDD5V0 = > P2_5V0

FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM

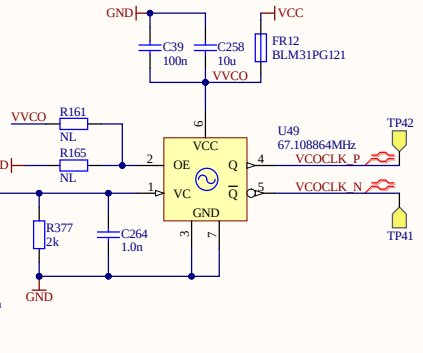
PCIe
AVTT = 1.2V
AVCC = 1.0V

PHASE1
ACNV
AIN
ACLK

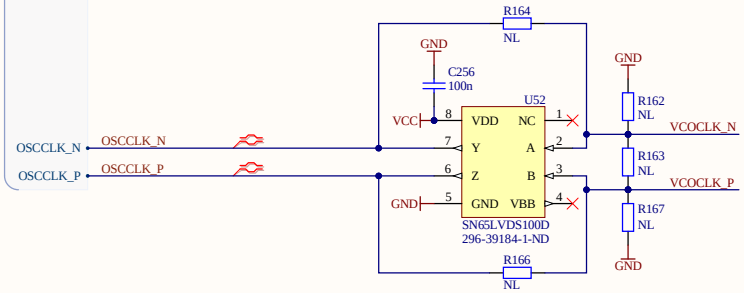
Phase Detector



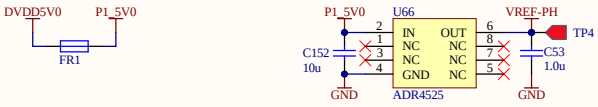
Vectron VCO



Optional LVPECL-LVDS Translator

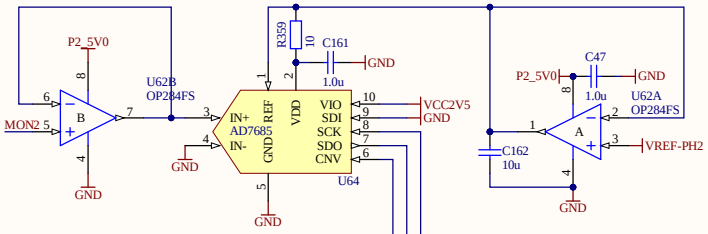


2.5V Reference



Project	*LIGO ADC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*VCO & Phase Detector*		
Size: B	DCC D2300400	Rev: 2	
Date: 2/4/2026	Time: 12:09:42 PM	Sheet: 2 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: AD32_PHASE.SchDoc			

Control Voltage Monitor



PHASE2
ACNVF ACNV
AINF AIN
ACLKF ACLK

Power Usage (350mW)
AD7685 2.5V*50uA = <1mW
2x OP284FS 20mA * 5V * 2 = 200mW
2x SN74LVC74APWR 10uA*3.3V*2 = <1mW
SN74LVC1G00 10uA * 3.3V = >1mW
2x SN65LVDT2 8mA * 3.3V * 2 = 53mW
ADR4525 950uA * 5V = 4.75mW
OCXO = n/a
8P34S1102 40mA * 1.8V = 90mW

Voltage Legend:
SW+2V5 = 2.5V from switcher
SW+6V = 6V from switcher

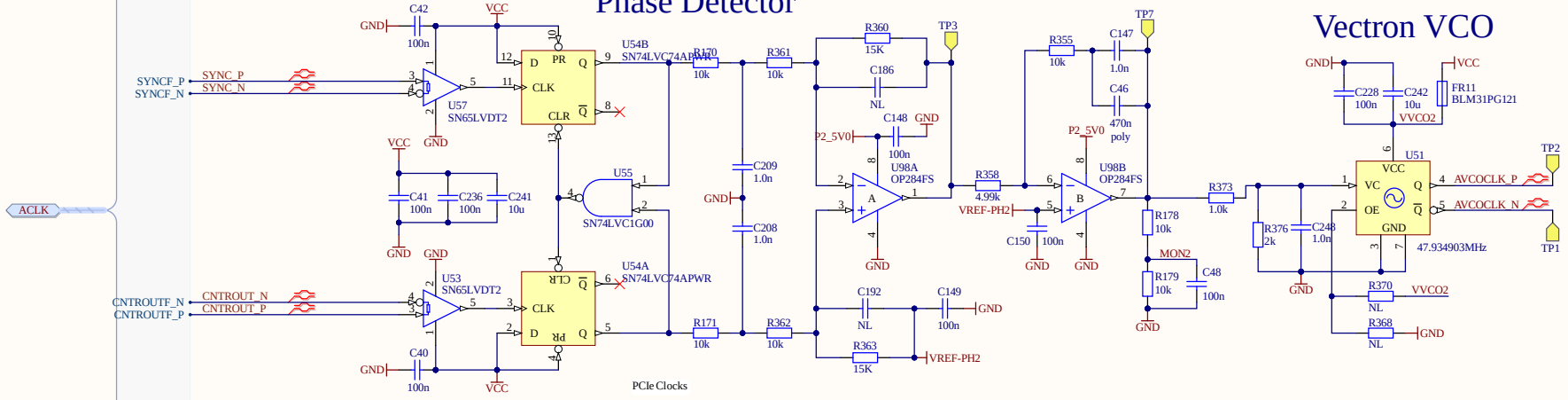
ADC Power
AVDD1V8 = 1.8V ADC apwr
DVDD1V8 = 1.8V ADC dpwr
AVDD5V0 = 5V ADC apwr
DVDD5V0 = 5V ADC dpwr

Phase Power:
DVDD5V0 = > P1_5V0
DVDD5V0 = > P2_5V0

FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM

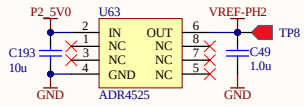
PCIe
AVTT = 1.2V
AVCC = 1.0V

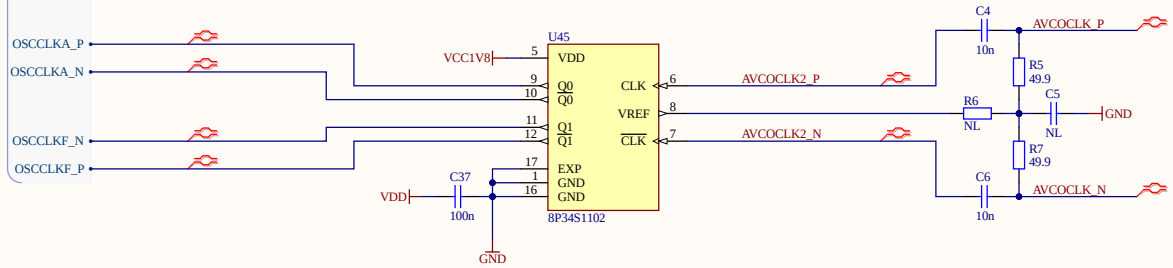
Phase Detector



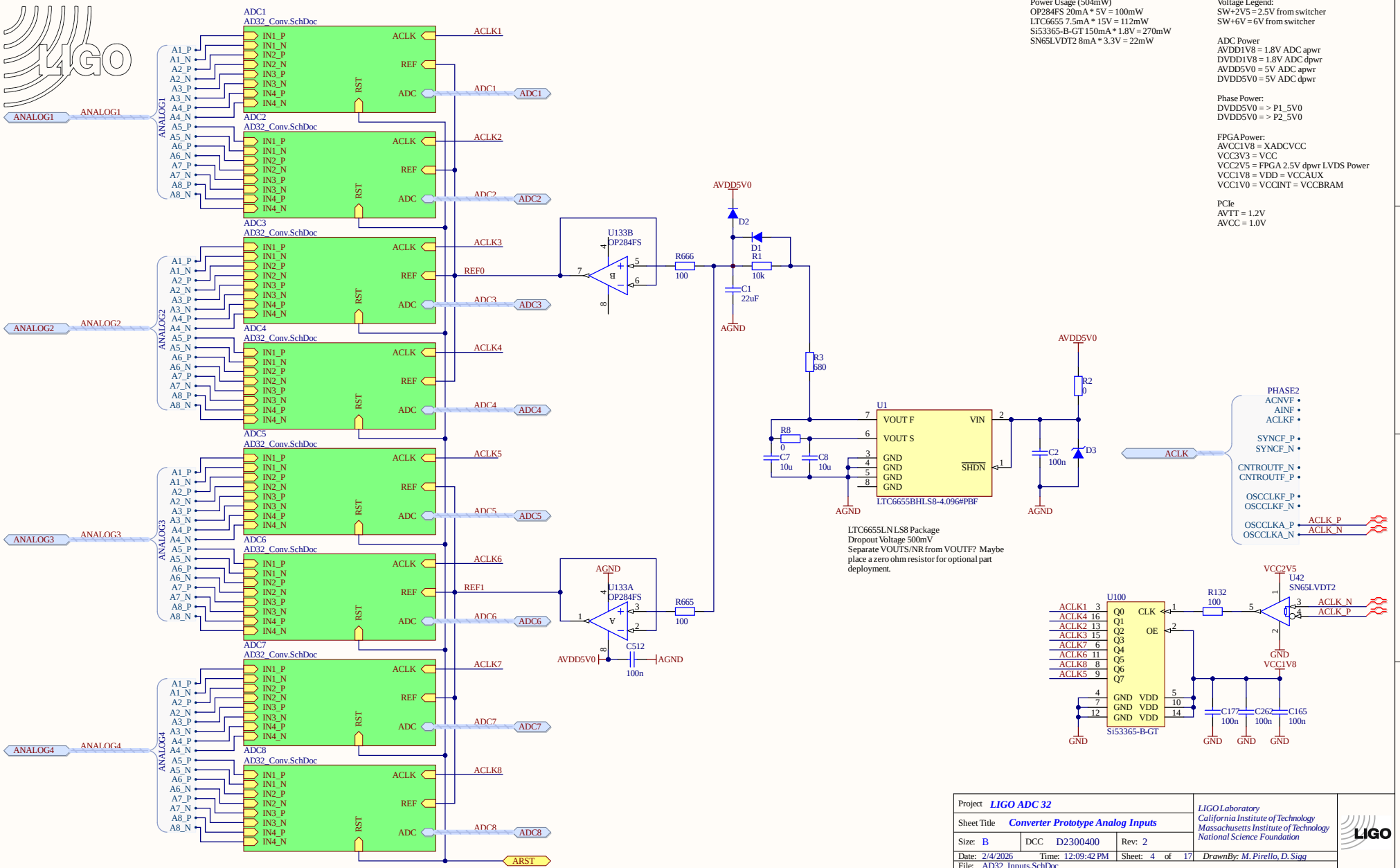
Vectron VCO

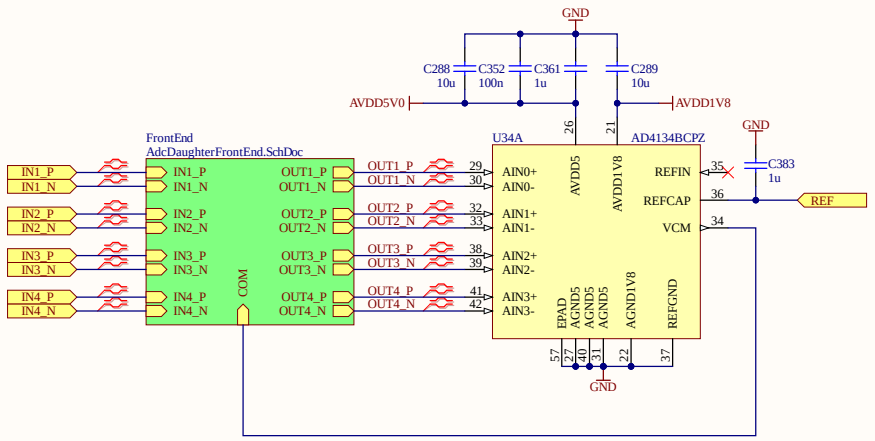
2.5V Reference

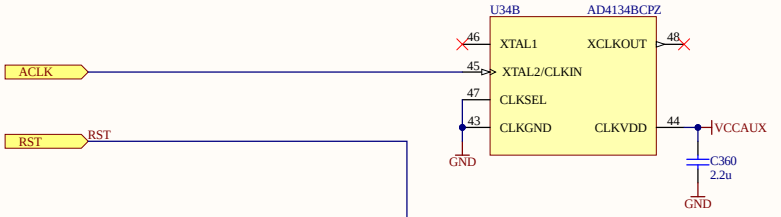


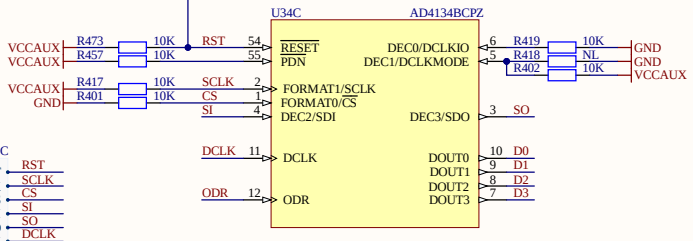


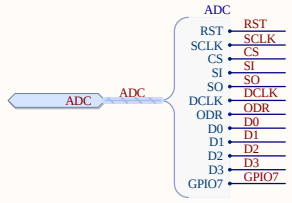
Project	LIGO ADC 32		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation
Sheet Title	VCO & Phase Detector		
Size: B	DCC D2300400	Rev: 2	
Date: 2/4/2026	Time: 12:09:42 PM	Sheet: 3 of 17	DrawnBy: M. Pirello, D. Sigg
File: AD32_PHASE2.SchDoc			

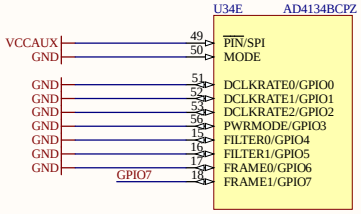

ADC1
AD32_Conv.SchDoc
ADC2
ADC3
ADC4
ADC5
ADC6
ADC7
ADC8
IN1_P
IN1_N
IN2_P
IN2_N
IN3_P
IN3_N
IN4_P
IN4_N
ACLK
REF
ADC
RST
ANALOG1
ANALOG2
ANALOG3
ANALOG4
A1_P
A1_N
A2_P
A2_N
A3_P
A3_N
A4_P
A4_N
A5_P
A5_N
A6_P
A6_N
A7_P
A7_N
A8_P
A8_N
ACLK1
ACLK2
ACLK3
ACLK4
ACLK5
ACLK6
ACLK7
ACLK8
ADC1
ADC2
ADC3
ADC4
ADC5
ADC6
ADC7
ADC8
ARST
REF0
REF1
U133B
OP284FS
U133A
R666
R665
100
AVDD5V0
D2
D1
R1
10k
C1
22uF
AGND
R3
680
R8
0
C7
10u
C8
10u
U1
VOUT F
VOUT S
VIN
GND
SHDN
LTC6655BHLS8-4.096#PBF
R2
0
D3
C2
100n
C512
100n
Power Usage (504mW)
OP284FS 20mA * 5V = 100mW
LTC6655 7.5mA * 15V = 112mW
Si53365-B-GT 150mA * 1.8V = 270mW
SN65LVDT2 8mA * 3.3V = 22mW
Voltage Legend:
SW+2V5 = 2.5V from switcher
SW+6V = 6V from switcher
ADC Power
AVDD1V8 = 1.8V ADC apwr
DVDD1V8 = 1.8V ADC dpwr
AVDD5V0 = 5V ADC apwr
DVDD5V0 = 5V ADC dpwr
Phase Power:
DVDD5V0 = > P1_5V0
DVDD5V0 = > P2_5V0
FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM
PCIe
AVTT = 1.2V
AVCC = 1.0V
LTC6655LN LS8 Package
Dropout Voltage 500mV
Separate VOUTS/NR from VOUTF? Maybe place a zero ohm resistor for optional part deployment.
PHASE2
ACNVF
AINF
ACLKF
SYNCF_P
SYNCF_N
CNTROUTF_N
CNTROUTF_P
OSCCLKF_P
OSCCLKF_N
OSCCLKA_P
OSCCLKA_N
ACLK_P
ACLK_N
VCC2V5
U42
SN65LVDT2
U100
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
CLK
OE
GND
VDD
Si53365-B-GT
R132
100
VCC1V8
C177
100n
C262
100n
C165
100n
Project LIGO ADC 32
Sheet Title Converter Prototype Analog Inputs
Size: B
DCC D2300400
Rev: 2
Date: 2/4/2026
Time: 12:09:42 PM
Sheet: 4 of 17
File: AD32_Inputs.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello, D. Sigg

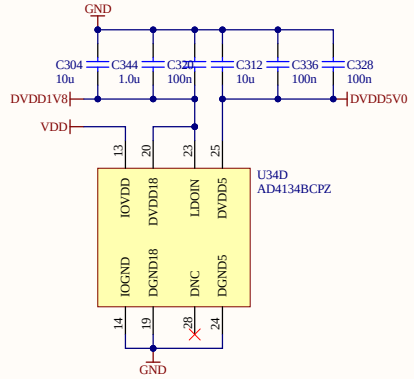












ADC INFORMATION
AD4134BCPZ is compatible with prior version AD7134BCPZ
Max Current Requirements, there are 8 chips
AVDD5 - 11mA * 8 = 88mA Max
DVDD5 - 44.8mA * 8 = 358mA
AVDD1V8 - 81mA * 8 = 648mA
DVDD1V8 - 105.5mA = 844mA
IOVDD - 3.17mA * 8 = 25.4mA
CLKVDD - 3.53mA * 8 = 28.3mA

Supplies
AVDD5 needs one
DVDD5 needs one
AVDD1V8 needs two
DVDD1V8 needs two

Power Usage (3.2266W)
AVDD5 = 88mA * 5V = 440mW
DVDD5 = 358mA * 5V = 1.8W
AVDD1V8 = 648mA * 1.8V = 1.17W
DVDD1V8 = 844mA * 1.8V = 1.52W
IOVDD = 25.4mA * 1.8V = 45.7mW
CLKVDD 28.3mA * 1.8V = 50.9mW

Voltage Legend:
SW+2V5 = 2.5V from switcher
SW+6V = 6V from switcher

ADC Power
AVDD1V8 = 1.8V ADC apwr
DVDD1V8 = 1.8V ADC dpwr
AVDD5V0 = 5V ADC apwr
DVDD5V0 = 5V ADC dpwr

Phase Power:
DVDD5V0 = > P1_5V0
DVDD5V0 = > P2_5V0

FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM

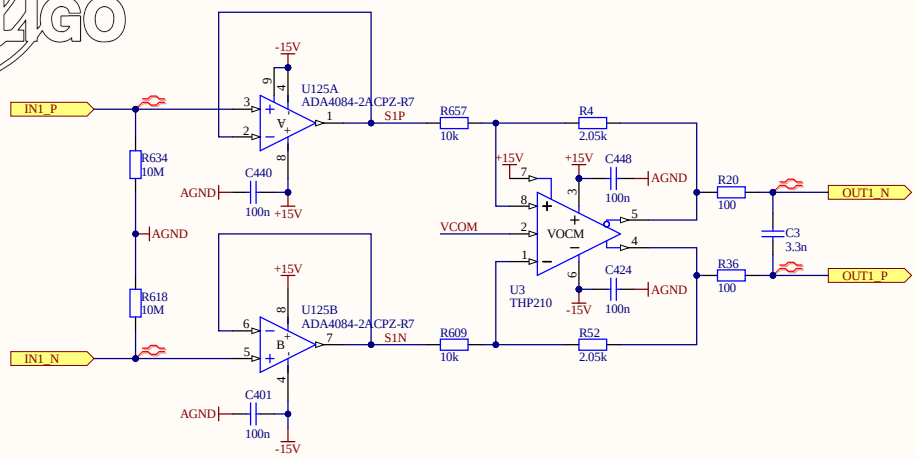
PCIe
AVTT = 1.2V
AVCC = 1.0V

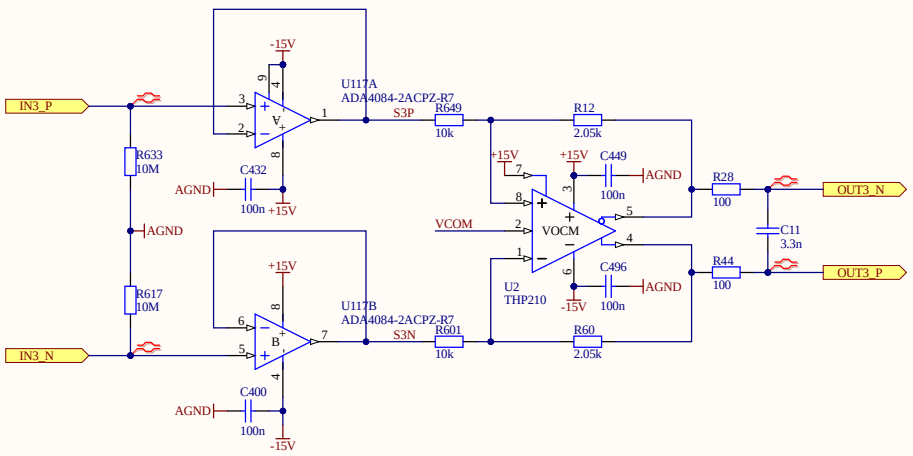
Power Dissipation
12.5V in 4.096V Reference, drop of 8.4V
5.25mA current per ADC or 42mA total
400mW total, 200mW per OPAMP

Max Output Current of OP284 is 10mA at +/-15V supply.

Required input current of each ADC is 5.25mA, probably an issue here.

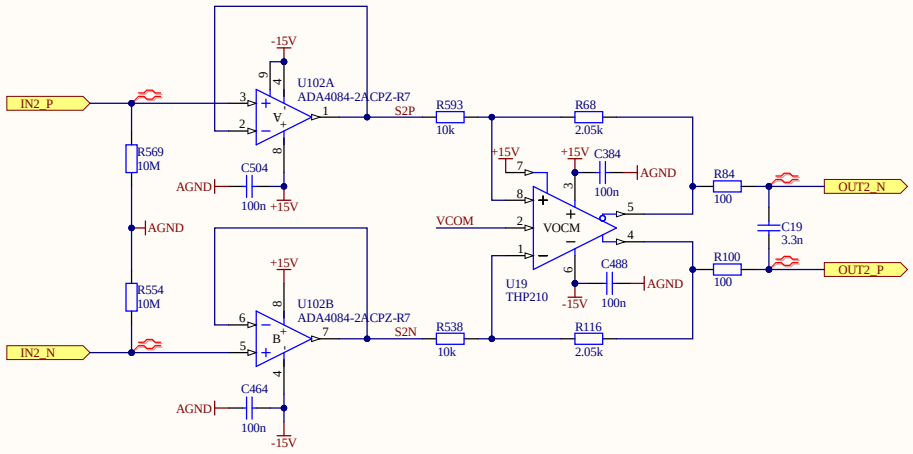
Project	LIGO ADC 32		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation
Sheet Title	Converter Prototype ADC		
Size: B	DCC D2300400	Rev: 2	
Date: 2/4/2026	Time: 12:09:42 PM	Sheet: 5 of 17	DrawnBy: M. Pirello, D. Sigg
File: AD32_Conv.SchDoc			

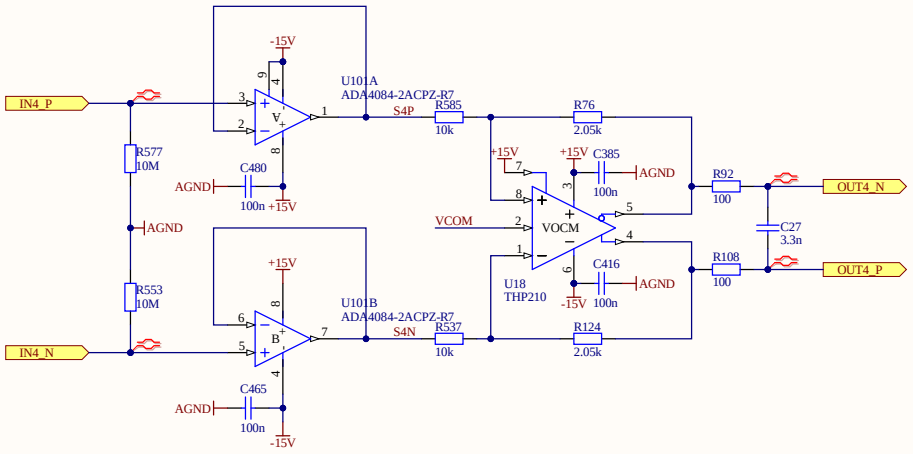




Power Usage ()
OPA1612AID(32) 23V*3.6mA*2*32 = 5.15W
THP210 (32) 23V*950uA*32 = 670mW

ADA4084-2ACPZ-R7(32) 23V*2*32*0.565mA=831mW

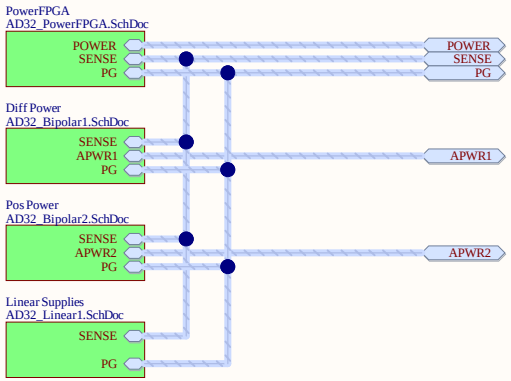




COM VCOM

Project *LIGO ADC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *Converter ADC Front End*			
Size: B	DCC D2300400	Rev: 2	
Date: 2/4/2026 Time: 12:09:42 PM		Sheet: 6 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: AdcDaughterFrontEnd.SchDoc			

Power Top Sheet



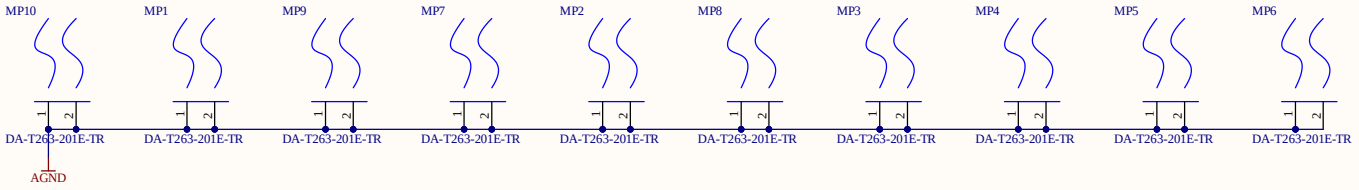
Voltage Legend:
SW+2V5 = 2.5V from switcher
SW+6V = 6V from switcher

ADC Power
AVDD1V8 = 1.8V ADC apwr
DVDD1V8 = 1.8V ADC dpwr
AVDD5V0 = 5V ADC apwr
DVDD5V0 = 5V ADC dpwr

Phase Power:
DVDD5V0 = > P1_5V0
DVDD5V0 = > P2_5V0

FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM

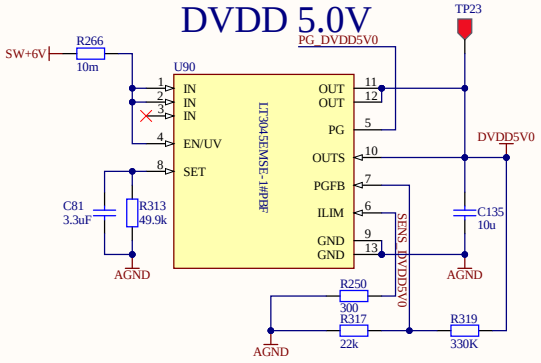
PCIe
AVTT = 1.2V
AVCC = 1.0V



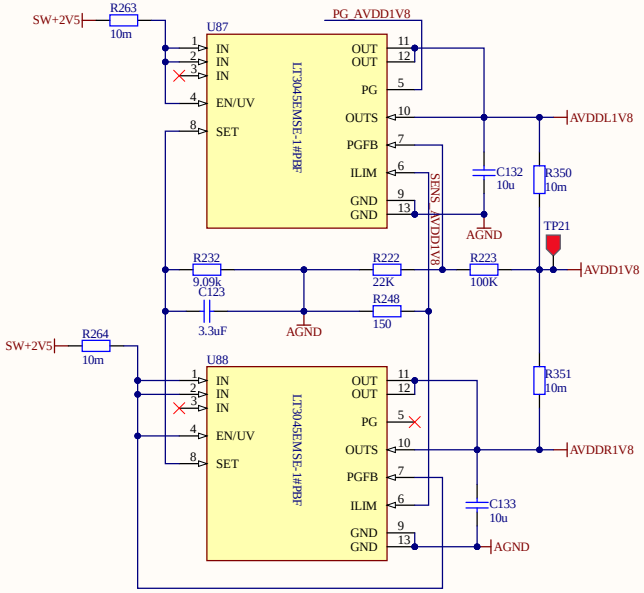
Project *LIGO ADC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *Power Top*			
Size: B	DCC D2300400	Rev: 2	
Date: 2/4/2026 Time: 12:09:42 PM		Sheet: 7 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: AD32_Power.SchDoc			

ADC Linear Power Supplies

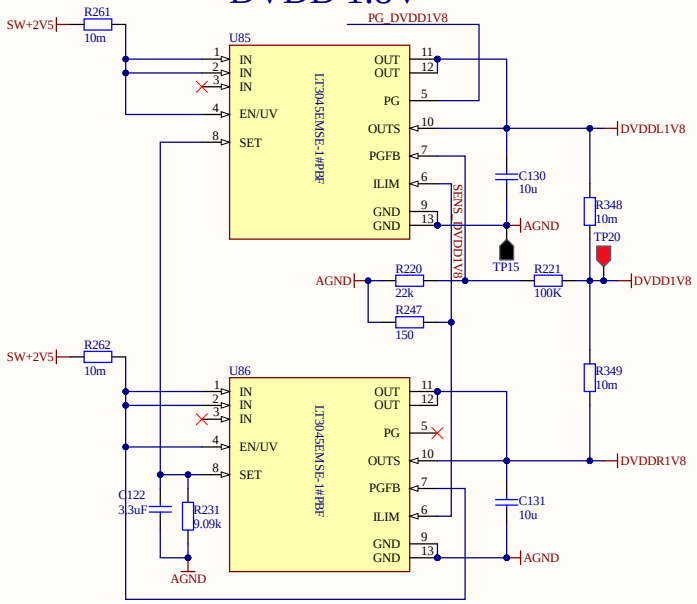
DVDD 5.0V



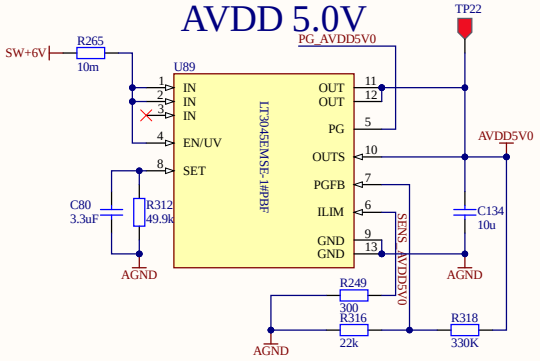
AVDD 1.8V



DVDD 1.8V



AVDD 5.0V



SENSE

- SENS_33_P → SENS_33_P
- SENS_33_N → SENS_33_N
- SENS_25_P → SENS_25_P
- SENS_25_N → SENS_25_N
- SENS_18_P → SENS_18_P
- SENS_18_N → SENS_18_N
- SENS_10_P → SENS_10_P
- SENS_10_N → SENS_10_N
- SENS_120x_P → SENS_120x_P
- SENS_120x_N → SENS_120x_N
- SENS_120b_P → SENS_120b_P
- SENS_120b_N → SENS_120b_N
- SENS_DVDD1V8 → SENS_DVDD1V8
- SENS_DVDD5V0 → SENS_DVDD5V0
- SENS_AVDD1V8 → SENS_AVDD1V8
- SENS_AVDD5V0 → SENS_AVDD5V0
- SENS_AVCC → SENS_AVCC
- SENS_AVTT → SENS_AVTT
- SENS_+15
- SENS_-15
- SENS_-15_N
- SENS_-15_P

→ SENSE

Voltage Legend:
SW+2V5 = 2.5V from switcher
SW+6V = 6V from switcher

ADC Power
AVDD1V8 = 1.8V ADC apwr
DVDD1V8 = 1.8V ADC dpwr
AVDD5V0 = 5V ADC apwr
DVDD5V0 = 5V ADC dpwr

Phase Power:
DVDD5V0 = > P1_5V0
DVDD5V0 = > P2_5V0

FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM

PCIe
AVTT = 1.2V
AVCC = 1.0V

POWER GOOD

- PG_AVDD1V8 → PG_AVDD1V8
- PG_AVDD5V0 → PG_AVDD5V0
- PG_DVDD1V8 → PG_DVDD1V8
- PG_DVDD5V0 → PG_DVDD5V0
- PG_SW+2V5 → PG_SW+2.5V
- PG_SW+6V → PG_SW+6V
- PWRGOOD → PG_FPGA
- PG_SW+16V → PG_SW+16V
- PG_SW-16V → PG_SW-16V
- PG-15V → PG_L-15V
- PG+15V → PG_L+15V

→ PG

LT3045-1 Configs:
VCC5V0
Vset = Iset * Rset = 100uA * Rset
Rs = 50k
Vset = 50k *100uA = 5.0V
PGFB:
Vset = 5.0V ; RPG1 = 22k
5.0V = 0.3V*(1+RPG2/22k)
(5.0V/0.3V-1)*22k=RPG2
RPG2 < 345k

LT3045-1 Configs:
VDD1V8:
Vset = Iset * Rset = 100uA * Rset
Rs = 9k * 2 (two supplies)
Vset = 9k*2*100uA = 1.8V
PGFB:
Vset = 1.8V ; RPG1 = 22k
1.8V = 0.3V*(1+RPG2/22k)
(1.8V/0.3V-1)*22k=RPG2
RPG2 < 110k

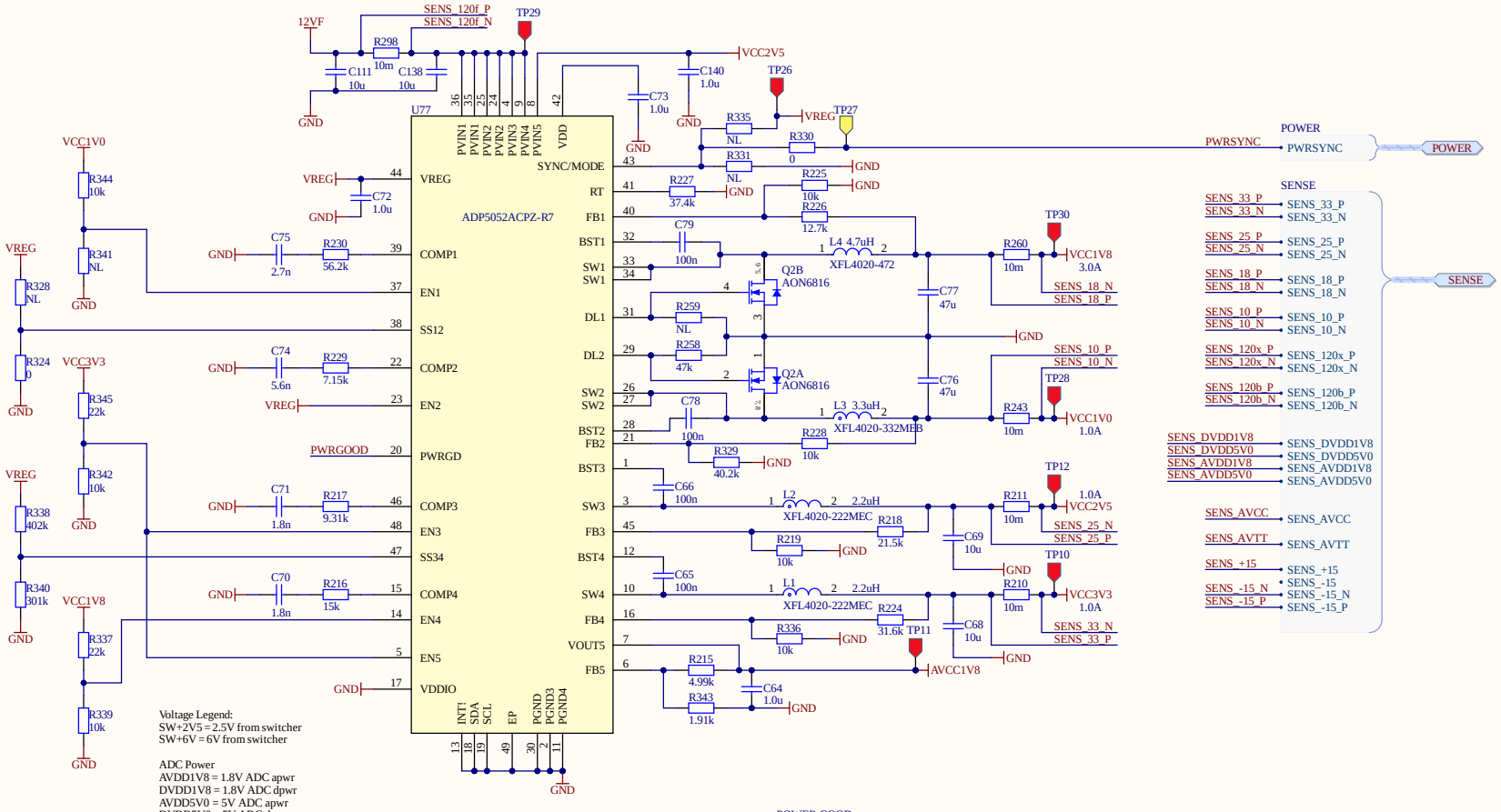
Project	*LIGO ADC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Linear Supplies*		
Size: B	DCC D2300400	Rev: 2	
Date: 2/4/2026	Time: 12:09:42 PM	Sheet: 8 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: AD32_Linear1.SchDoc			

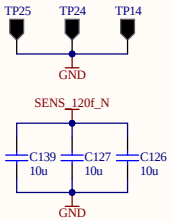
Switched FPGA Power

ADP505x Configs
FB1 - 1.8V 12.7k, 10k, 4.7uH
FB2 - 1.0V 10k. 40k, 3.3uH
FB3 - 2.5V 21.5k, 10k, 2.2uH
FB4 - 3.3V 31.6k, 10k, 2.2uH
FB5 - 1.8V 5k, 1.91k

Legend
VCC = 3.3V (digital votlage)
VDD = 1.8V (digital voltage)
VCCINT = 0.95V (fpga internal)
VCCAUX = 1.8V (fpga internal)
VCCADC = 1.8V (ADC ref voltage)
AVCC1V8

Power Up Config
1st - VCC1V0
2nd - VCC1V8
3rd - VCC3V3
4th & 5th VCC2V5 & AVCC1V8





VCC Bridge

VDD Bridge

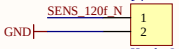
Voltage Legend:
SW+2V5 = 2.5V from switcher
SW+6V = 6V from switcher

ADC Power
AVDD1V8 = 1.8V ADC apwr
DVDD1V8 = 1.8V ADC dpwr
AVDD5V0 = 5V ADC apwr
DVDD5V0 = 5V ADC dpwr

Phase Power:
DVDD5V0 = > P1_5V0
DVDD5V0 = > P2_5V0

FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM

PCIe
AVTT = 1.2V
AVCC = 1.0V



POWER GOOD
PG_AVDD1V8
PG_AVDD5V0
PG_DVDD1V8
PG_DVDD5V0
PG_SW+2V5
PG_SW+6V
PWRGOOD
PG_SW+16V
PG_SW-16V
PG-15V
PG+15V
PG_AVDD1V8
PG_AVDD5V0
PG_DVDD1V8
PG_DVDD5V0
PG_SW+2.5V
PG_SW+6V
PG_FPGA
PG_SW+16V
PG_SW-16V
PG_L-15V
PG_L+15V
PG

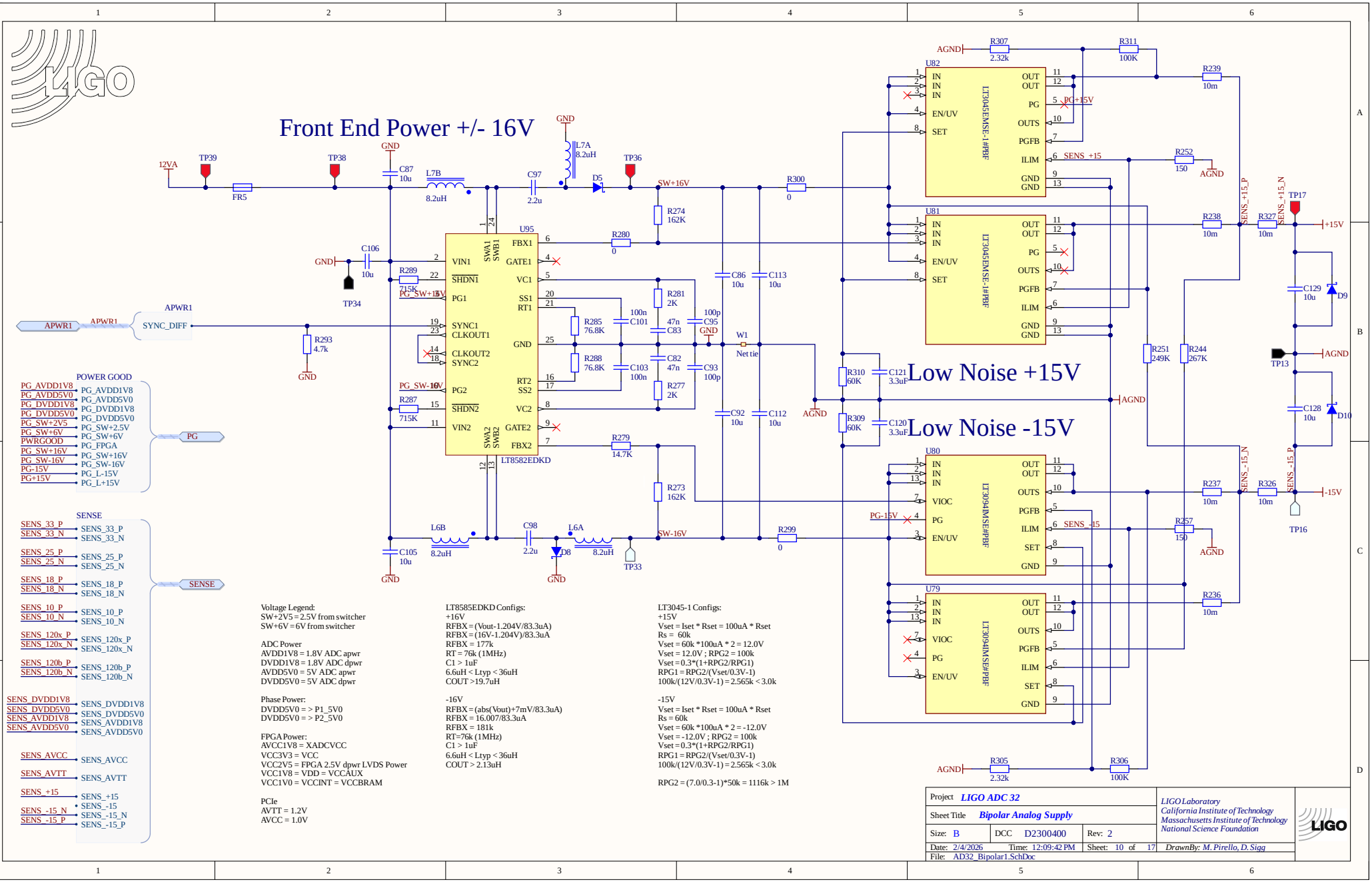
POWER
PWRSYNC
PWRSYNC
POWER

SENSE
SENS_33_P
SENS_33_N
SENS_25_P
SENS_25_N
SENS_18_P
SENS_18_N
SENS_10_P
SENS_10_N
SENS_120x_P
SENS_120x_N
SENS_120b_P
SENS_120b_N
SENS_DVDD1V8
SENS_DVDD5V0
SENS_AVDD1V8
SENS_AVDD5V0
SENS_AVCC
SENS_AVTT
SENS_+15
SENS_-15
SENS_-15_N
SENS_-15_P
SENSE

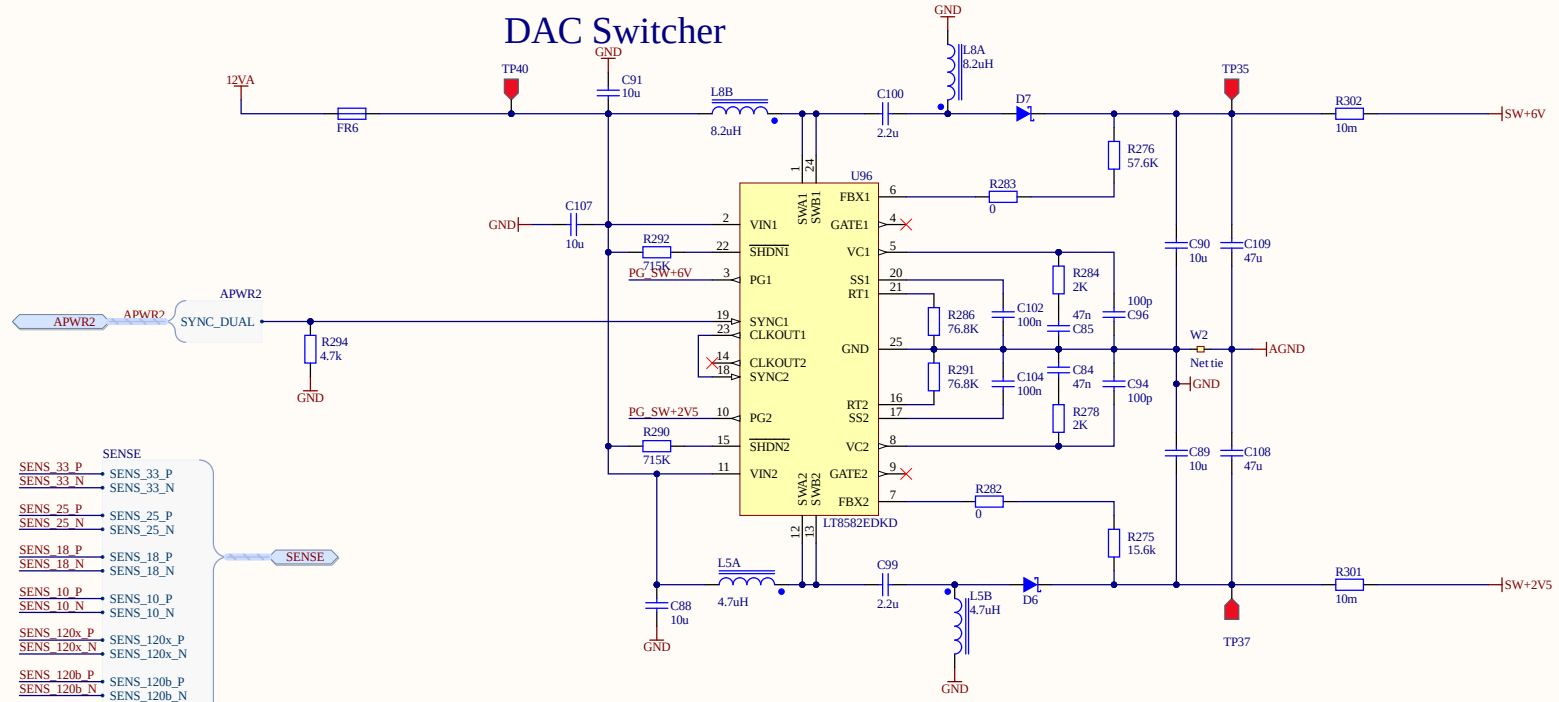
AON6816 (Alpha & Omega)
MOSFET 2N-CH 30V 17A 8DFN (5x6)

SI7904BDN-T1-E3 (Vishay)
MOSFET 2N-CH 20V 6A PPAK 1212

Project	LIGO ADC 32		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation
Sheet Title	FPGA Supply		
Size: B	DCC D2300400	Rev: 2	
Date: 2/4/2026	Time: 12:09:42 PM	Sheet: 9 of 17	DrawnBy: M. Pirello, D. Sigg
File: AD32_PowerFPGA.SchDoc			


Front End Power +/- 16V
Low Noise +15V
Low Noise -15V
12VA
TP39
FR5
TP38
GND
C87 10u
L7B 8.2uH
C97 2.2u
L7A 8.2uH
D5
TP36
SW+16V
R300 0
R274 162K
U95
LT8582EDKD
VIN1
VIN2
SHDN1
SHDN2
PG1
PG2
SYNC1
CLKOUT1
CLKOUT2
SYNC2
SWA1
SWB1
SWA2
SWB2
FBX1
FBX2
GATE1
GATE2
VC1
VC2
SS1
RT1
RT2
GND
R280 0
R279 14.7K
R289 715K
R287 715K
C106 10u
TP34
APWR1
SYNC_DIFF
R293 4.7k
R285 76.8K
R288 76.8K
R281 2K
R277 2K
R273 162K
C101 100n
C103 100n
C83 47n
C82 47n
C95 100p
C93 100p
C86 10u
C113 10u
C92 10u
C112 10u
W1
Net tie
AGND
R310 60K
R309 60K
C121 3.3uF
C120 3.3uF
L6B 8.2uH
C98 2.2u
L6A 8.2uH
D8
TP33
C105 10u
SW-16V
R299 0
U82
LT3045EMSE-1#PBF
U81
LT3045EMSE-1#PBF
U80
LT3094IMSE#PBF
U79
LT3094IMSE#PBF
IN
OUT
EN/UV
SET
PG
OUTS
PGFB
ILIM
VIOC
R307 2.32k
R311 100K
R305 2.32k
R306 100K
R239 10m
R238 10m
R237 10m
R236 10m
R327 10m
R326 10m
R252 150
R257 150
R251 249K
R244 267K
PG+15V
SENS_+15
PG-15V
SENS_-15
SENS_+15_P
SENS_+15_N
SENS_-15_N
SENS_-15_P
TP17
TP13
TP16
+15V
-15V
C129 10u
C128 10u
D9
D10
POWER GOOD
PG_AVDD1V8
PG_AVDD5V0
PG_DVDD1V8
PG_DVDD5V0
PG_SW+2V5
PG_SW+6V
PWRGOOD
PG_SW+16V
PG_SW-16V
PG-15V
PG+15V
PG_AVDD1V8
PG_AVDD5V0
PG_DVDD1V8
PG_DVDD5V0
PG_SW+2.5V
PG_SW+6V
PG_FPGA
PG_SW+16V
PG_SW-16V
PG_L-15V
PG_L+15V
PG
SENSE
SENS_33_P
SENS_33_N
SENS_25_P
SENS_25_N
SENS_18_P
SENS_18_N
SENS_10_P
SENS_10_N
SENS_120x_P
SENS_120x_N
SENS_120b_P
SENS_120b_N
SENS_DVDD1V8
SENS_DVDD5V0
SENS_AVDD1V8
SENS_AVDD5V0
SENS_AVCC
SENS_AVTT
SENS_+15
SENS_-15
SENS_-15_N
SENS_-15_P
Voltage Legend:
SW+2V5 = 2.5V from switcher
SW+6V = 6V from switcher
ADC Power
AVDD1V8 = 1.8V ADC apwr
DVDD1V8 = 1.8V ADC dpwr
AVDD5V0 = 5V ADC apwr
DVDD5V0 = 5V ADC dpwr
Phase Power:
DVDD5V0 = > P1_5V0
DVDD5V0 = > P2_5V0
FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM
PCIe
AVTT = 1.2V
AVCC = 1.0V
LT8585EDKD Configs:
+16V
RFBX = (Vout-1.204V/83.3uA)
RFBX = (16V-1.204V)/83.3uA
RFBX = 177k
RT = 76k (1MHz)
C1 > 1uF
6.6uH < Ltyp < 36uH
COUT >19.7uH
-16V
RFBX = (abs(Vout)+7mV/83.3uA)
RFBX = 16.007/83.3uA
RFBX = 181k
RT=76k (1MHz)
C1 > 1uF
6.6uH < Ltyp < 36uH
COUT > 2.13uH
LT3045-1 Configs:
+15V
Vset = Iset * Rset = 100uA * Rset
Rs = 60k
Vset = 60k *100uA * 2 = 12.0V
Vset = 12.0V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(12V/0.3V-1) = 2.565k < 3.0k
-15V
Vset = Iset * Rset = 100uA * Rset
Rs = 60k
Vset = 60k *100uA * 2 = -12.0V
Vset = -12.0V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(12V/0.3V-1) = 2.565k < 3.0k
RPG2 = (7.0/0.3-1)*50k = 1116k > 1M
Project LIGO ADC 32
Sheet Title Bipolar Analog Supply
Size: B
DCC D2300400
Rev: 2
Date: 2/4/2026
Time: 12:09:42 PM
Sheet: 10 of 17
File: AD32_Bipolar1.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello, D. Sigg

DAC Switcher



SENSE

SENS_33_P — SENS_33_P
SENS_33_N — SENS_33_N
SENS_25_P — SENS_25_P
SENS_25_N — SENS_25_N
SENS_18_P — SENS_18_P
SENS_18_N — SENS_18_N
SENS_10_P — SENS_10_P
SENS_10_N — SENS_10_N
SENS_120x_P — SENS_120x_P
SENS_120x_N — SENS_120x_N
SENS_120b_P — SENS_120b_P
SENS_120b_N — SENS_120b_N
SENS_DVDD1V8 — SENS_DVDD1V8
SENS_DVDD5V0 — SENS_DVDD5V0
SENS_AVDD1V8 — SENS_AVDD1V8
SENS_AVDD5V0 — SENS_AVDD5V0
SENS_AVCC — SENS_AVCC
SENS_AVTT — SENS_AVTT
SENS_+15
SENS_-15
SENS_-15_N
SENS_-15_P

→ SENSE

POWER GOOD

PG_AVDD1V8 — PG_AVDD1V8
PG_AVDD5V0 — PG_AVDD5V0
PG_DVDD1V8 — PG_DVDD1V8
PG_DVDD5V0 — PG_DVDD5V0
PG_SW+2V5 — PG_SW+2.5V
PG_SW+6V — PG_SW+6V
PWRGOOD — PG_FPGA
PG_SW+16V — PG_SW+16V
PG_SW-16V — PG_SW-16V
PG-15V — PG_L-15V
PG+15V — PG_L+15V

→ PG

Voltage Legend:
SW+2V5 = 2.5V from switcher
SW+6V = 6V from switcher

ADC Power
AVDD1V8 = 1.8V ADC apwr
DVDD1V8 = 1.8V ADC dpwr
AVDD5V0 = 5V ADC apwr
DVDD5V0 = 5V ADC dpwr

Phase Power:
DVDD5V0 = > P1_5V0
DVDD5V0 = > P2_5V0

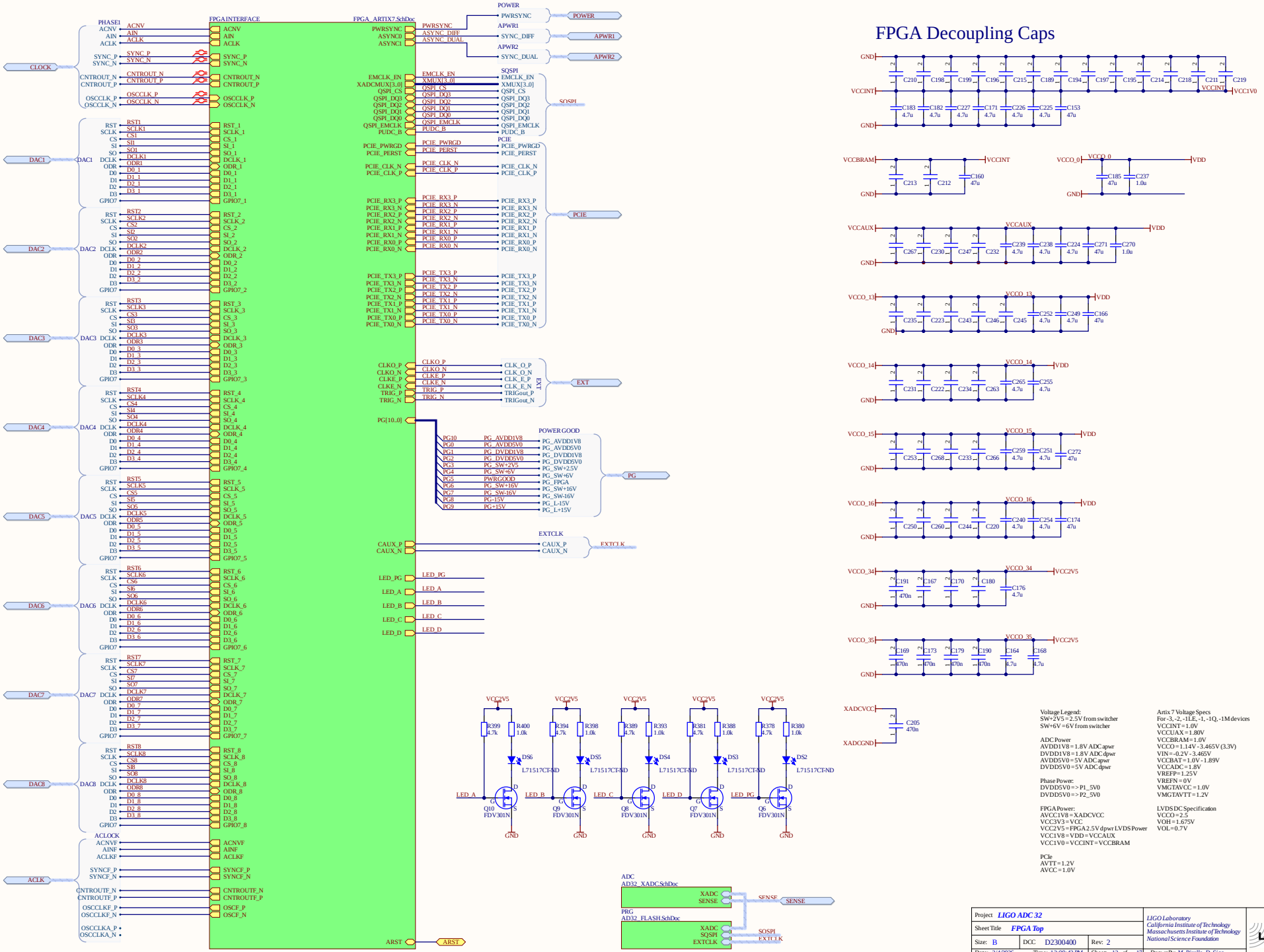
FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM

PCIe
AVTT = 1.2V
AVCC = 1.0V

LT8585EDKD Configs:
+6V
RFBX = (Vout-1.204V)/83.3uA
RFBX = (6V-1.204V)/83.3uA
RFBX = 57.6k
RT = 76k (1MHz)
C1 > 1uF
4uH < Ltyp < 22uH
COUT >33uF

+2.5V
RFBX = (Vout-1.204V)/83.3uA
RFBX = (2.5V-1.204V)/83.3uA
RFBX = 15.6k
RT = 76k (1MHz)
C1 > 1uF
2.3uH < Ltyp < 12.6uH
COUT >45uF

Project	*LIGO ADC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Dual Analog Supply*		
Size: B	DCC D2300400	Rev: 2	
Date: 2/4/2026	Time: 12:09:42 PM	Sheet: 11 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: AD32_Bipolar2.SchDoc			



FPGA Decoupling Caps

Voltage Legend:
SW+2V5 = 2.5V from switcher
SW+6V = 6V from switcher

ADC Power
AVDD1V8 = 1.8V ADC apwr
DVDD1V8 = 1.8V ADC dpwr
AVDD5V0 = 5V ADC apwr
DVDD5V0 = 5V ADC dpwr

Phase Power:
DVDD5V0 => P1_5V0
DVDD5V0 => P2_5V0

FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM

PCIe
AVTT = 1.2V
AVCC = 1.0V

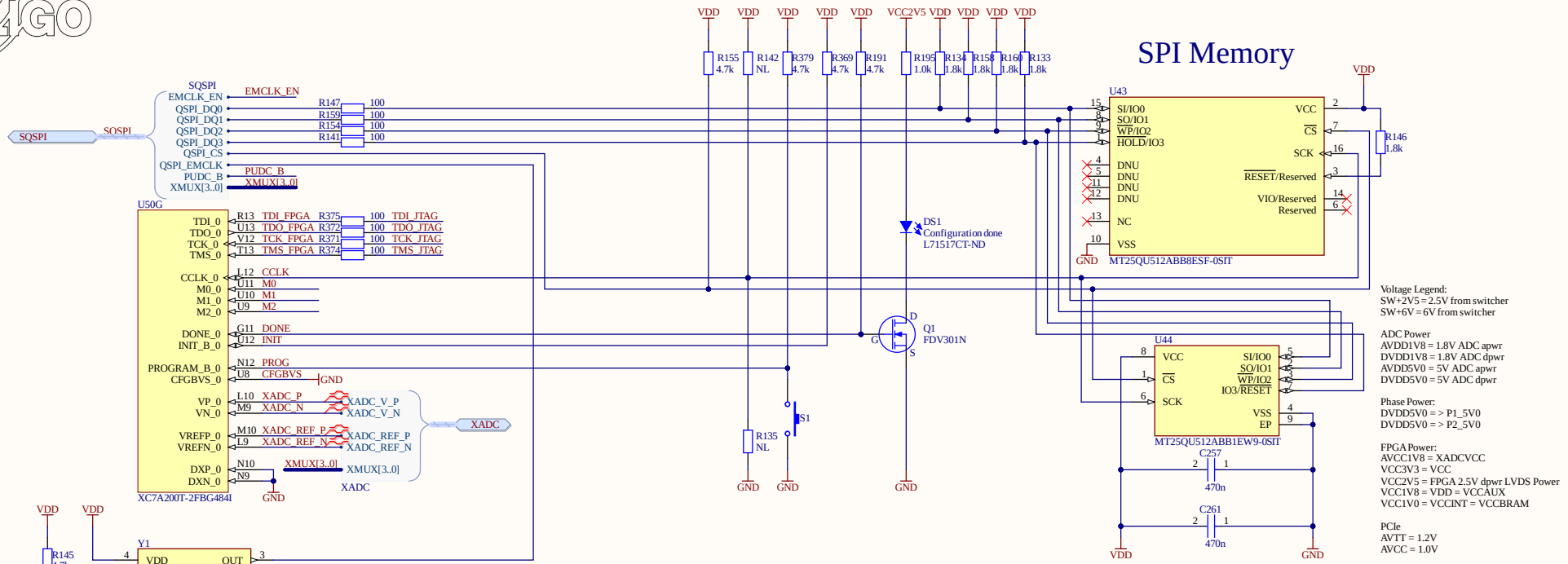
Artix 7 Voltage Specs
For -3, -2, -1LE, -1, -1Q, -1M devices
VCCINT = 1.0V
VCCUAX = 1.80V
VCCBRAM = 1.0V
VCCO = 1.14V - 3.465V (3.3V)
VIN = -0.2V - 3.465V
VCCBAT = 1.0V - 1.89V
VCCADC = 1.8V
VREFP = 1.25V
VREFN = 0V
VMGTAVCC = 1.0V
VMGTAVTT = 1.2V

LVDS DC Specification
VCCO = 2.5
VOH = 1.675V
VOL = 0.7V

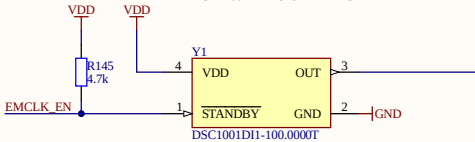
Project	*LIGO ADC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*FPGA Top*		
Size: B	DCC: D2300400	Rev: 2	
Date: 2/4/2026	Time: 12:09:42 PM	Sheet 12 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: AD32_FPGA.SchDoc			

JTAG and SPI Flash

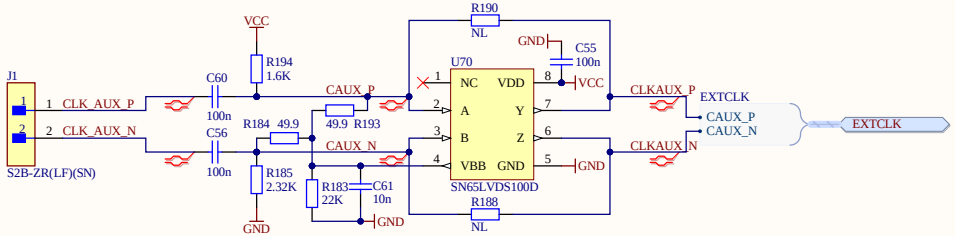
VDD is 1.8V for this design



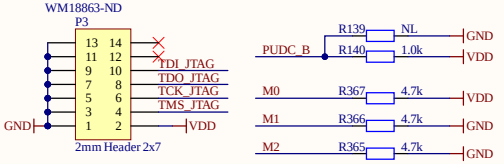
100 MHz Program Clock



AUX Input Clock Buffers



JTAG Header



Project	LIGO ADC 32		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation
Sheet Title	JTAG & SPI Flash		
Size: B	DCC D2300400	Rev: 2	
Date: 2/4/2026	Time: 12:09:42 PM	Sheet: 13 of 17	DrawnBy: M. Pirello, D. Sigg
File: AD32_FLASH.SchDoc			

INA210 configuration
VCC = VCC2 = 3.3V
Vout = (I x 10mohm) * 200
I = Vout / (200 * 10mohm)

12.5mOhm sense R
2A range
Gain 200 V/V

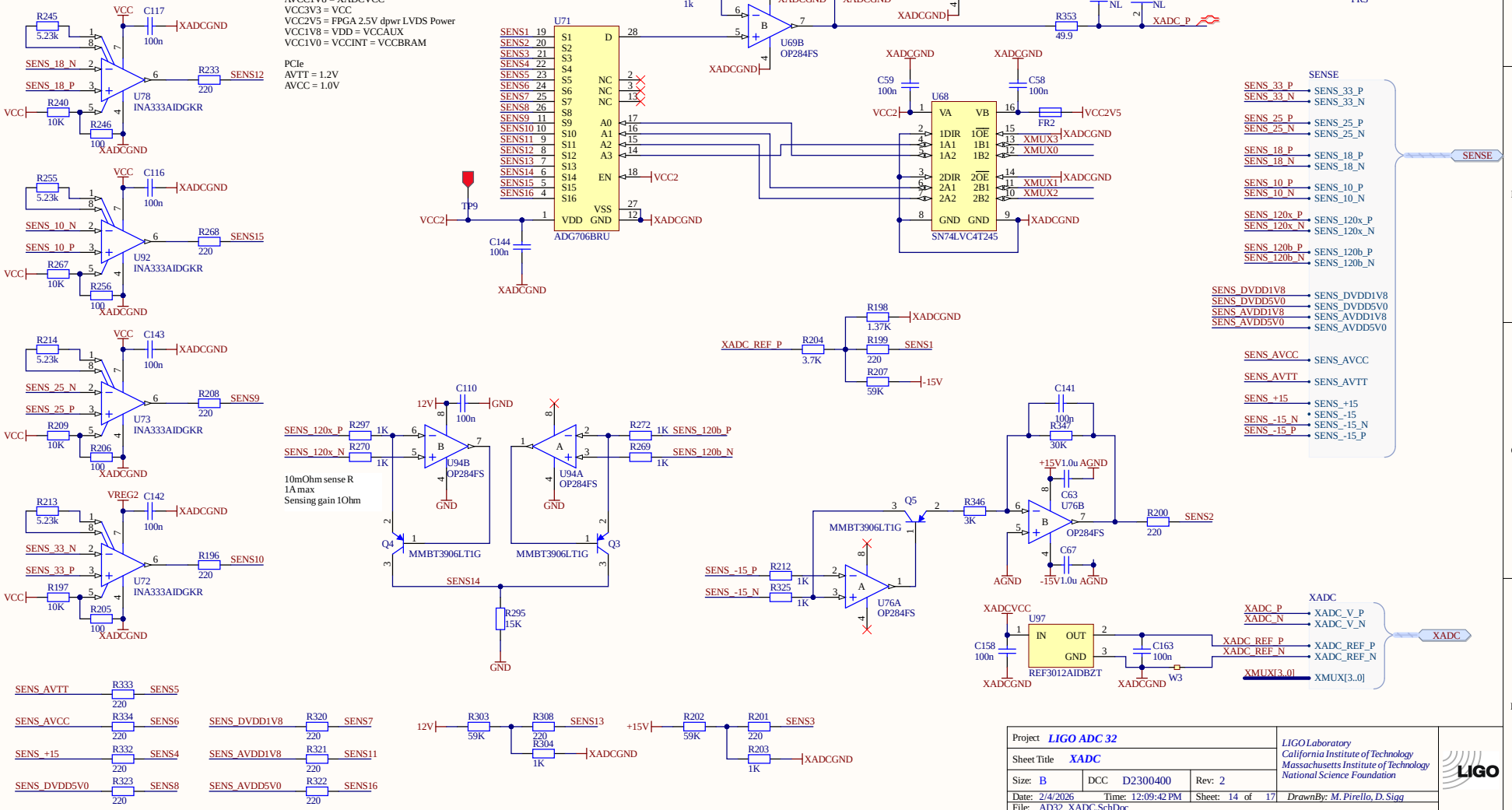
Voltage Legend:
SW+2V5 = 2.5V from switcher
SW+6V = 6V from switcher

ADC Power
AVDD1V8 = 1.8V ADC apwr
DVDD1V8 = 1.8V ADC dpwr
AVDD5V0 = 5V ADC apwr
DVDD5V0 = 5V ADC dpwr

Phase Power:
DVDD5V0 = > P1_5V0
DVDD5V0 = > P2_5V0

FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM

PCIe
AVTT = 1.2V
AVCC = 1.0V



Project	LIGO ADC 32		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation
Sheet Title	XADC		
Size: B	DCC D2300400	Rev: 2	
Date: 2/4/2026	Time: 12:09:42 PM	Sheet: 14 of 17	DrawnBy: M. Pirello, D. Sigg
File: AD32_XADC.SchDoc			

ADC 1

RST_1
SCLK_1
CS_1
SI_1
SO_1
DCLK_1
ODR_1
D0_1
D1_1
D2_1
D3_1
GPIO7_1

ADC 2

RST_2
SCLK_2
CS_2
SI_2
SO_2
DCLK_2
ODR_2
D0_2
D1_2
D2_2
D3_2
GPIO7_2

ADC 3

RST_3
SCLK_3
CS_3
SI_3
SO_3
DCLK_3
ODR_3
D0_3
D1_3
D2_3
D3_3
GPIO7_3

ADC 4

RST_4
SCLK_4
CS_4
SI_4
SO_4
DCLK_4
ODR_4
D0_4
D1_4
D2_4
D3_4
GPIO7_4

ADC 5

RST_5
SCLK_5
CS_5
SI_5
SO_5
DCLK_5
ODR_5
D0_5
D1_5
D2_5
D3_5
GPIO7_5

ADC 6

RST_6
SCLK_6
CS_6
SI_6
SO_6
DCLK_6
ODR_6
D0_6
D1_6
D2_6
D3_6
GPIO7_6

ADC 7

RST_7
SCLK_7
CS_7
SI_7
SO_7
DCLK_7
ODR_7
D0_7
D1_7
D2_7
D3_7
GPIO7_7

ADC 8

RST_8
SCLK_8
CS_8
SI_8
SO_8
DCLK_8
ODR_8
D0_8
D1_8
D2_8
D3_8
GPIO7_8

ADC Reset

ARST

FPGA xADC

XADCMUX[3..0]

FPGA Flash

QSPI_DQ0
QSPI_DQ1
QSPI_DQ2
QSPI_DQ3
QSPI_CS
EMCLK_EN
QSPI_EMCLK
PUDC_B

Clocks & Triggers

CLKO_P
CLKO_N
CLKE_P
CLKE_N
TRIG_P
TRIG_N

PCIe Connector

PCIE_RX3_N
PCIE_RX3_P
PCIE_RX2_N
PCIE_RX2_P
PCIE_RX1_N
PCIE_RX1_P
PCIE_RX0_N
PCIE_RX0_P
PCIE_TX3_N
PCIE_TX3_P
PCIE_TX2_N
PCIE_TX2_P
PCIE_TX1_N
PCIE_TX1_P
PCIE_TX0_N
PCIE_TX0_P
PCIE_CLK_N
PCIE_CLK_P
PCIE_PERST
PCIE_PWRGD

Power Sync

PWRSYNC
ASYNC0
ASYNC1

Power Good

PG[10..0]

Aux Input Clock

CAUX_P
CAUX_N

LED Indicators

LED_PG
LED_A
LED_B
LED_C
LED_D

Phase Detector 1

ACNV
AINV
ACLK
SYNC_P
SYNC_N
CNTROUT_N
CNTROUT_P
OSCCLK_P
OSCCLK_N

Phase Detector 2

ACNVF
AINF
ACLKF
SYNCF_P
SYNCF_N
CNTROUTF_N
CNTROUTF_P
OSCFCLK_P
OSCFCLK_N

U50B — BANK 14 — XC7A200T-2FBG484I

U50C — BANK 15 — XC7A200T-2FBG484I

U50E — BANK 34 — XC7A200T-2FBG484I

U50J — XC7A200T-2FBG484I

U50A — BANK 13 — XC7A200T-2FBG484I

U50D — BANK 16 — XC7A200T-2FBG484I

U50F — BANK 35 — XC7A200T-2FBG484I

U50K — XC7A200T-2FBG484I

U50I — XC7A200T-2FBG484I

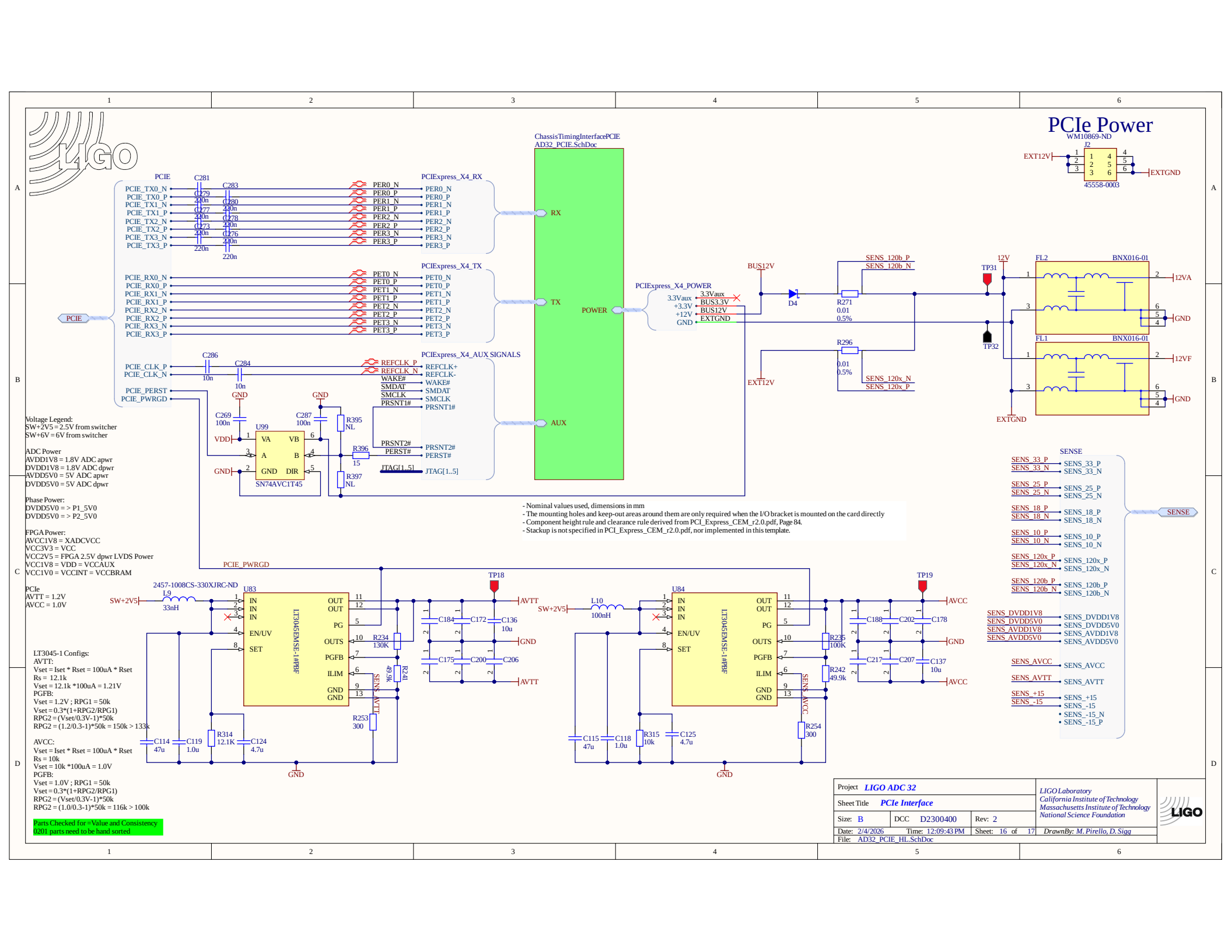
U50H — XC7A200T-2FBG484I

Project	LIGO ADC 32
Sheet Title	FPGA
Size: B	DCC: D2300400 Rev: 2
Date: 2/4/2026	Time: 12:09:42 PM Sheet 15 of 17
File:	FPGA_ARTIX7.SchDoc

LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation

Drawn By: M. Pirello, D. Sigg

PCIe Power



Voltage Legend:
SW+2V5 = 2.5V from switcher
SW+6V = 6V from switcher

ADC Power
AVDD1V8 = 1.8V ADC apwr
DVDD1V8 = 1.8V ADC dpwr
AVDD5V0 = 5V ADC apwr
DVDD5V0 = 5V ADC dpwr

Phase Power:
DVDD5V0 = > P1_5V0
DVDD5V0 = > P2_5V0

FPGA Power:
AVCC1V8 = XADCVCC
VCC3V3 = VCC
VCC2V5 = FPGA 2.5V dpwr LVDS Power
VCC1V8 = VDD = VCCAUX
VCC1V0 = VCCINT = VCCBRAM

PCIe
AVTT = 1.2V
AVCC = 1.0V

LT3045-1 Configs:
AVTT:
Vset = Iset * Rset = 100uA * Rset
Rs = 12.1k
Vset = 12.1k *100uA = 1.21V
PGFB:
Vset = 1.2V ; RPG1 = 50k
Vset = 0.3*(1+RPG2/RPG1)
RPG2 = (Vset/0.3V-1)*50k
RPG2 = (1.2/0.3-1)*50k = 150k > 133k

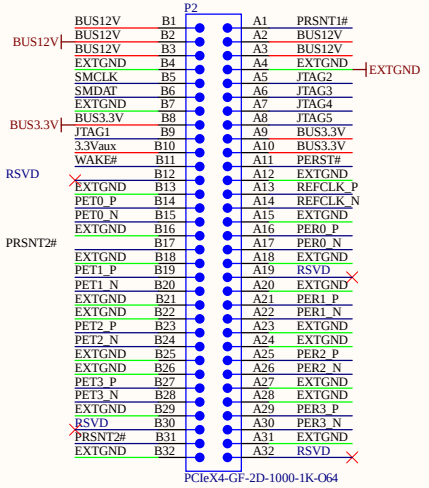
AVCC:
Vset = Iset * Rset = 100uA * Rset
Rs = 10k
Vset = 10k *100uA = 1.0V
PGFB:
Vset = 1.0V ; RPG1 = 50k
Vset = 0.3*(1+RPG2/RPG1)
RPG2 = (Vset/0.3V-1)*50k
RPG2 = (1.0/0.3-1)*50k = 116k > 100k

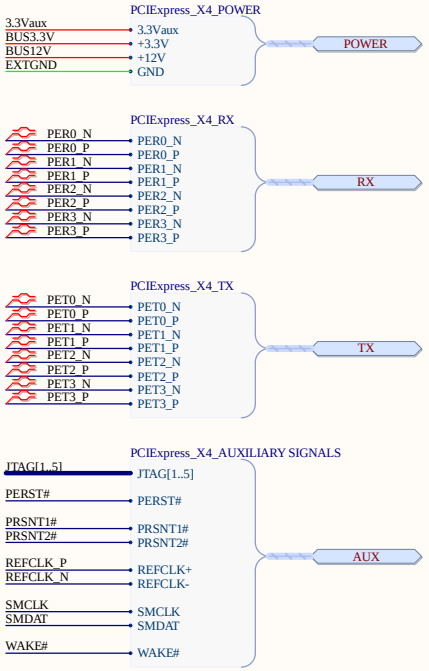
Parts Checked for =Value and Consistency
0201 parts need to be hand sorted

- Nominal values used, dimensions in mm
- The mounting holes and keep-out areas around them are only required when the I/O bracket is mounted on the card directly
- Component height rule and clearance rule derived from PCI_Express_CEM_r2.0.pdf, Page 84.
- Stackup is not specified in PCI_Express_CEM_r2.0.pdf, nor implemented in this template.

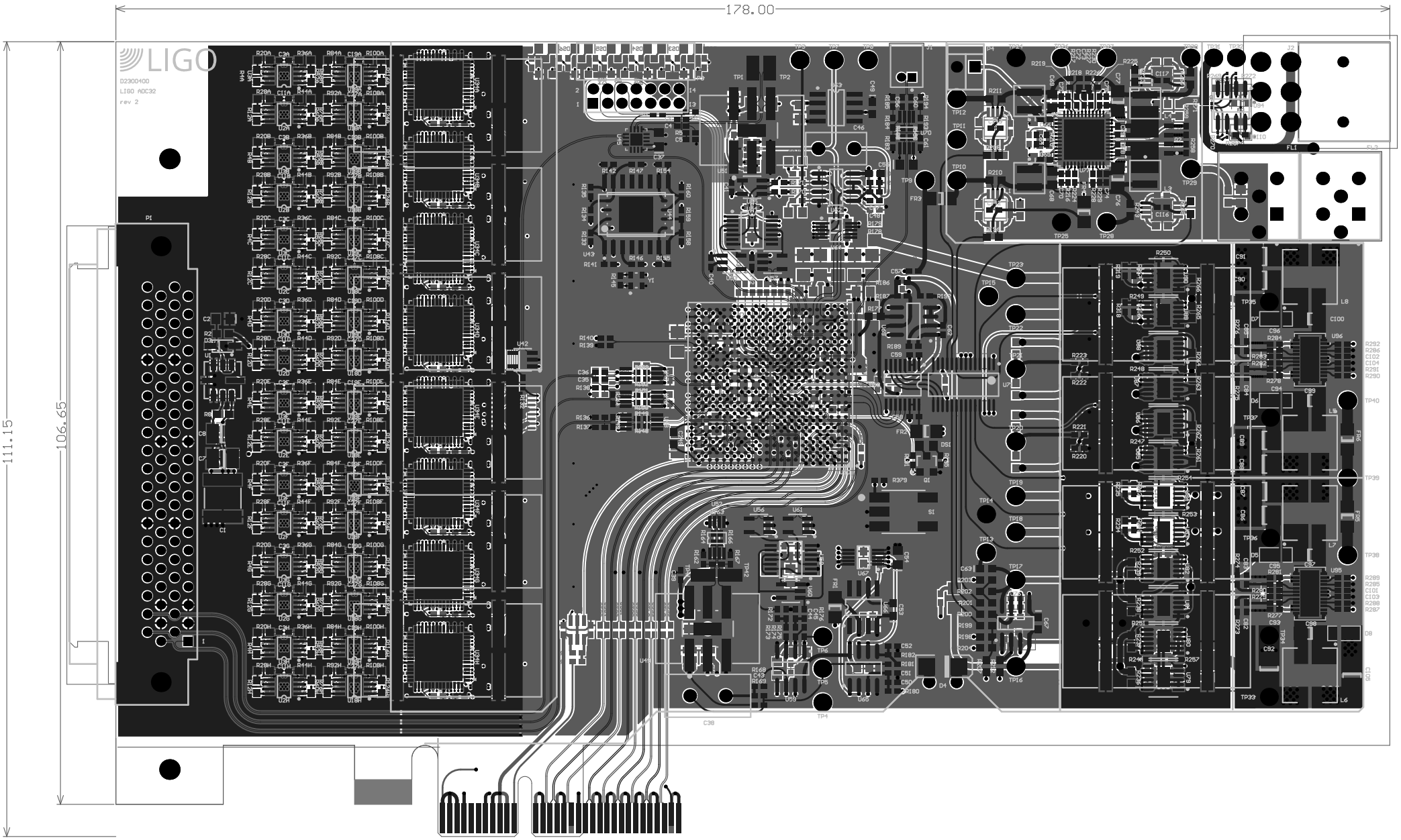
Project	*LIGO ADC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*PCIe Interface*		
Size: B	DCC D2300400	Rev: 2	
Date: 2/4/2026	Time: 12:09:43 PM	Sheet: 16 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: AD32_PCIE_HL.SchDoc			

PCIe 4x Slot





Project *LIGO ADC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *PCIe*			
Size: B	DCC D2300400	Rev: 2	
Date: 2/4/2026	Time: 12:09:43 PM	Sheet: 17 of 17	*DrawnBy: M. Pirello, D. Sigg*
File: AD32_PCIE.SchDoc			


178.00
111.15
106.65
LIGO
D2300400
LIGO ADC32
rev 2