LIGO DAC Design
Results and Prospects

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Reminder Goals

- Technology:
  - New ADC/DAC chips typically support faster rates not necessarily more bits
    - iLIGO: ~20kHz, aLIGO: ~200kHz, now: ~1MHz.
  - Lower noise achieved by faster acquisition
  - Avoid higher data rates for IO chassis by implementing FPGA decimation filters
- Clocking Improvements:
  - No rogues clocks: synchronized switchers, FPGA clock is 2^{26}Hz
  - Use timing distribution signal as input clock: Converter knows GPS time
  - No special startup synchronization procedure required, always synchronized
  - Allows for time stamped data transfers
    - Watchdog: Outputs can be stopped when no valid data is received
- Others:
  - Replace failing 18-bit DAC (GS 20-bit DAC very expensive, i.e., ~$7500 for 8 channels)
  - Running out of space in some IO chassis

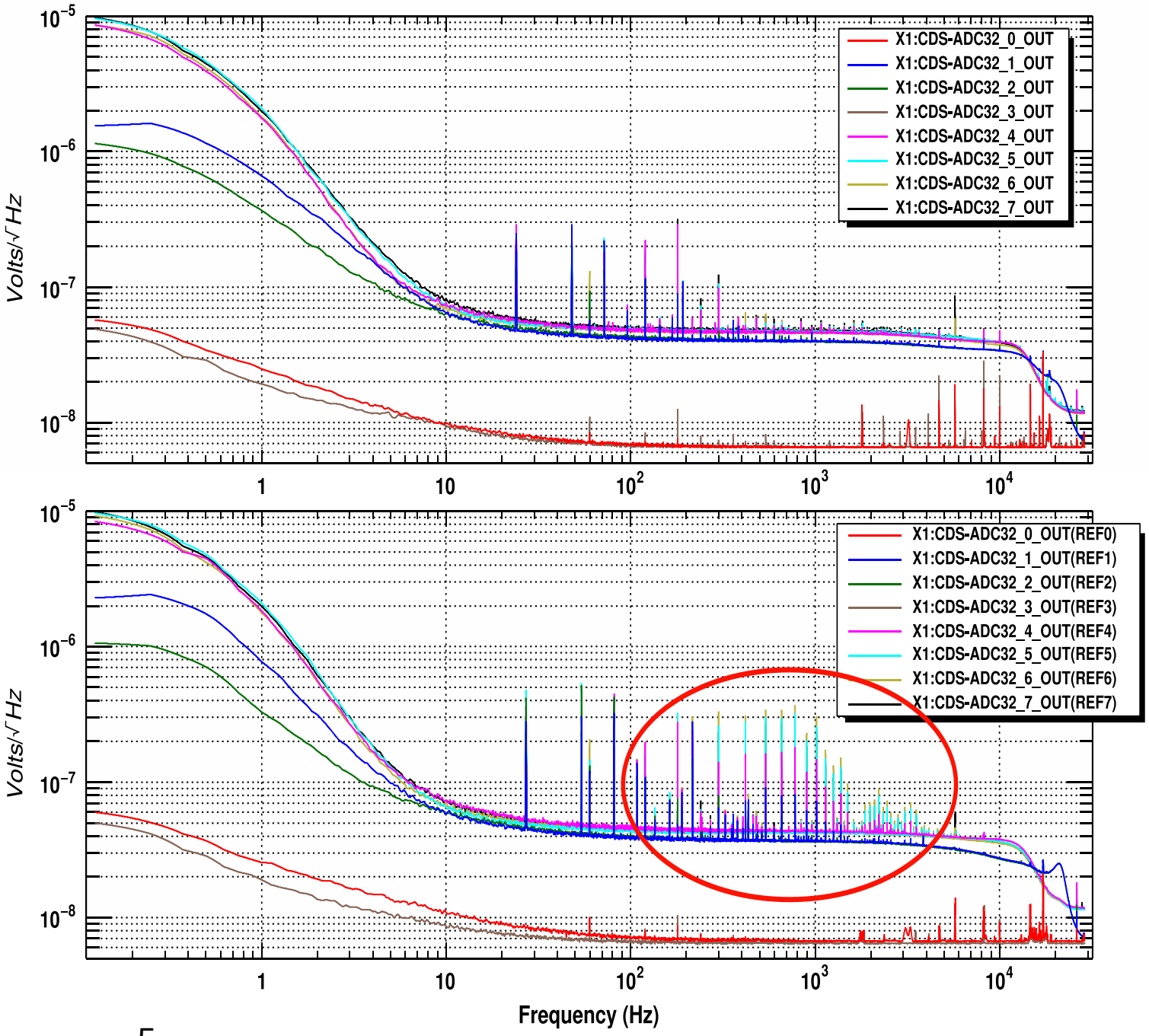
Status

- DAC Prototype done
  - Uses ΣΔ-Technology, on chip FIR filters replaced by FPGA IIR filters
  - Runs at 1MHz data rate, but max useful rate is 128kHz
    - Runs at 64kHz in RTCDS: Up-sampling to 1MHz and 30KHz low pass filters in FPGA
  - FPGA firmware debugged, DMA and filters working
  - RTCDS drivers fully functional
- In-Situ DAC Testing
  - 1 DAC board installed at EX driving ETMX ESD, L1, L2
  - Reliability: Installed on 7/25/24, running with connected outputs since 9/17/24
  - No visible effect on sensitivity or operations
- Test stand results
  - Superior to 20bit DAC in all tests performed
  - See next pages for details
- Report T2400066, compare to G1500761 (20-bit) and G1401399 (18-bit)

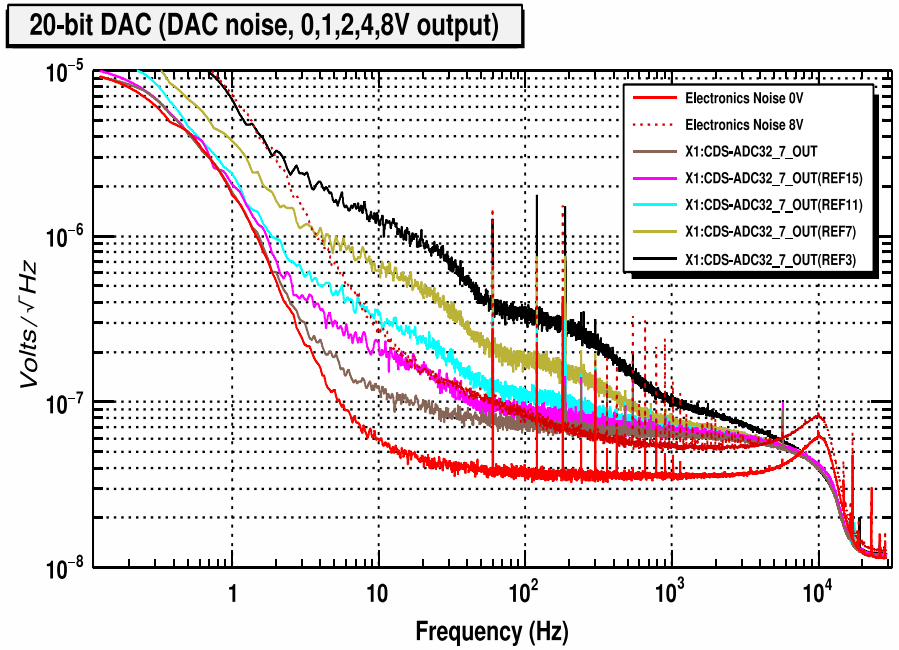
Proposal

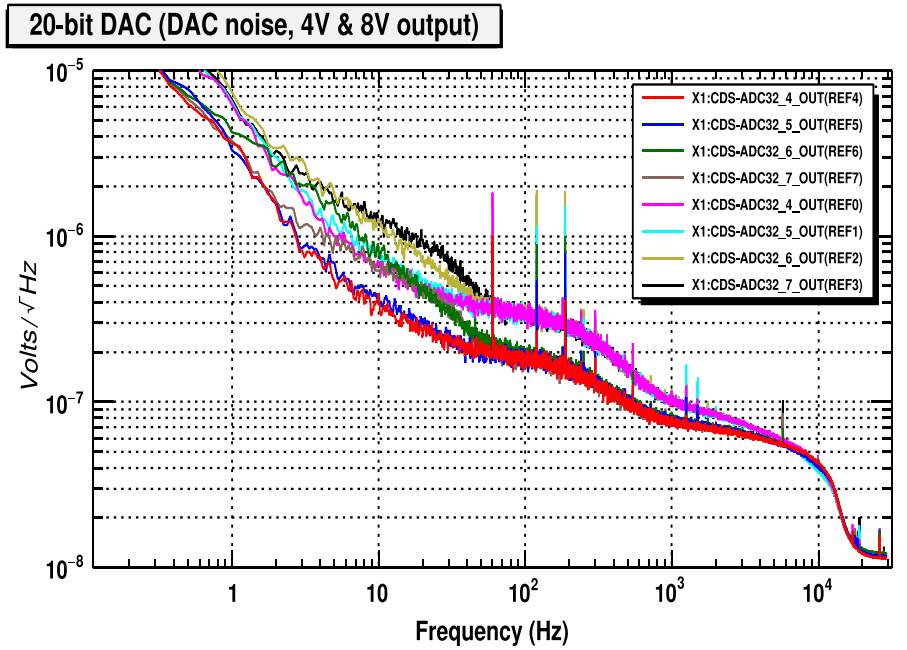
- Build 20 new 32-chn DACs to replace old 8-chn 18-bit DACs at LHO
  - Cost: ~$2500/DAC when ordering 20 or more (includes new adapter/interface boards for AI)
- Still use 33 18-bit DACs in H1
  - Don’t have enough 20-bit DACs, would have to buy ~20 more to complete the transition
  - Would cost ~$150k
- Will have extra channels to cover any A+ short fall
  - A+ is using 16-bit DACs in some places to save costs, wouldn’t be needed
- Will have extra channels to cover JAC/POPX upgrades
  - sus2a and sus2b IO chassis can be combined into sus12

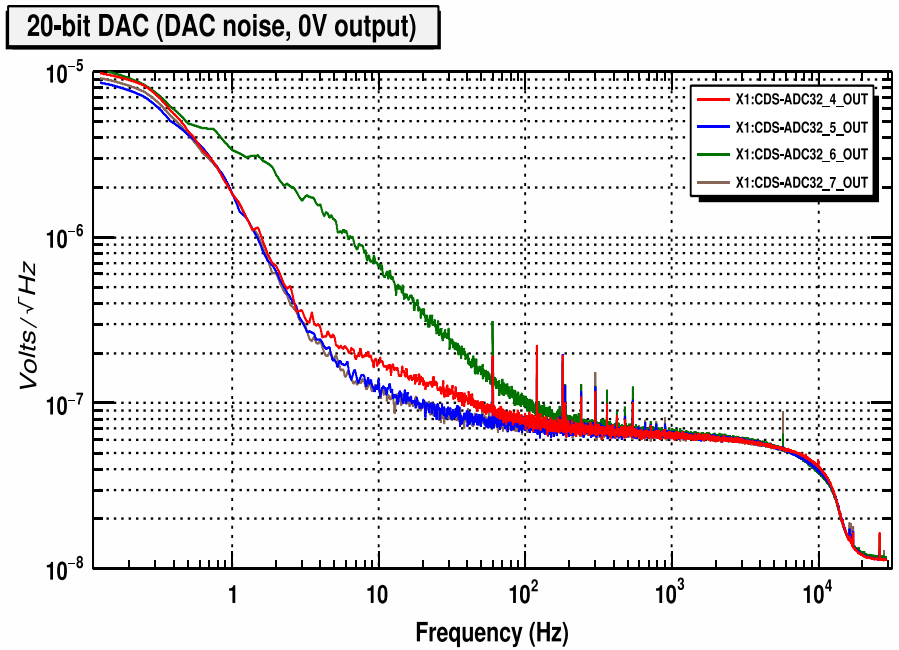
Results from Test Stand

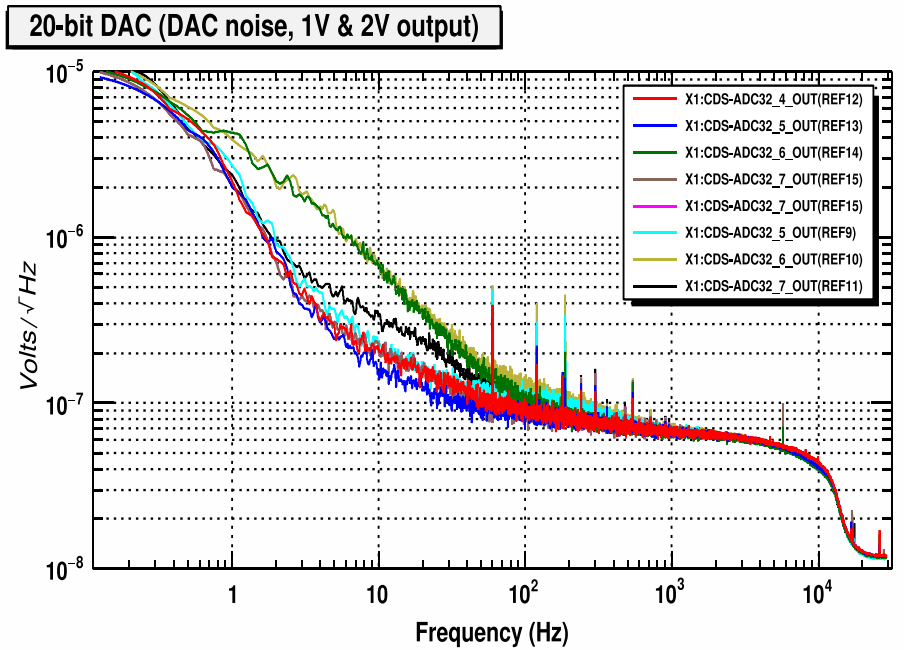


- Top: New DAC in empty IO chassis
- Bottom: Multiple old 16-bit ADC cards added
- Beat notes of oscillators on ADC boards



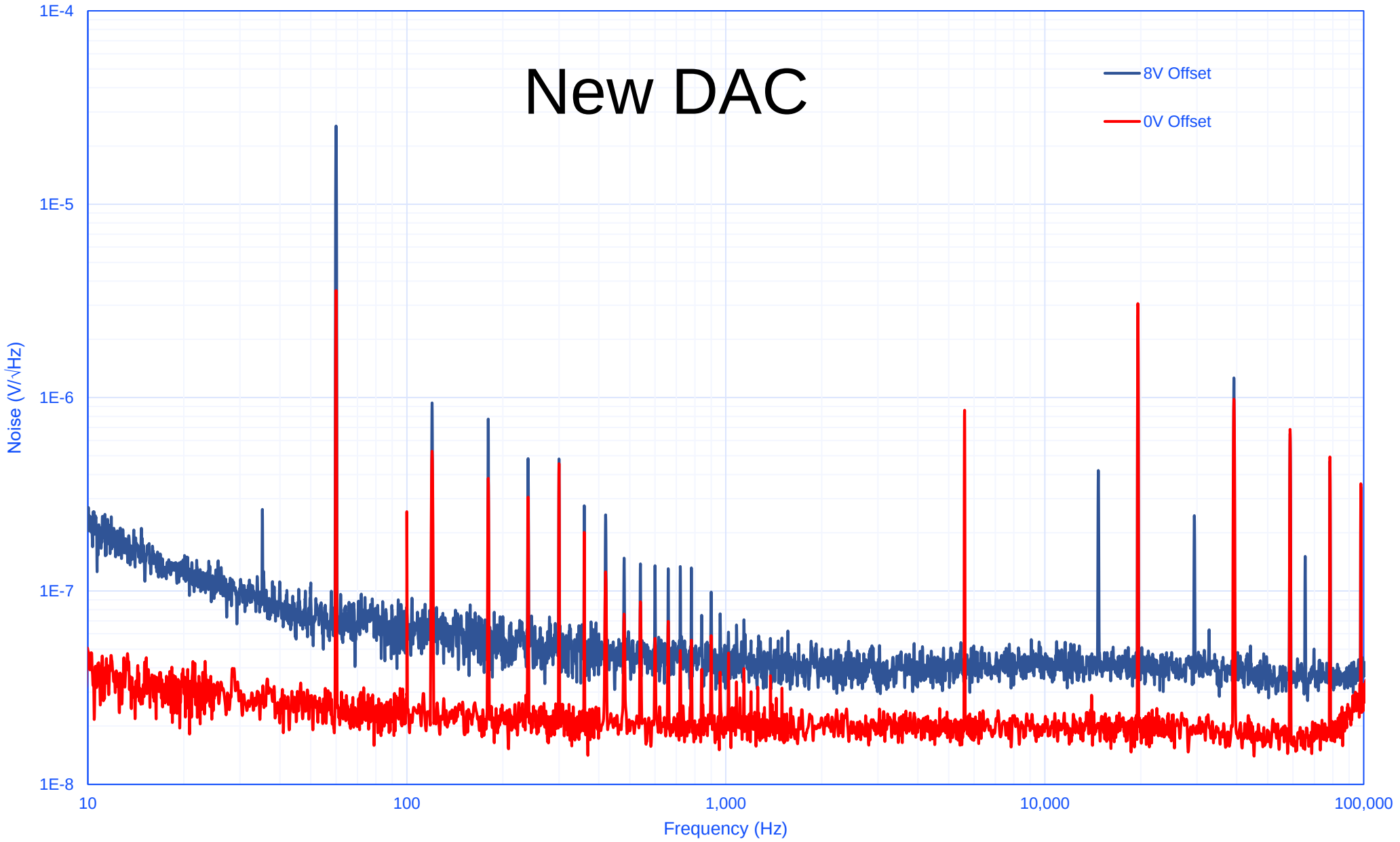




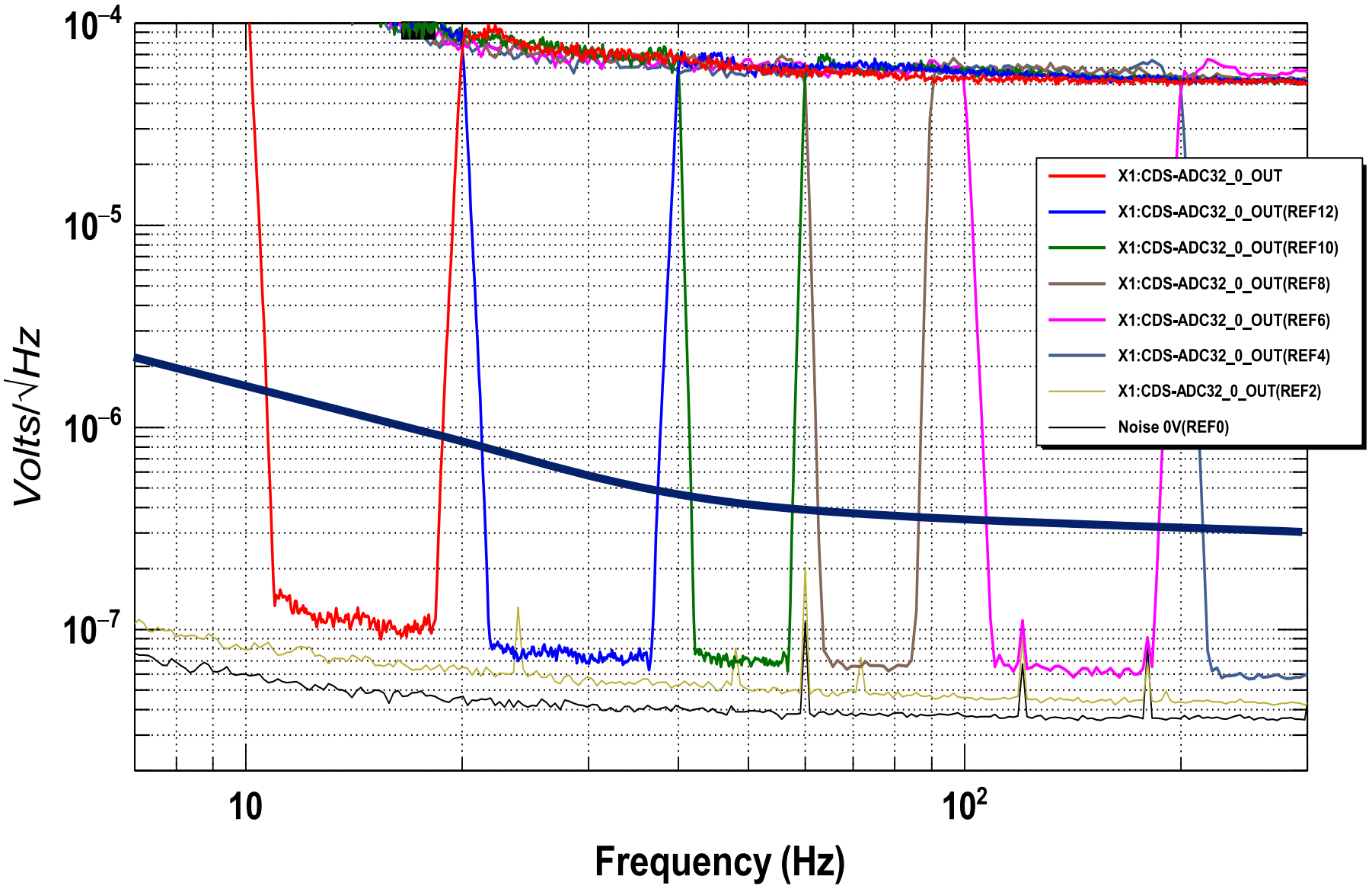


20-bit DAC

- Fair amount of excess noise with high bias voltage
- Channel 6 probably broken

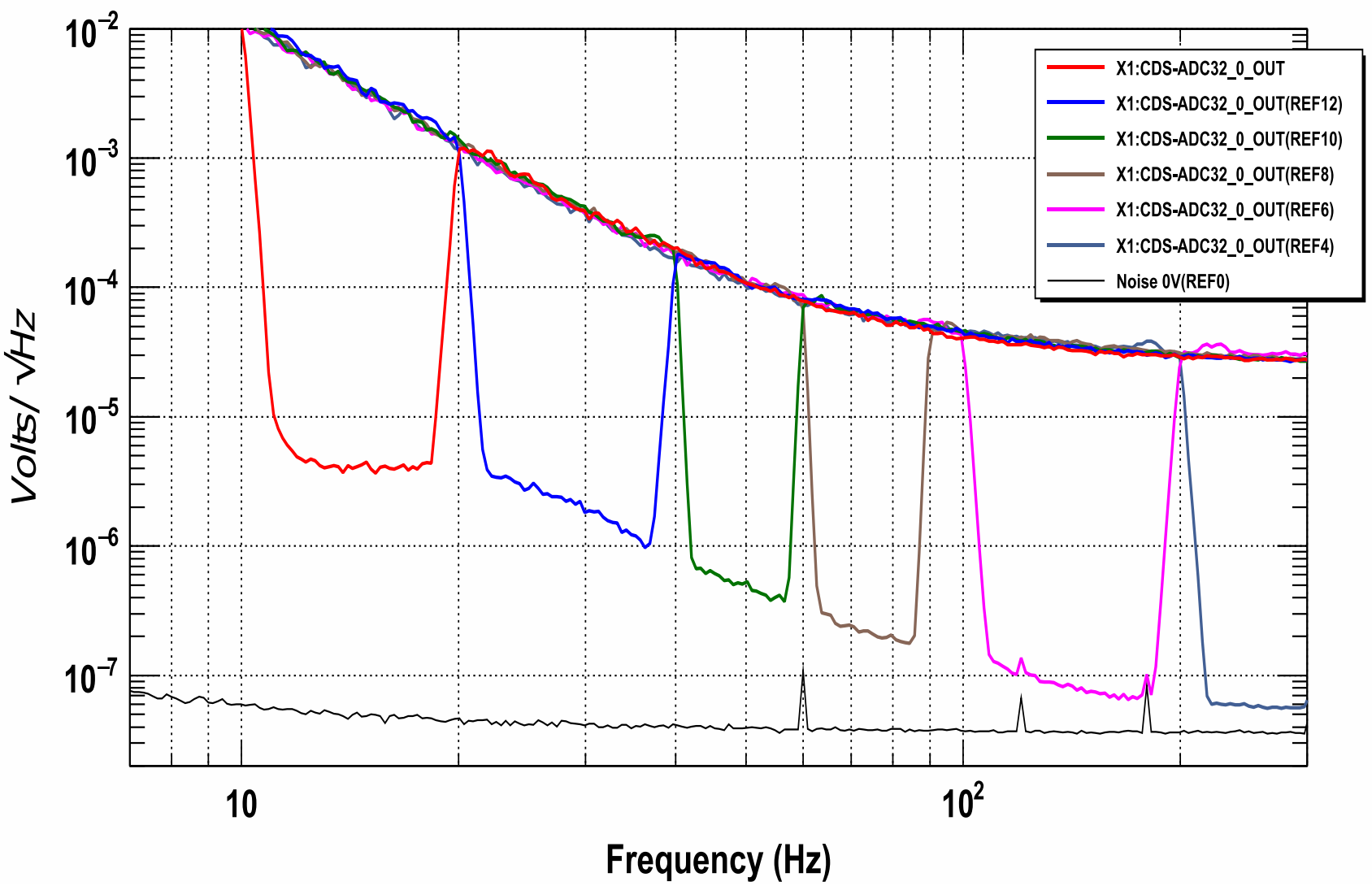

New DAC
8V Offset
0V Offset
1E-4
1E-5
1E-6
1E-7
1E-8
Noise (V/√Hz)
10
100
1,000
10,000
100,000
Frequency (Hz)

Four Simple Poles/Zeroes at 1 Hz/10 Hz



- Significantly better than 20-bit DAC G1500761

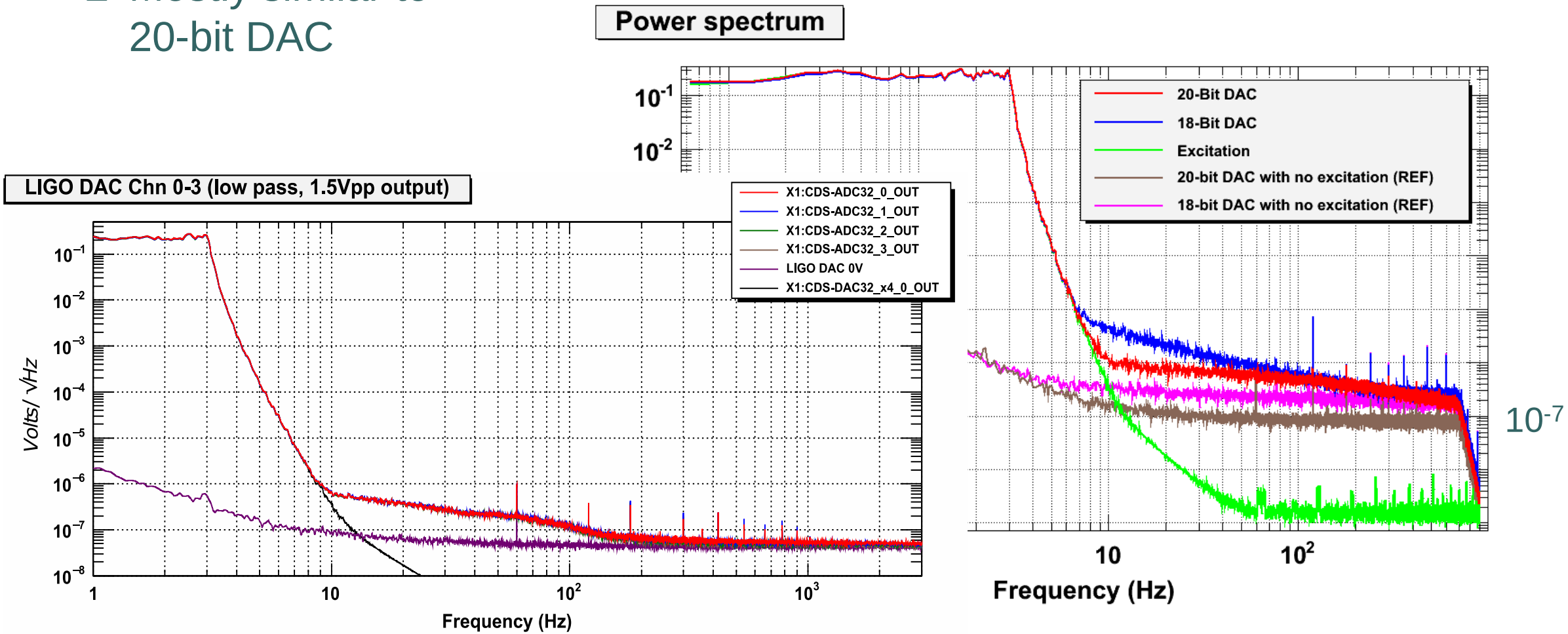
Four Simple Poles/Zeroes at 5 Hz/50 Hz



- Low frequency similar to 20-bit DAC
- Not totally clear if we are seeing ADC noise

cheby1(“LowPass”,8,1,3)

- Mostly similar to 20-bit DAC



10^{-7}

Summary

- New DAC has superior performance in most tests
- No rogue oscillators
- Costs 15x less per channel than 20-bit DAC
- Has performed well in ETMX test

- Recommend going forward with 1st purchase of 20 boards for H1

Front-End Chassis