LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

LIGO Laboratory / LIGO Scientific Collaboration

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Fast Digital Servo: Timing Diagrams

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1 Overview

This document shows proposed timing diagrams to communicate with the converters in the fast digital servo board. The main clock is assumed to be 2^{28} Hz (or roughly 268 MHz), which is derived from the 2^{26} Hz timing clock through the help of a PLL.

2 ADAQ23876 and ADAQ23878 ADCs

These ADCs have an LVDS interface that can be clocked at rates up to 400 MHz. Since we are using two lanes to transfer the data a 134MHz clock frequency is sufficient.

See Figure 1 for the ADAQ23876, and figure 2 for the ADAQ23878.

A full conversion plus readout takes 32 cycles and supports a 2^{23} Hz (8.4 MHz) conversion clock.

3 AD3551R and AD3552R

These DACs have quad SPI interface that can be clocked at rates up to 66 MHz. This is slightly lower than a 2^{26} Hz (67.1 MHz) clock, which means that we cannot easily support the AD3552R in a non-streaming mode unless we run the interface 1.6% faster than recommended. For the AD3551R we can use 6 clock cycles at 268 MHz for one SPI clock cycle which results in a 44.7 MHz SPI clock.

See Figure 3 for the AD3551R, and figure 4 for the AD3552R.

A full conversion plus readout takes 32 cycles and supports a 2^{23} Hz (8.4 MHz) conversion clock when the AD3552R is operated at 67.1 MHz. In principle, it is possible to run these devices in streaming mode that does not require a full address/data cycle but instead keeps sending the data only. This would allow the AD3552R to meet the timing requirements but could result in prolonged invalid data outputs if a SPI cycle is ever missed.

4 DAC11001B

These DACs have SPI interface that can be clocked at rates up to 50 MHz assuming DV_{DD} is 5V and IOV_{DD} is 3.3V. Since 32 bits need to be transmitted per conversion cycle, we can support a 2^{20} Hz (1 MHz) sampling clock for the precision DAC.

See Figure 5 for the DAC11001B timing diagram.

We again use 6 clock cycles at 268 MHz for one SPI clock cycle resulting in a 44.7 MHz SPI clock. Since this interface is single lane, without DDR and requires 32-bits per cycle, we can support a 2^{20} Hz (1 MHz) sampling clock. With a reduced IOV_{DD} at 2.5V or 1.8V we would have to half the sampling clock.

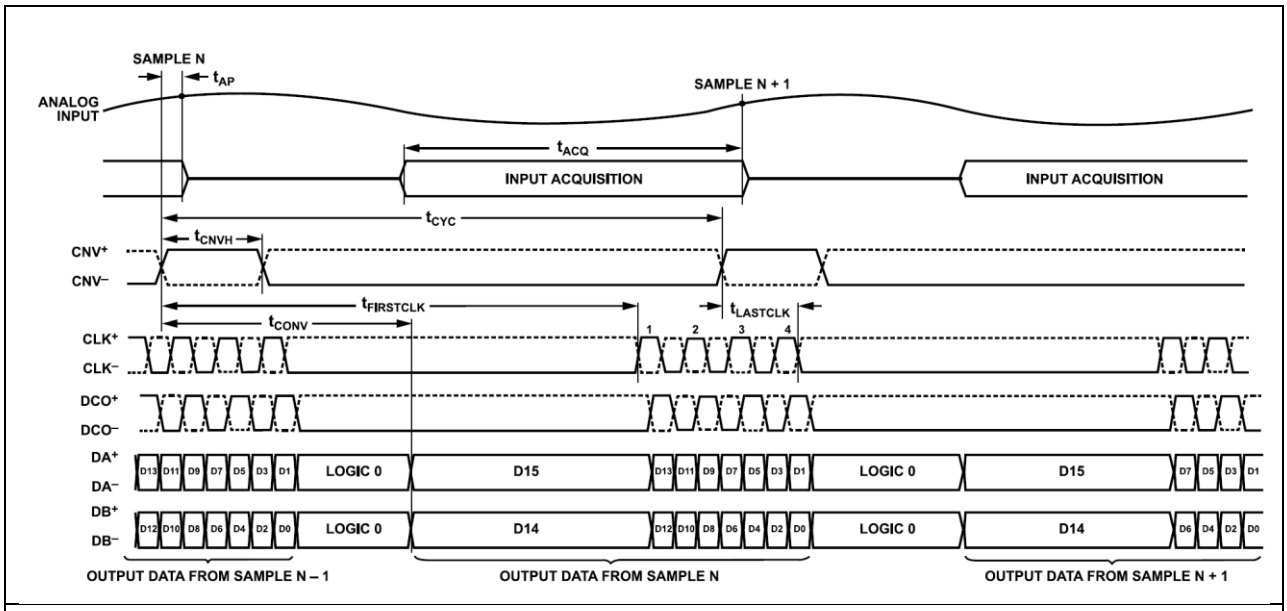


Table 2. Digital Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
Sampling Frequency	f_{SMPL}	0.02		15	MSPS
Conversion Time—CNV± Rising Edge to Data Available	t_{CONV}	54	58	63	ns
Acquisition Phase	t_{ACQ}		t_{CYC} – 39		ns
Time Between Conversions	t_{CYC}	66.6		50,000	ns
CNV± High Time	t_{CNVH}	5			ns
CNV± Low Time	t_{CNVL}	8			ns
CNV± Rising Edge to First CLK± Rising Edge from the Same Conversion	$t_{FIRSTCLK}$	65			ns
CNV± Rising Edge to Last CLK± Falling Edge from the Previous Conversion	$t_{LASTCLK}$			49	ns
CLK± to DCO± Delay	t_{CLKDCO}	0.7	1.3	2.3	ns
CLK± Low Time	t_{CLKL}	1.25			ns
CLK± High Time	t_{CLKH}	1.25			ns
CLK± to DA±/DB± Delay	t_{CLKD}	0.7	1.3	2.3	ns
DCO± to DA±/DB± Skew	t_{SKEW}	–200	0	+200	ps
Sampling Delay Time	t_{AP}		0		ns
Sampling Delay Jitter	t_{JITTER}		0.25		ps_{RMS}

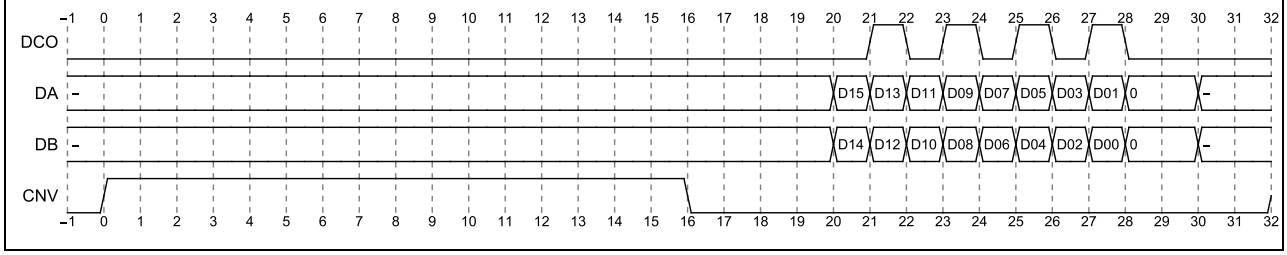
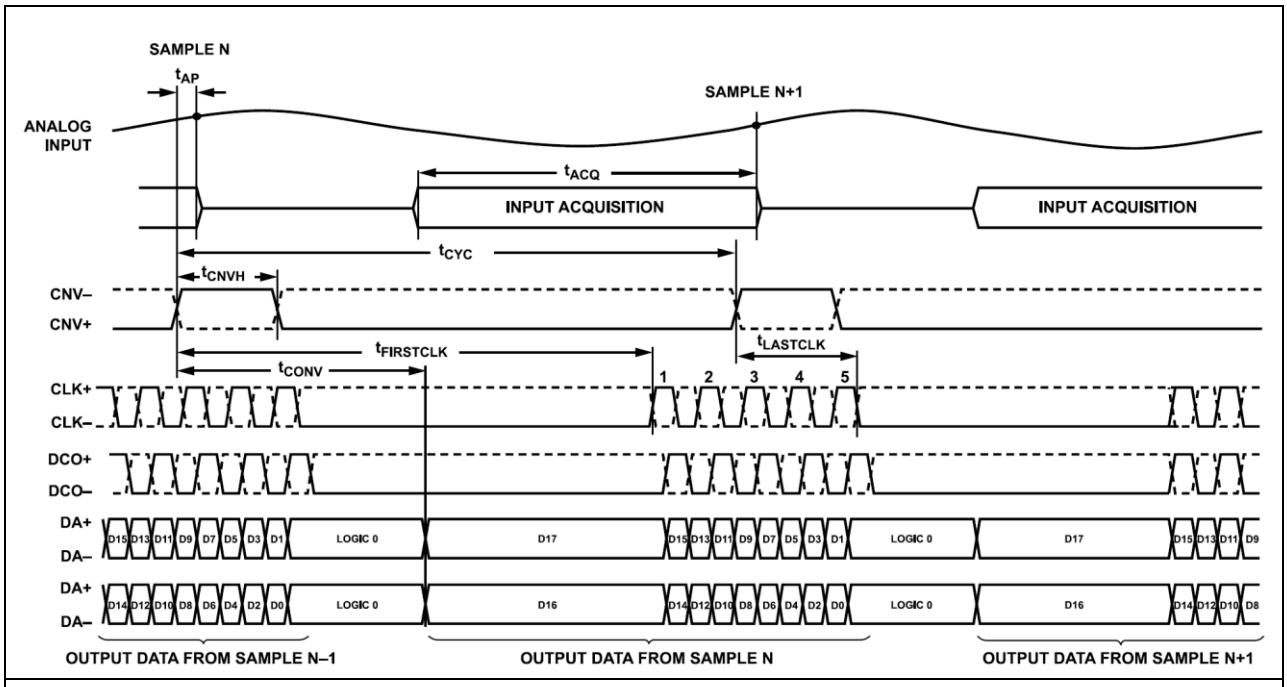


Figure 1: Timing diagram from the ADAQ23876 data sheet (top), timing requirements (middle) and proposed FPGA timing.



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Acquisition Phase	t_{ACQ}		t_{CYC} – 39		ns
Time Between Conversions	t_{CYC}	66.6		50,000	ns
CNV± High Time	t_{CNVH}	5			ns
CNV± Low Time	t_{CNVL}	8			ns
CNV± Rising Edge to First CLK± Rising Edge from the Same Conversion	$t_{FIRSTCLK}$	65			ns
CNV± Rising Edge to Last CLK± Falling Edge from the Previous Conversion	$t_{LASTCLK}$			49	ns
CLK± to DCO± Delay	t_{CLKDCO}	0.7	1.3	2.3	ns
CLK± Low Time	t_{CLKL}	1.25			ns
CLK± High Time	t_{CLKH}	1.25			ns
CLK± to DA±/DB± Delay	t_{CLKD}	0.7	1.3	2.3	ns
DCO± to DA±/DB± Skew	t_{SKEW}	–200	0	+200	ps
Sampling Delay Time	t_{AP}		0		ns
Sampling Delay Jitter	t_{JITTER}		0.25		ps_{RMS}

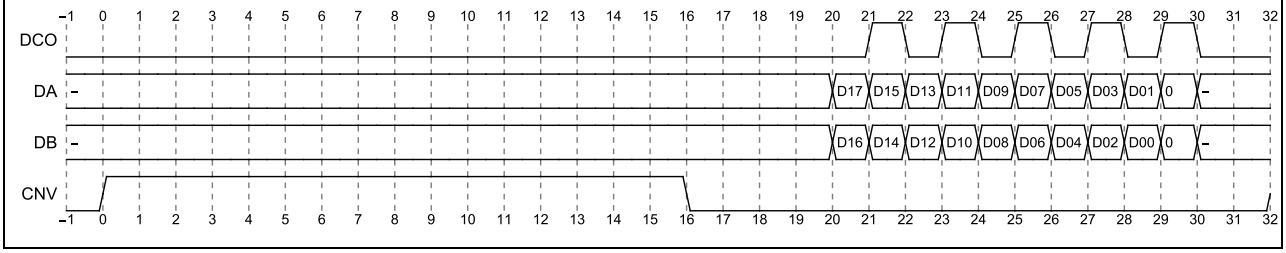
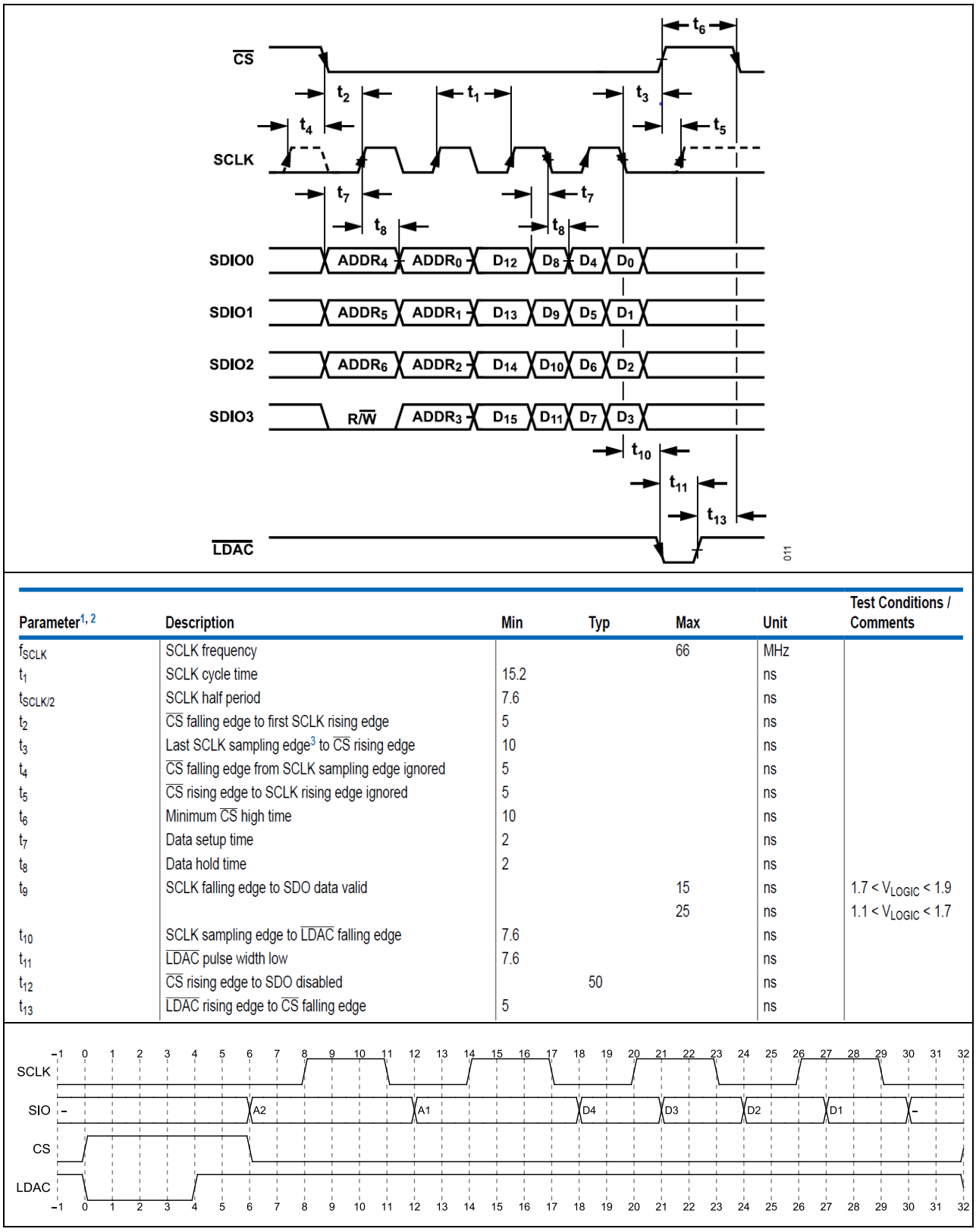
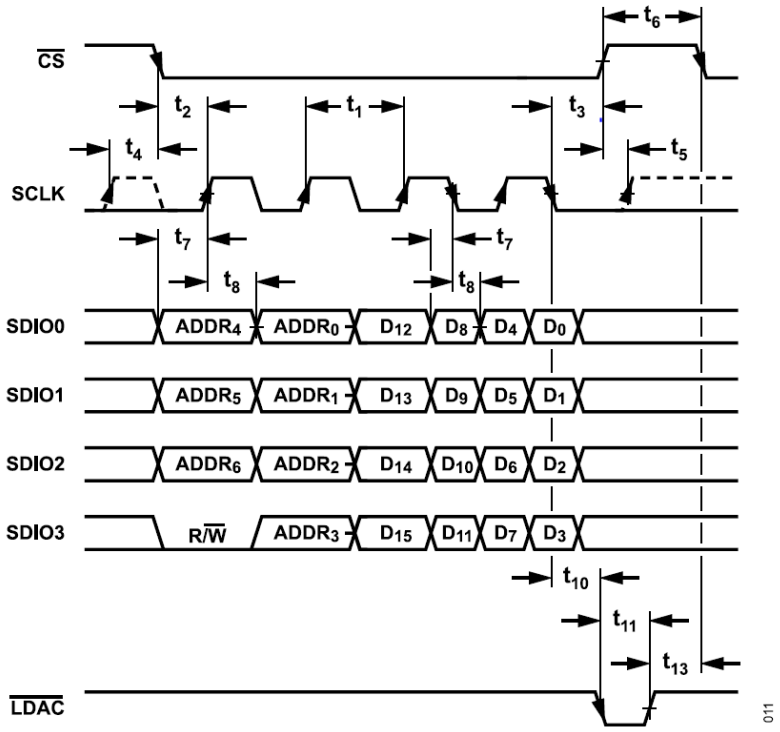


Figure 2: Timing diagram from the ADAQ23878 data sheet (top), timing requirements (middle) and proposed FPGA timing.



Parameter[1, 2]	Description	Min	Typ	Max	Unit	Test Conditions / Comments
f_{SCLK}	SCLK frequency			66	MHz	
t_1	SCLK cycle time	15.2			ns	
$t_{SCLK/2}$	SCLK half period	7.6			ns	
t_2	$\overline{CS}$ falling edge to first SCLK rising edge	5			ns	
t_3	Last SCLK sampling edge[3] to $\overline{CS}$ rising edge	10			ns	
t_4	$\overline{CS}$ falling edge from SCLK sampling edge ignored	5			ns	
t_5	$\overline{CS}$ rising edge to SCLK rising edge ignored	5			ns	
t_6	Minimum $\overline{CS}$ high time	10			ns	
t_7	Data setup time	2			ns	
t_8	Data hold time	2			ns	
t_9	SCLK falling edge to SDO data valid			15	ns	$1.7 < V_{LOGIC} < 1.9$
				25	ns	$1.1 < V_{LOGIC} < 1.7$
t_{10}	SCLK sampling edge to $\overline{LDAC}$ falling edge	7.6			ns	
t_{11}	$\overline{LDAC}$ pulse width low	7.6			ns	
t_{12}	$\overline{CS}$ rising edge to SDO disabled		50		ns	
t_{13}	$\overline{LDAC}$ rising edge to $\overline{CS}$ falling edge	5			ns	

Figure 3: Timing diagram from the AD3551R data sheet (top), timing requirements (middle) and proposed FPGA timing.



Parameter[1, 2]	Description	Min	Typ	Max	Unit	Test Conditions / Comments
f_{SCLK}	SCLK frequency			66	MHz	
t_1	SCLK cycle time	15.2			ns	
$t_{SCLK/2}$	SCLK half period	7.6			ns	
t_2	$\overline{CS}$ falling edge to first SCLK rising edge	5			ns	
t_3	Last SCLK sampling edge[3] to $\overline{CS}$ rising edge	10			ns	
t_4	$\overline{CS}$ falling edge from SCLK sampling edge ignored	5			ns	
t_5	$\overline{CS}$ rising edge to SCLK rising edge ignored	5			ns	
t_6	Minimum $\overline{CS}$ high time	10			ns	
t_7	Data setup time	2			ns	
t_8	Data hold time	2			ns	
t_9	SCLK falling edge to SDO data valid			15	ns	$1.7 < V_{LOGIC} < 1.9$
				25	ns	$1.1 < V_{LOGIC} < 1.7$
t_{10}	SCLK sampling edge to $\overline{LDAC}$ falling edge	7.6			ns	
t_{11}	$\overline{LDAC}$ pulse width low	7.6			ns	
t_{12}	$\overline{CS}$ rising edge to SDO disabled		50		ns	
t_{13}	$\overline{LDAC}$ rising edge to $\overline{CS}$ falling edge	5			ns	

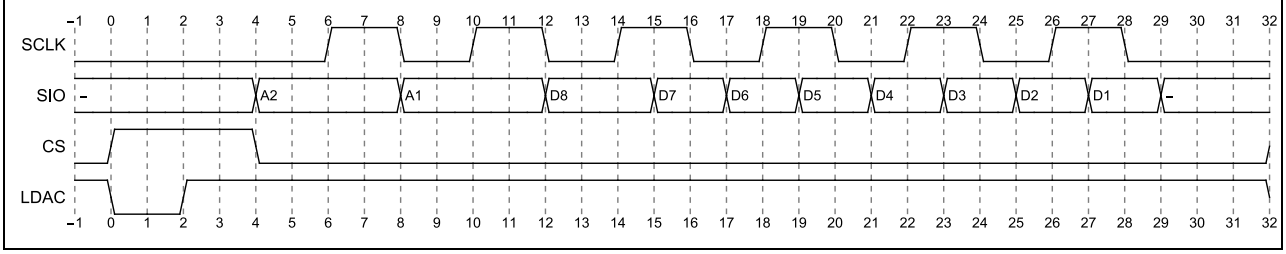
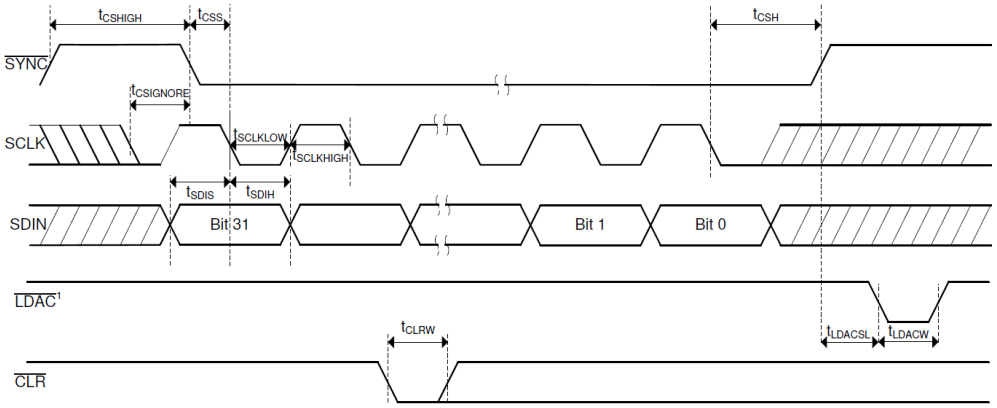
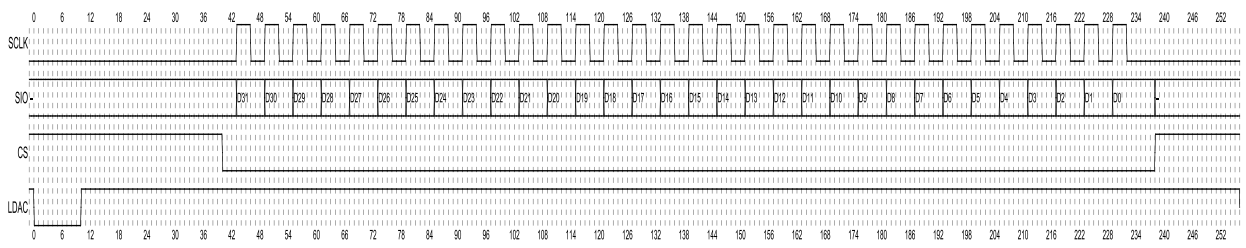


Figure 4: Timing diagram from the AD3552R data sheet (top), timing requirements (middle) and proposed FPGA timing. Notice the slight timing violation.



		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency, 1.7 V ≤ IOV_{DD} < 2.7 V			33	MHz
	SCLK frequency, 2.7 V ≤ IOV_{DD} ≤ 5.5 V			50	
$t_{SCLKHIGH}$	SCLK high time, 1.7 V ≤ IOV_{DD} < 2.7 V	15			ns
	SCLK high time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	10			
$t_{SCLKLOW}$	SCLK low time, 1.7 V ≤ IOV_{DD} < 2.7 V	15			ns
	SCLK low time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	10			
t_{SDIS}	SDI setup, 1.7 V ≤ IOV_{DD} < 2.7 V	13			ns
	SDI setup, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	8			
t_{SDIH}	SDI hold, 1.7 V ≤ IOV_{DD} < 2.7 V	13			ns
	SDI hold, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	8			
t_{CSS}	$\overline{SYNC}$ falling edge to SCLK falling edge, 1.7 V ≤ IOV_{DD} < 2.7 V	23			ns
	$\overline{SYNC}$ falling edge to SCLK falling edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	18			
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge, 1.7 V ≤ IOV_{DD} < 2.7 V	15			ns
	SCLK falling edge to $\overline{SYNC}$ rising edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	10			
t_{CSHIGH}	$\overline{SYNC}$ high time, 1.7 V ≤ IOV_{DD} < 2.7 V	55			ns
	$\overline{SYNC}$ high time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	50			
$t_{CSIGNORE}$	SCLK falling edge to $\overline{SYNC}$ ignore, 1.7 V ≤ IOV_{DD} < 2.7 V	10			ns
	SCLK falling edge to $\overline{SYNC}$ ignore, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	5			
t_{LDACSL}	Synchronous update: $\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge, 1.7 V ≤ IOV_{DD} < 2.7 V	50			ns
	Synchronous update: $\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	50			
t_{LDACW}	$\overline{LDAC}$ low time, 1.7 V ≤ IOV_{DD} < 2.7 V	20			ns
	$\overline{LDAC}$ low time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	20			
t_{CLRW}	$\overline{CLR}$ low time, 1.7 V ≤ IOV_{DD} < 2.7 V	20			ns
	$\overline{CLR}$ low time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	20			



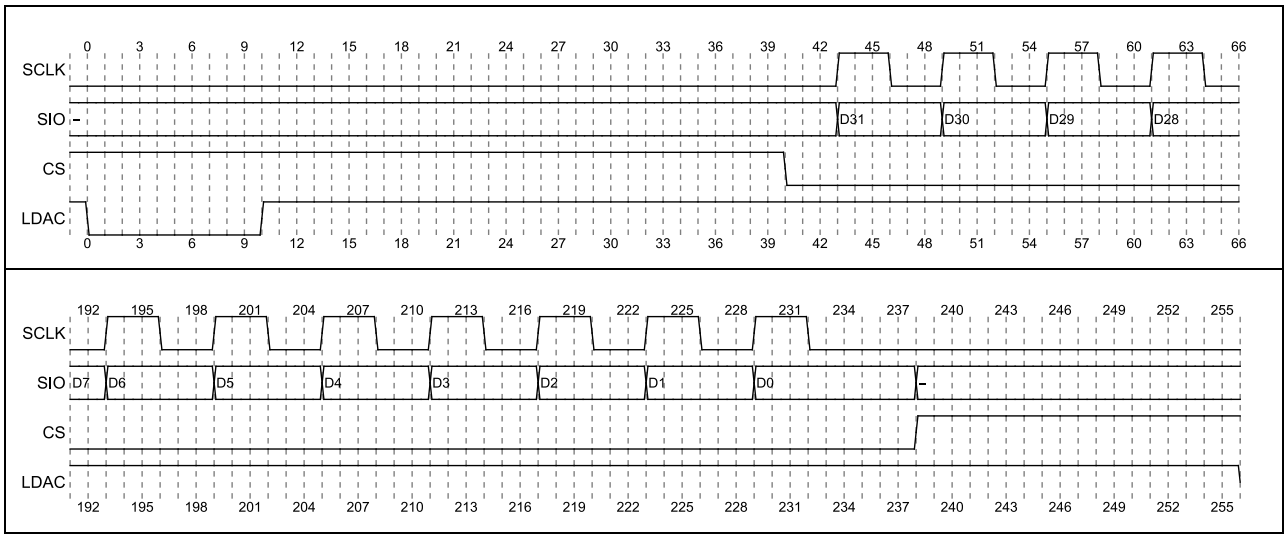


Figure 5: Timing diagram from the DAC11001B data sheet (top), timing requirements (second) and proposed FPGA timing (full acquisition cycle, zoomed in at start of acquisition cycle and end of acquisition cycle).