LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

LIGO Laboratory / LIGO Scientific Collaboration

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LIGO ADC Tests

Daniel Sigg Marc Pirello

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This is an internal working note
of the LIGO Laboratory.

California Institute of Technology
LIGO Project – MS 18-34
1200 E. California Blvd.
Pasadena, CA 91125
Phone (626) 395-2129
Fax (626) 304-9834
E-mail: info@ligo.caltech.edu

Massachusetts Institute of Technology
LIGO Project – NW22-295
185 Albany St
Cambridge, MA 02139
Phone (617) 253-4824
Fax (617) 253-7014
E-mail: info@ligo.mit.edu

LIGO Hanford Observatory
P.O. Box 159
Richland WA 99352
Phone 509-372-8106
Fax 509-372-8137

LIGO Livingston Observatory
P.O. Box 940
Livingston, LA 70754
Phone 225-686-3100
Fax 225-686-7189

http://www.ligo.caltech.edu/

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1 Summary

1.1 General

Testing low noise converters is difficult since the device's non-linearity depends on the signal strength and requires signals with big swings to exposed noise in neighboring frequency bins. Both DACs and ADCs experience this type of noise. If one device is used to test the other, dedicated high quality analog circuits are required in-between to reduce the signal amplitude at the frequencies of the main signal and measure the distortion in close-by frequency bins.

A further difficulty is that the up- and down-converted noise heavily depends on the signal amplitude, the signal frequency distribution and the converter technology. A unified noise model may not be readily deducible, and a fixed noise curve, such as presented in E1800243 for DACs and G2201909 for ADCs, may not represent real world circumstances.

Most of our analog circuits such as AI, AA and whitening filters were built with converters in mind that had noise levels at and around 1µV/√Hz whereas newer devices may approach noise levels below 100nV/√Hz. Consequently, their contribution to the noise is no longer negligible in all circumstances.

We recommend developing test procedures and setups that include dynamic signal testing for our electronics in critical places.

1.2 LIGO ADC

The LIGO ADC generally performs better than the previously tested 16-bit and low noise ADCs from General Standards. Compared to the 16-bit ADC the noise is more than an order of magnitude lower and compared to the low noise ADC a factor of around 3.

Since all switching power supplies on the board are synchronized with GPS we expect to see none of the intermodulation products of the previous boards.

2 Introduction

The DCC node for the LIGO DAC is E2300322.

The measurements for the low noise ADC can be found in the "A+/O4 OMC DCPD Whitening Chassis Redesign Oct 2022 Update" at G2201909.

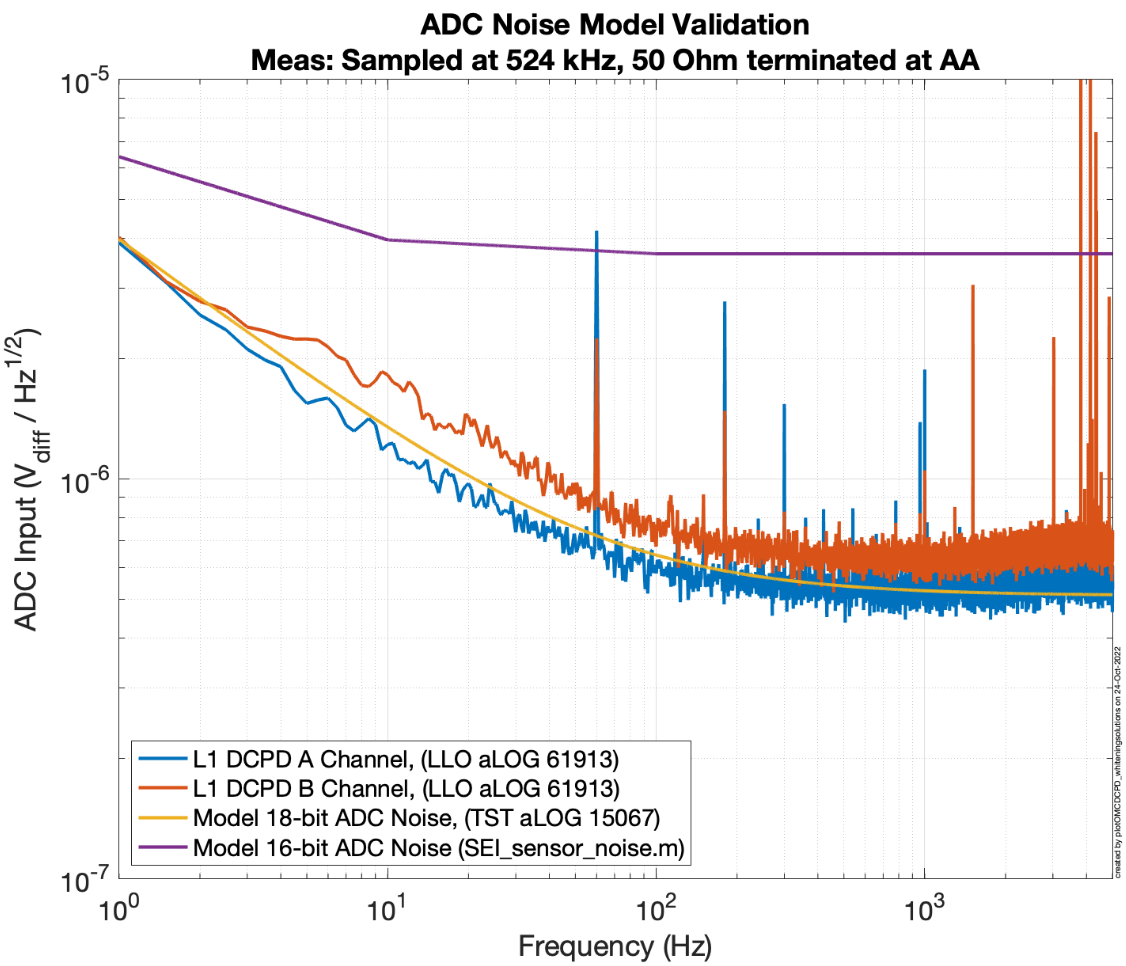
The test setup is using the hardware described in E2500146.

3 DC Tests

The DC test applies a fixed DC voltage that is heavily low-pass filters to the input of the ADC and measures the noise as readout by the test setup.

3.1 Previous ADCs

For comparison we cite the noise plot from page 1 in G2201909. It shows the noise at 1 kHz of the 16-bit ADC at roughly 4 µV/√Hz, and the noise level of the low noise ADC at 500 nV/√Hz with a full-scale range of ±20 V. When comparing it to the DAC results keep in mind that its full-scale range is only half at ±10 V.

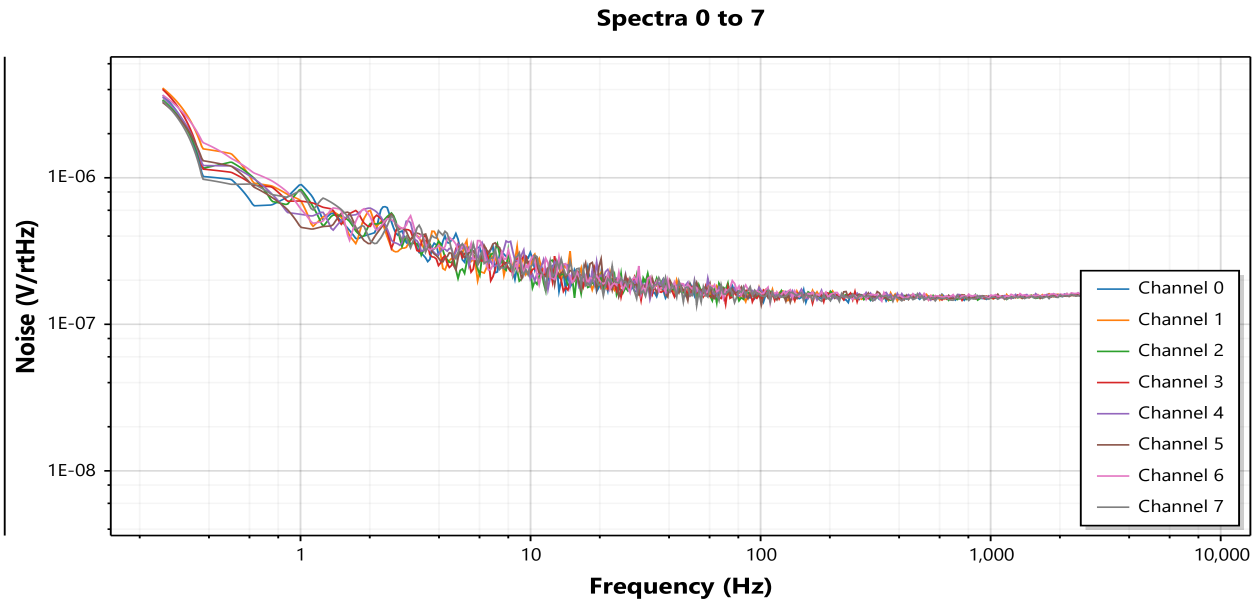


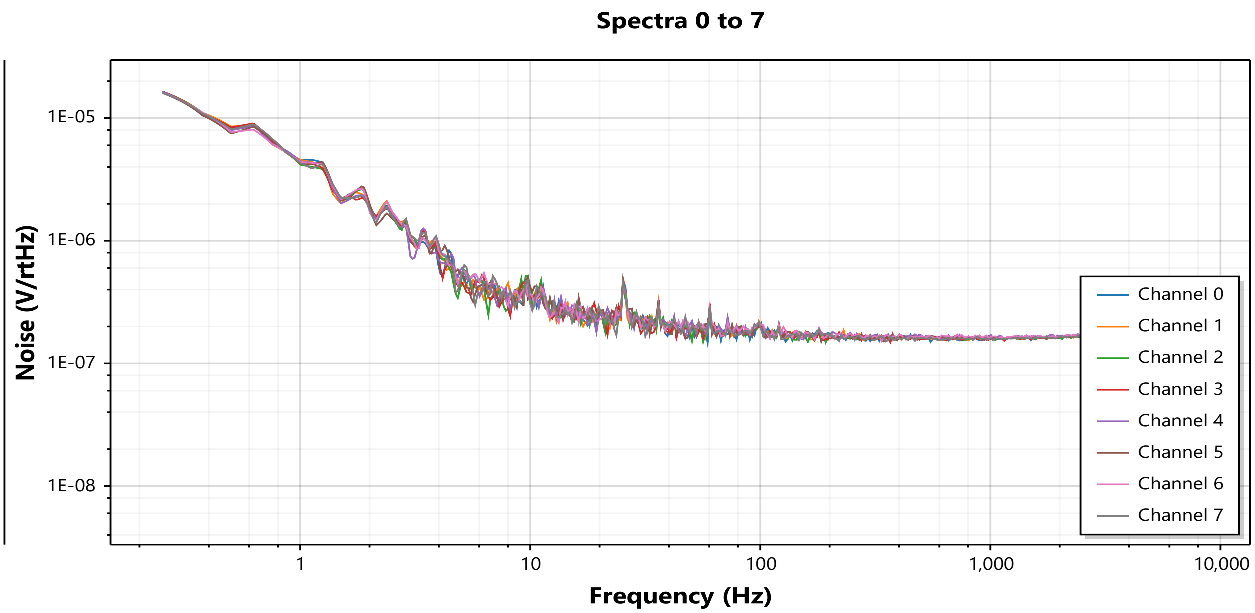
Plot 1: Noise measurements for the low noise ADC (General Standards PCIE66-18AI64SSC750K) in red and blue, and the 16-bit ADC (General Standards PCIe-16AI64SSC-64-50) in purple. A noise model for the low noise ADC is shown in yellow.

3.2 LIGO ADC

Plot 2 shows a plot of the noise of the LIGO ADC at fixed voltages of 0 V and 8 V. The measurement was done on the test stand described in E2500146.

We can see that the noise at 1 kHz is around 170 nV/√Hz and around 200 nV/√Hz at 100 Hz with an 8 V input signal. It is slightly lower with 0 V input with 160 nV/√Hz at 1 kHz and 170 nV/√Hz at 100 Hz. This is a full factor of 3 better than the low noise ADC from General Standards.





Plot 2: LIGO ADC noise at fixed offset voltages. Top plot is with 0 V input, whereas bottom plot is with 8 V input.

4 Dynamic Tests

TBD.